

Bruno Cavalcante de Souza Sanches

**An Application Specific Signal Processor for Gaseous
Detector Systems in High Energy Physics Experiments**

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Detector Systems in High Energy Physics Experiments**

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Supervisor: Prof. Titular Wilhelmus Adrianus Maria Van Noije

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*This work is dedicated to my beloved partner Larissa Marconi,
to my family and to the ones who contributed to its development.*

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“O Homem que a cada dia se supera dá sentido a vida.”

Sensei Walter José de Moraes

“Muitas vezes somos como cegos lendo em braille em uma mesa cheia de areia.”

Bruno Sanches

“Nossa maior fraqueza está em desistir.

O caminho mais certo de vencer é tentar mais uma vez.”

Thomas Alva Edison

*“Una volta che abbiate conosciuto il volo, camminerete sulla terra guardando il cielo,
perché là siete stati e là desidererete tornare.”*

Leonardo Da Vinci

“What we usually consider as impossible are simply engineering problems. . .

There’s no law of physics preventing them.”

Michio Kaku

“Everyone wants the project to be good, fast, and cheap...

Pick two.”

Unknown

Resumo

Nesta tese foi realizado um estudo sobre front-ends para física de altas energias, tendo como foco a atualização do experimento ALICE (A Large Ion Collider Experiment) no LHC (Large Hadron Collider) do CERN (Conseil Européen pour la Recherche Nucléaire). Devido a diversas alterações e a uma maior taxa de eventos, foi necessário desenvolvimento de um novo ASIC (Application Specific Integrated Circuit) para fazer a leitura dos sinais nos detectores TPC (Time-Projection Chamber) e MCH (Muon Tracking Chambers). Este chip foi denominado SAMPa (Serialized Analog-digital Multi-Purpose ASIC) e é um circuito integrado de sinal misto e leitura contínua com 32 canais. Este trabalho aborda fundamentalmente a parte digital deste chip e as melhorias, metodologias e estratégias utilizadas em seu desenvolvimento. O ASIC anteriormente utilizado no TPC apresentava eventos errôneos de travamento em seus filtros FIR (Finite Impulse Response) e visando uma solução para isso, foram melhorados o condicionamento de sinais e os filtros de correção de baseline em relação a sua tolerância a falhas e resistência a erros causados pela radiação. Foi implementado um novo filtro não linear complementar aos filtros existentes, de modo que a capacidade de estimativa de baseline ininterrupta pudesse ser atingida. Foi proposto um protocolo baseado em pacotes com capacidades de correção de erros, o qual tolera até duas falhas por cabeçalho ao custo de apenas 0,07% de largura de banda. Para alcançar a solução final para o CERN, quatro protótipos diferentes foram fabricados na tecnologia TSMC 130 nm, os ASICs SAMPa MPW1, V2, V3 e V4. Essas versões foram necessárias para obter de forma incremental um design otimizado que atendesse as várias restrições e especificações exigidas. Iniciou-se por uma versão reduzida com 3 canais, que foi irradiada com prótons sendo a fonte inicial de dados de seção de choque do SAMPa. Foi então projetada a primeira versão completa do chip, o SAMPa V2 um ASIC com características únicas nunca realizado antes. Este chip foi testado funcionalmente e se aproximou das necessidades dos experimentos. Porém, irradiações mostraram problemas relacionados a latch-ups. Uma técnica de prevenção de latch-ups foi então desenvolvida, a qual foi aplicada nas novas versões do chip. Foi ainda proposto um sistema de otimização baseado em algoritmos genéticos com o objetivo de obter implementações balanceadas em relação a área, potência e tolerância a erros. Foram desenvolvidas mais duas versões do SAMPa, contendo correções e melhorias na resistência a radiação da parte digital, o SAMPa V3 e V4. Novas irradiações mostraram que o projeto estava adequado e um teste de laser pulsado confirmou as hipóteses levantadas sobre a origem dos latch-ups, sendo que com as alterações propostas, uma redução de mais de 99% da seção transversal foi alcançada. O SAMPa V4 foi bem-sucedido e aprovado para uso pelo ALICE. Um protótipo adicional denominado MPW5 foi posteriormente projetado, extendendo este trabalho por meio de avaliações comparativas e testes com o otimizador abordando novas implementações do filtro FIR e do SAR (Successive Approximation Register) ADC (Analog-to-Digital

Converter). Os blocos foram testados e validados por meio de irradiações no acelerador Pelletron da USP (Universidade de São Paulo), onde obteve-se novos tempos médios entre falhas que apresentaram relevantes melhorias superiores a mil vezes, fornecendo importante base estrutural e experimental para novos projetos.

Palavras-chave: MICROELETRÔNICA. DETECÇÃO DE PARTÍCULAS. LHC. CIRCUITOS INTEGRADOS. PROCESSAMENTO DIGITAL DE SINAIS. FÍSICA DE PARTÍCULAS. ACELERADOR DE PARTÍCULAS. ÍONS PESADOS. OTIMIZAÇÃO NÃO LINEAR. ALGORITMOS GENÉTICOS. RADIAÇÃO IONIZANTE.

Abstract

In this thesis, a study on front-ends for high energy physics was developed focusing on the ALICE experiment upgrade at the CERN LHC. Due to a higher event rate and several other changes, the development of a new ASIC was necessary to support the signal readout in the TPC and MCH detectors. This chip was named SAMPA (Serialized Analog-digital Multi-Purpose ASIC) and is a continuous readout mixed-signal integrated circuit with 32 channels. The present work fundamentally addresses the digital part of this chip and the improvements, methodologies and strategies used in its development. The previous ASIC used in TPC presented erroneous lockout events in its FIR filters and aiming in a solution for this, the signal conditioning and baseline correction filters were modified concerning also their fault tolerance and resistance to errors caused by radiation. A new non-linear filter complementary to the existing filters was implemented so that an uninterrupted baseline tracking ability could be achieved. A dedicated packet-based protocol with error correction capabilities is also proposed, tolerating up to two faults per header and adding just 0.07% bandwidth overhead. To achieve the final solution for CERN, four different prototypes were manufactured using TSMC 130 nm technology, which were SAMPA MPW1, V2, V3 and V4. These versions were necessary to incrementally achieve an optimal design satisfying the several constraints and specifications required. The initial implementation was a reduced version with 3 channels, that was further irradiated with protons being the initial source of cross-section data for SAMPA. With these practical results, the first complete version of the chip was designed, the SAMPA V2, being a unique ASIC never realized before. This chip was functionally tested and was very close to the CERN's needs. However, irradiations revealed problems related to latch-ups. A latch-up prevention technique was further developed during this thesis, which was applied to the new versions of the chip. A novel optimization system based on genetic algorithms was also proposed to obtain balanced implementations concerning area, power and error tolerance. Two more versions, SAMPA V3 and V4, were developed implementing corrections and improvements in the radiation tolerance of the digital part. New irradiations showed that the design was adequate and a pulsed laser test confirmed the hypotheses raised about the origin of the latch-ups, wherewith the proposed changes, a reduction of more than 99% of the cross-section was achieved. Finally, with the successful measurements, SAMPA V4 was approved for use by the ALICE collaboration. An additional prototype named SAMPA MPW5 was further designed, permitting the extension of this work by performing tests with the optimizer and new implementations of the FIR baseline correction filter and the SAR ADC control block. The designs were tested and validated through irradiations using the Pelletron accelerator at USP; with these measurements, new mean times between failures were obtained showing improvements greater than a thousand times and also providing a relevant architectural and experimental base for new projects.

Keywords: MICROELECTRONICS. PARTICLE DETECTION. LHC. INTEGRATED CIRCUITS. DIGITAL SIGNAL PROCESSING. PARTICLE PHYSICS. PARTICLES ACCELERATOR. HEAVY IONS. NONLINEAR OPTIMIZATION. GENETIC ALGORITHMS. IONIZING RADIATION.

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Acronyms

ADC analog to digital converter.

ALICE A Large Ion Collider Experiment.

ALTRO ALICE TPC Readout.

AMS Austria Micro Systems.

ASIC application specific integrated circuit.

ATLAS A Toroidal LHC Apparatus.

BC1 baseline correction 1.

BC2 baseline correction 2.

BC3 baseline correction 3.

BGA ball grid array.

BNL Brookhaven National Laboratory.

CERN Conseil Européen pour la Recherche Nucléaire.

CFD constant fraction discriminator.

CITAR Radiation Tolerant Integrated Circuits.

CMFB common-mode feedback.

CMOS complementary metal oxide semiconductor.

CMS Compact Muon Solenoid.

CRU common readout unit.

CSA charge sensitive amplifier.

DAC digital to analog converter.

DAQ data acquisition.

DC direct current.

DCS detector control system.

DDF data flip flop.

DFT design for test.

DICE dual interlocked cell.

DNL differential non-linearity.

DRC design rule check.

DS digital shaper.

DSP digital signal processor.

DUT device under test.

EDA electronic design automation.

ENC equivalent noise charge.

ENOB effective number of bits.

EOC end of conversion.

ESE Electronic Systems for Experiments.

FEC front-end cards.

FinFET fin field effect transistor.

FIR finite impulse response.

FIT failures in time.

FPD fixed pedestal.

FPGA field programmable gate array.

FSM finite state machine.

GBT gigabit transceiver.

GdSP Gas Detector Digital Signal Processor.

GEM gas electron multiplier.

HDL hardware description language.

HEP high energy physics.

HEPIC High Energy Physics and Instrumentation Center.

HIF Heavy-ion Irradiation Facility.

HMR hamming modular redundancy.

HPS hard processor system.

HSMC high speed mezzanine card.

I2C inter-integrated circuit.

IEEE Institute of Electrical and Electronic Engineers.

IFUSP Physics Institute of São Paulo University.

IIR infinite impulse response.

IN2P3 Institut National de Physique Nucléaire et de Physique des Particules.

INL integral non-linearity.

IO input/output.

IP intellectual property.

ISCAS International Symposium on Circuits and Systems.

JEDEC Joint Electron Device Engineering Council.

JTAG Joint Test Action Group.

LERI Ionizing Radiation Effects Laboratory.

LET linear energy transfer.

LHC Large Hadron Collider.

LHCb Large Hadron Collider Beauty Experiment.

LS2 long shutdown 2.

LSB least significant bit.

LUP latch-up preventing.

LUT look-up table.

MAF moving average filter.

MCH Muon Chambers.

MIM metal-insulator-metal.

MLM multi layer mask.

MMMC multi mode multi corner.

MPGD micro-pattern gas detector.

MPW multi-project wafer.

MSps mega-samples per second.

MTBF mean time between failures.

MUX multiplexer.

MWPC multi-wire proportional chambers.

NICA Nuclotron-based Ion Collider Facility.

NSREC Nuclear and Space Radiation Effects Conference.

PASA Preamplifier Shaper.

PMR penta modular redundancy.

PRR production readiness review.

PSRR power supply rejection ratio.

PZC pole-zero cancellation.

QFN quad-flat no-leads.

QGP quark-gluon plasma.

QOR quality of results.

R/W read/write.

RCU readout control unit.

RF radio frequency.

RHIC Relativistic Heavy-ion Collider.

RTL register transfer level.

SAMPA Serialized Analog-digital Multi-Purpose ASIC.

SAR successive approximation register.

SCM signed coefficient multiplier.

SDF standard delay format.

SECDED single error correction double error detection.

SEE single event effect.

SEL single event latch-up.

SET single-event transient.

SEU single-event upset.

SLVS scalable low-voltage signaling.

SoC system on chip.

SOI silicon on insulator.

SOS second order section.

SRAM static random-access memory.

TCAD technology computer-aided design.

TID total ionizing dose.

TMR triple modular redundancy.

TMRG triple modular redundancy generator.

TPC Time Projection Chamber.

TSL The Svedberg Laboratory.

TSMC Taiwan Semiconductor Manufacturing Company.

UCL Université Catholique de Louvain.

UiB University of Bergen.

UiO University of Oslo.

USP University of São Paulo.

VPD variable pedestal.

ZSU zero suppression unit.

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1 Introduction

1.1 Motivations

With the increase of the computational systems complexity along the time, the amount of digital logic in the same chip area is getting extremely high.

This opens opportunities for new applications, services and research, providing more processing power and memory for systems and users. But at the same time that this is good, it also implies that there are more and more devices that can suffer logic errors caused by external effects, possibly causing malfunctions, mistakes and losses.

One important class of nondestructive functional errors is known as soft errors and may usually be induced by energetic ion strikes. Soft errors can be linked to single event effects (SEEs) (JEDEC, 2006), and include several phenomena that will be discussed further in this work.

In general, soft errors can happen even without any aggressive environment and may be induced by alpha particles emitted from radioactive impurities in materials nearby the sensitive volume, such as packaging, solder bumps, etc., and by highly ionizing secondary particles produced from the reaction of both thermal and high-energy neutrons with component materials. Cosmic rays are other possible source (ZIEGLER, 1996; O'GORMAN *et al.*, 1996).

While the apparent error rates may seem as extremely low for several standard systems in common environment (O'GORMAN *et al.*, 1996), in more elaborated scenarios and with critical devices these errors can lead to the total inapplicability of the system.

This opens a wide field of investigation aiming the increase of device reliability. Typical scenarios for that are on devices operating in standard conditions but needing to have really low error rate and the case where the environment is aggressive (for example, there is radiation involved), and the designer needs to control the error rate. The scenario can also be a balanced mix of both cited cases.

One relevant case to be evaluated is the one with radioactive interactions, as this is an important known generator of errors and malfunctions in digital electronic devices (DODD *et al.*, 2010).

There are several kinds of systems that suffer from these types of logic errors; some examples are health support equipment, monitoring devices in nuclear power plants, circuits in satellites and electronics in high energy physics detectors. There is a broad list of circuits and various of them could take advantage of radiation tolerance improvements.

Resistance to errors caused by radiation is a common practice in space electronics engineering and several works can be cited; however, some not so standard ground situations will be referenced to show the wideness of applicability in the area before describing the specific target in this work.

In Wilkinson *et al.* (2005) a study over cancer-radiotherapy equipment as a cause of soft errors in electronic equipment is conducted, showing that devices in the environment may suffer from radiation effects of this equipment. This implies that these devices need special care in terms of logic errors and redundancy.

An important case to be cited is Elders *et al.* (2013) where implantable cardioverter defibrillators are studied and an impressive result was found showing that soft errors happened and the events were probably due to the incidence of neutrons originated from medical treatment, like radiotherapy.

Now focusing on the environment where this work is mainly involved, a very relevant area is the high energy particle physics, more specifically the integrated circuits dedicated to the processing and readout of events in particle accelerators and colliders.

In this scenario, the Large Hadron Collider (LHC) at the Conseil Européen pour la Recherche Nucléaire (CERN) rises as one remarkable reference in the area (CERN, 2012a), being the biggest particle accelerator in the world. The LHC has maintenance and improvement windows called long shutdowns and an important one has been during 2019 and 2021.

In this window, improvements in electronics could be carried out to support the increasing needs of the involved experiments. Timely, one important experiment called A Large Ion Collider Experiment (ALICE) announced its plans for the upgrade and a critical requirement was a new application specific integrated circuit (ASIC) to compose the front-end electronics involved in the readout of events in the Time Projection Chamber (TPC) and Muon Chambers (MCH) detectors.

The types of systems and their basic working principles will be reviewed further, but the main point is that they are also exposed to environments with radiation and usually will suffer errors caused by the interactions, and in this way may need some form of protection.

The work of Roed, Brugger and Spiezia (2011) presents an overview of the radiation environment at the CERN LHC where the energy spectra is covered together with fluence aspects, very important for the evaluation of single event effects correlated to this work; total dose analysis is also treated.

Tsiligiannis *et al.* (2018) shows that radiation effects continue to have relevance in environments with mixed-field radiation and even on deep sub-micrometer technologies where 28 nm static random-access memory (SRAM) based field programmable gate array

(FPGA) designs are studied to be applied under the CERN experiments.

Several works released from CERN researchers refer to ASIC projects, their radiation resistance and testing due to a constant need for dedicated designs; as an example it is possible to cite Rosa (2017) characterization of a new chip called VFAT3 for the data acquisition electronics of the Compact Muon Solenoid (CMS) detector. Other related paper is Andreotti *et al.* (2018) where the chip CLARO8 for the upgrade in Large Hadron Collider Beauty Experiment (LHCb) detector at CERN is briefly presented including radiation hardness characterization and its prototypes.

In Mager *et al.* (2012) an analysis is made with single event upset data from one important detector part of ALICE, where moderate radiation exposition is claimed to be present and the authors state the need of a careful selection of the components together with means to protect their functionality against soft errors; this need is right in the direction of the present thesis line of action.

Mager *et al.* (2012) was extensively based on studies over the ALICE TPC Readout (ALTRO) chip (CERN, 2003; BOSCH *et al.*, 2003) an important part of the ALICE detector front-end. The ALTRO replacement by a new and more complete integrated circuit is one of the targets of the ALICE upgrade and also of this work.

In this way, it is possible to find several cases of systems exposed in colliders, where this work could contribute in the area of ASICs for particle physics experiments and focusing on digital readout aiming to investigate the design and comprehensively add elements to help maintaining the functional performance of the device in the aggressive environment.

The first line of work will be in the development of an application specific digital signal processor for a real ASIC made to be used in ALICE at the LHC. The application itself will be described in section 2.2, where the need of this ASIC is justified in section 2.4.

A second main line will take advantage of the several scenarios, modules and characteristics learned from the development of a state of art detector chip, and work in possible actions to the control or mitigation of errors caused by radiation effects in the logic.

The focus then will be changed to the development and implementation of automated actions in the chip design using the proposed strategies in the last step targeting for fast and optimized results considering tradeoffs in the design of complex chips.

To accomplish with this automation, software tools with artificial intelligence algorithms will be developed and tested in selected blocks extracted from the designed particle physics readout ASIC project restrictions, aiming for a proper evaluation of the algorithms in real application.

With this scenario, it is also possible to specify that this work will focus on the mitigation of nondestructive errors in digital logic based blocks and ASICs, targeting solutions in the direction to changes in hardware, not in software, as it is very frequent to have designs without standard processors or software at all in this field.

There are several ways to design a digital logic integrated circuit, including standard cell based design, full custom design, array based strategies and others.

One frequent solution is the design using synthesis from register transfer level (RTL) hardware description language (HDL) or higher level sources. This is usually followed by place & route of standard cells, due to its fast, flexible and general approach, satisfying a wide range of design constraints, but without the slow and extensive work of dealing with full custom design.

Standard cells are layout implementations of basic logic functions frequently needed by digital designs. Normally, the cells are very simple, containing one or very few digital logic gates. One general approach used in the layout is that the cells should have the same height, so the cells can be easily placed side by side as rows. Another advantage is that the power lines can be automatically connected in horizontal low level metal layers as the cells are laterally juxtaposed (BRODERSON, 1981; ILIN; RYZHOVA; KORSHUNOV, 2018).

In addition, one of the major positive aspects of the standard cells is that, in general, it is possible to get a full set of designed cells from the foundry, and this arrives in a form of a design kit with silicon proven layouts already tested, measured and characterized. Also models extracted from the characterization are normally generated too, which simplify the design flow (ILIN; RYZHOVA; KORSHUNOV, 2018).

One possible option for hardening should be the modification or redesign of the standard cell kit to create a protected final chip using the standard digital flow, the papers from Liu *et al.* (2016), Rockett and Kouba (2008), Cameron *et al.* (2014), Liu *et al.* (2014) deals with hardening by design making its steps to achieve cells for process between 65 nm and 180 nm.

Kumari and Mekie (2017) even go further where simulations for upset hardened dual interlocked cell (DICE) in much newer process were addressed including technology nodes of 180 nm, 130 nm, 65 nm and 40 nm for planar devices and 20 nm, 16 nm, 14 nm, 10 nm and 7 nm for fin field effect transistor (FinFET) devices.

These techniques have good performance, coming at the cost of area and power, but the real problem then is that there are a lot of work and costs involved in the design kit development and this generates a big risk for the time to market and quality of results (QOR) which several teams are not prone to take.

Other restrictions can also exist like the impossibility of changing the design kit cells or the hiding of the real content of the cells and several other legal issues that can

interfere.

Due to that, the present work intends to increase the design tolerance to errors caused by interactions with radiation, but without changing the base layout of the design kit.

In this direction, the work of Sielewicz (2018) deal with redundancy and fault tolerance in FPGA designs subject to radiation, where the designer can not change the predefined logic blocks, and strategies to mitigate errors and configurations changes are addressed.

These changes are based on manual approaches which tend to be difficult to apply when time to market is critical. The work Andrikos, Violante and Codinachs (2013) proposes an automated technique for FPGAs, where they shown that automated approaches boost both the productivity of the designers and the QOR of the final implementations.

Focusing back in ASICs and restricting the view to the standard cell case, it is possible also to find works aiming automation both in the analysis, detection of faults and in the hardening itself.

The publications Coelho, Zergainoh and Velazco (2019), Velazco, McMorrow and Estela (2019), Mansour and Velazco (2013), Ganapathy *et al.* (2014) and Mansour *et al.* (2013) deal with techniques and automated tools for evaluation of devices, also covering the estimation of the sensitivity to soft-errors of integrated circuits using fault injections emulating both single event upsets and transients. With further work and the feedback of this kind of analysis in an optimization loop an optimization strategy could possibly achieve better results as the changes in the design may be more effectively targeted.

Is also very important to cite the works Bavache *et al.* (2020), Stamenkovic and Petrovic (2016), Oh and Kaneko (2015) and Chiusano, Carlo and Prinetto (2002) addressing automated strategies for fault tolerance in device, circuit, and system. Where Bavache *et al.* (2020) operates over system on chips, Chiusano, Carlo and Prinetto (2002) deals with synthesis in general and Oh and Kaneko (2015) is more directed to data-path creation.

Quijada *et al.* (2019) and Hindman *et al.* (2011) are also important contributions to automation in fault tolerance where logic design methodology for radiation hardened by design high-speed logic using fine-grained triple modular redundancy are presented, which is similar to one of the techniques of protection further used in the present work.

Finally, the paper Sousa, Anghinolfi and Ferreira (2013) shares an environment similar to the one in the present work while developing automated strategies for upset mitigation in high energy physics experiments aiming to reduce the implementation time.

Therefore, it is possible to synthesize from the literature that several efforts in radiation resistance improvement exist and it is a relevant problem that keep appearing in

several areas.

But at the same time that the discussed papers share some degree of automation, there still some difficulty to deal with trade-offs due to a lack of intelligence in the techniques and algorithms where most of them use an all or nothing redundancy approach needing supervision and a lot of designer feedback if the constraints and desired targets are antagonic or tight.

The cited scenario creates a relevant study opportunity as there is the need for a singular novel ASIC to operate in an environment with radiation in a real application with a big set of design constraints and also limited by several technological aspects including also area, power, costs, intellectual property and legal issues.

Developing the application specific processor needed by CERN is already an important contribution, but the present work also intends to produce a design methodology for radiation tolerance improvement using artificial intelligence to proper deal with trade-offs while maintaining a good connection to the industry reference design kits, along with modern electronic design automation tools.

1.2 Objectives

The first and most notable objective of this work is the development of a novel application specific signal processor with continuous readout capability for high energy physics experiments.

This processor is the largest block of the Serialized Analog-digital Multi-Purpose ASIC (SAMPA) chip, which is in the core of the data acquisition front-end and is a critical part for the ALICE upgrade, targeted to happen in the CERN shutdown window between 2019 and 2021.

This work also has as a secondary objective to provide a new strategy for automated radiation tolerance improvement in digital designs based on artificial intelligence algorithms, digital simulation tools and electronic design automation softwares. That will be addressed using real application examples and tests extracted from the ASIC being developed to CERN, in a virtuous loop where both objectives receive benefits.

Finally, due to artifacts encountered during the SAMPA development, a contribution concerning single event latch-up analysis and avoidance is made using a practical design rule check (DRC) based method that was validated with measurements from real fabricated prototypes using 130 nm technology, which were tested in irradiation beams both in Europe and Brazil.

1.3 Structure of the thesis

This work is organized in chronological order as follows. Chapter two addresses the main systems related to the operating environment of the ASIC being designed where some of the updates targeted to happen between 2019 and 2021 are also highlighted due to their impact on the device. The state of art in the readout electronics at ALICE TPC is further reviewed, rising a finer motivation for the present chip.

Chapter three is devoted to the description of the novel ASIC named SAMPA. It starts presenting a gaseous readout front-end architecture, culminating in the application specific signal processor.

The processor is then carefully described, from its input buffers to the final output serialization protocol. The signal conditioning and the digital filters are addressed filter by filter, being several of its main details highlighted.

The fabricated prototypes are further shown together with their main targets, composing blocks and micro-photographies, mapping the path up to the complete SAMPA chip.

The focus is then changed to radiation tolerance optimization, where the applied strategies are listed and a new automated radiation tolerance improvement algorithm is proposed.

A novel single event latch-up investigation and avoidance technique is also described and tested for the present project, culminating to the end of this chapter and motivating the testing of the fabricated prototypes.

Chapter four presents the measurement results and the extracted information of the irradiation tests performed. The full development path is covered, starting from the partial SAMPA MPW1, going up to the complete version to be used in CERN.

This chapter also has a final section addressing the design and irradiation of two important SAMPA blocks, the finite impulse response (FIR) filter and the successive approximation register (SAR). Results of the Pelletron irradiation tests executed are also deeply evaluated and discussed.

Finally, chapter five presents an overview and the main conclusions of this work followed by suggestions for the next steps.

2 The ASIC environment and state of art

CERN is a European organization founded in 1954 initially targeted to study nuclear physics (CERN, 2012a).

The CERN main research center is located astride the Franco-Swiss border near Geneva and administrate diverse particle accelerators. The organization has 22 member states and also several other associates and observers, all around the globe (CERN, 2012b; CERN, 2012a).

CERN has as mission the development of research in basic sciences, especially particle physics, technological applications, stimulate collaboration among scientists and create educational programs. Having by itself thousands of employees, the laboratory hosts more than 10.000 visiting scientists and engineers, representing hundreds of universities.

Most of the activities at CERN are currently directed towards operating the LHC and its detectors. The LHC represents a large-scale, worldwide scientific cooperation project.

2.1 LHC

The Large Hadron Collider is the world's largest and most powerful particle accelerator. It first started up on 10 September 2008, and remains the latest addition to CERN accelerator complex.

The LHC consists of a 27-kilometer ring of superconducting magnets with a number of accelerating structures to boost the energy of the particles along the way (CERN, 2014). These include 1232 dipole magnets 15 meters in length which bend the beams, and 392 quadrupole magnets, each 5–7 meters long, which focus the beams (CERN, 2014).

Inside the accelerator, two high-energy particle beams travel close to the speed of light before they are made to collide. The beams travel in opposite directions in separate beam pipes, two tubes kept at ultrahigh vacuum. They are guided around the accelerator ring by a strong magnetic field maintained by superconducting electromagnets. The electromagnets are built from coils of special material that operates in a superconducting state, efficiently conducting electricity with very low resistance or loss of energy. This requires chilling the magnets to -271.3 Celsius degrees, a temperature colder than outer space. For this reason, much of the accelerator is connected to a distribution system of liquid helium, which cools the magnets, as well as to other supply services (CERN, 2014).

LHC is also located in Switzerland and France in a tunnel that is approximately

between 50 m and 150 m deep underground depending on the location. Four main experiments exploit the high-energy beams provided by the LHC, these are the ALICE, CMS, LHCb and A Toroidal LHC Apparatus (ATLAS), as shown in figure 1 (CERN, 2014; MARCASTEL, 2014).

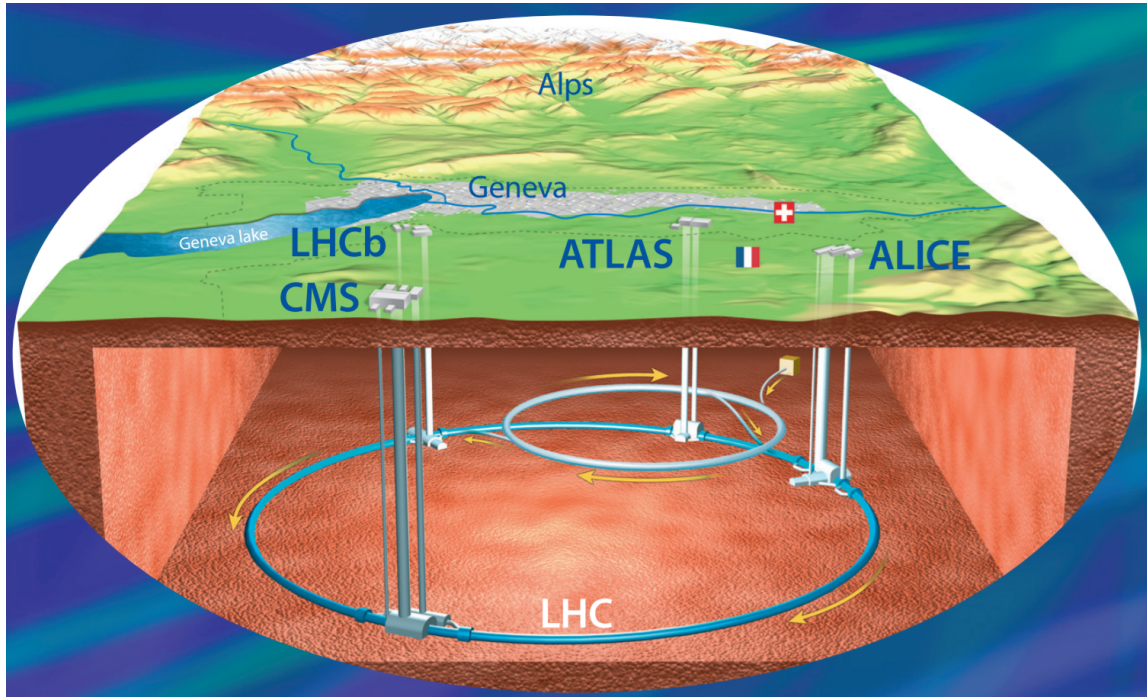


Figure 1 – Illustration of CERN LHC and its main experiments.

Source: Marcastel (2014).

2.2 ALICE

ALICE is a general-purpose heavy-ion experiment focused on studying the physics of strong interacting matter and the quark-gluon plasma (QGP) in collisions at the LHC. ALICE experiment is located at one of the collision points along the LHC, and targets primarily the study of the properties of the particles that are created in the Pb-Pb collisions.

Weighing 10.000 tonnes and with a height of 16 m and a length of 26 m, ALICE is a large and complex detector composed of 18 sub-detectors to track and identify the tens of thousands of particles produced in each heavy-ion collision. The ALICE detector is based on high precision systems for detecting and tracking the particles including miniaturized devices for processing electronic signals and a worldwide distribution of computing resources for data analysis, the ALICE grid (MARCASTEL, 2014).

An illustrative view of the ALICE experiment is shown in Figure 2. It has several parts and two notable ones are the central barrel and the forward muon spectrometer(8).

The ALICE Time Projection Chamber(15) is the main tracking detector in the central barrel (ALICE *et al.*, 2004).

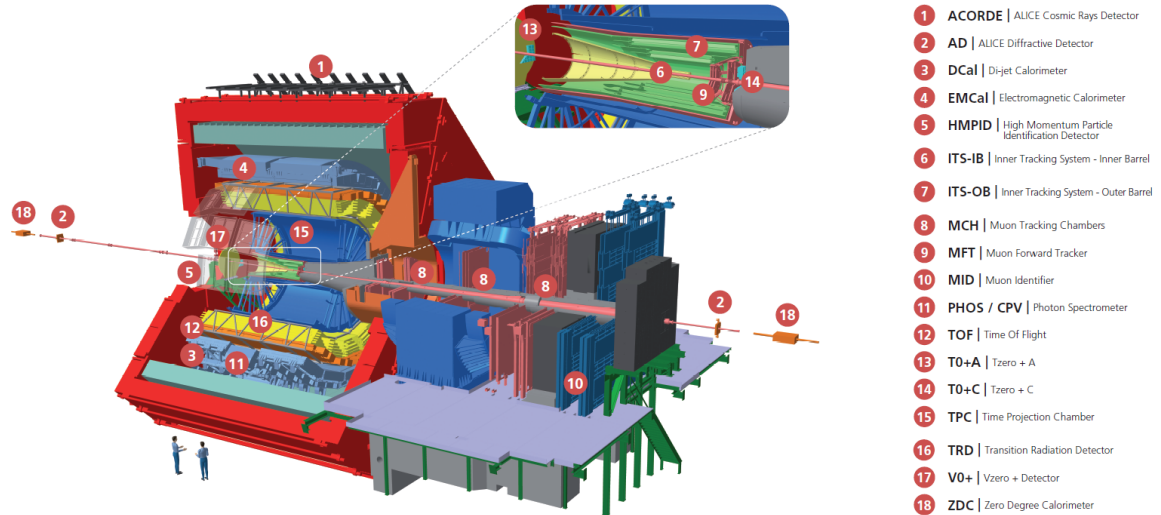


Figure 2 – Illustration of the ALICE experiment.

Source: Tauro (2017).

The TPC is based on gaseous detectors principle: "When any type of radiation that is energetic enough to ionize the gas confined between the electrodes of different polarity passes through, emergent electrons and ions are drifted towards the anode and cathode respectively hence produce an electrical current" (BLUM; RIEGLER; ROLANDI, 2008; HERNÁNDEZ, 2015). A schematic drawing for a simplistic gaseous radiation detector is given in figure 3 (HERNÁNDEZ, 2015).

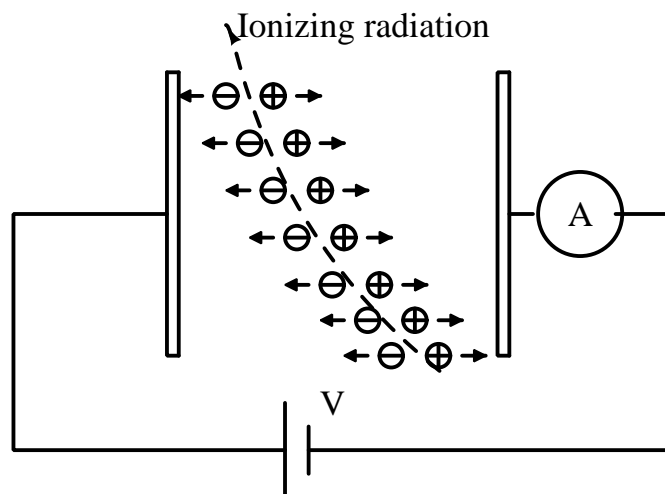


Figure 3 – Schematic drawing of a simplistic gaseous radiation detector.

Source: HERNÁNDEZ (2015).

2.2.1 ALICE TPC

The ALICE TPC consists of a $90m^3$ gas-filled (Ne-CO₂) detection chamber in an electric field with a position-sensitive electron collection system. Figure 4 illustrates the chamber (HERNÁNDEZ, 2015; ALME *et al.*, 2010; MAIRE, 2011).

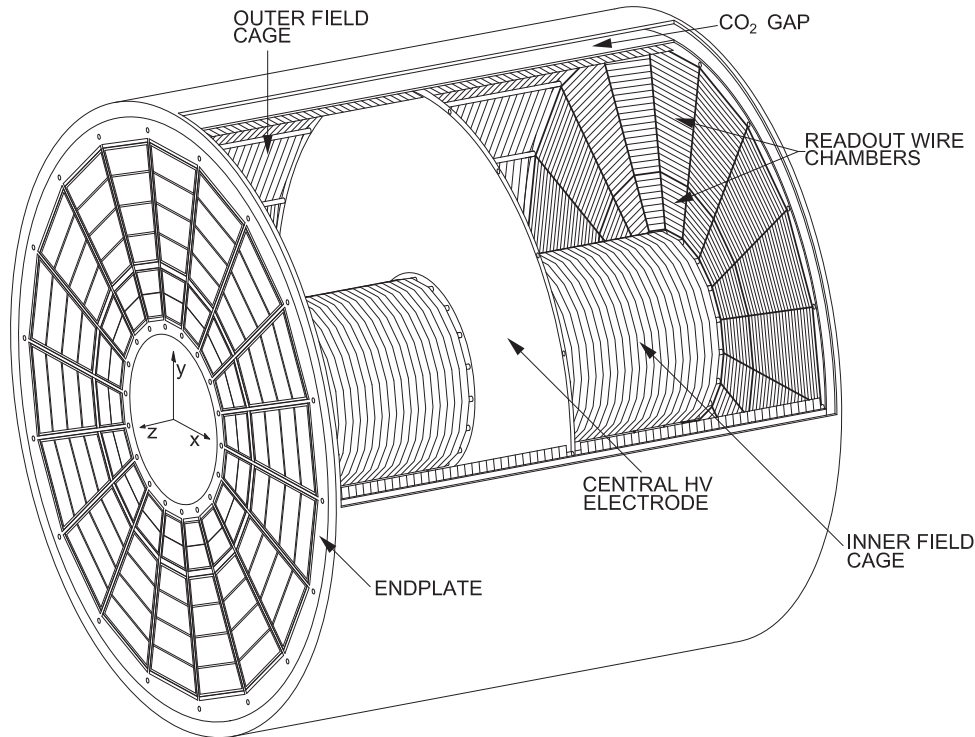


Figure 4 – 3D view of the TPC field cage.

Source: Alme *et al.* (2010), Maire (2011), HERNÁNDEZ (2015).

Along its length, the chamber is divided into halves by means of a central high-voltage electrode disc, which establishes an electric field between the center and the end-plates. On passing through the detector gas, a particle will produce primary ionization along its track. The ionization trail that a crossing particle leaves on a gas can be used to detect its trajectory. If an electric field is applied to the gas volume, most of the free ions and electrons will not recombine but rather drift in opposite directions towards the high voltage and the end-plates, where they can be sensed by the electronics after an amplification (HERNÁNDEZ, 2015).

The interpretation of the position in the readout plane where the electrons arrive gives a two-dimensional track information of the crossing particle. Since the drift velocity of the electrons and ions is on average constant in the medium, the arrival time gives information about the distance between the ionization trail and the end-plates. Therefore, a three-dimensional trajectory reconstruction is possible with a two-dimensional readout surface and the timing information (BLUM; RIEGLER; ROLANDI, 2008; ALME *et al.*, 2010; HERNÁNDEZ, 2015).

2.2.2 TPC signal amplification

The number of electrons generated by the passage of the particles through the gas is too small to be sensed and acquired by the usual electronics. Up to the LHC 2021 upgrade, the ALICE TPC used the multi-wire proportional chambers (MWPC) technology to multiply the number of free electrons by about four orders of magnitude (ALME *et al.*, 2010).

A MWPC schematic is illustrated in figure 5. On the end-plate inside the gas filled chamber a set of 3 staggered levels of wire grid named gating grid, cathode grid (or shielding grid) and anode grid (or sensing grid) generate the gas amplification. It presents two regions: the drift region or the effective volume where the trajectories of the crossing particles can be detected, and the amplification region where the ionization is amplified. A 100 kV voltage between the anode (positive) and the cathode grid (negative) is applied to produce the avalanche process that occurs at the vicinity of the anode wire grid (HERNÁNDEZ, 2015; ALME *et al.*, 2010).

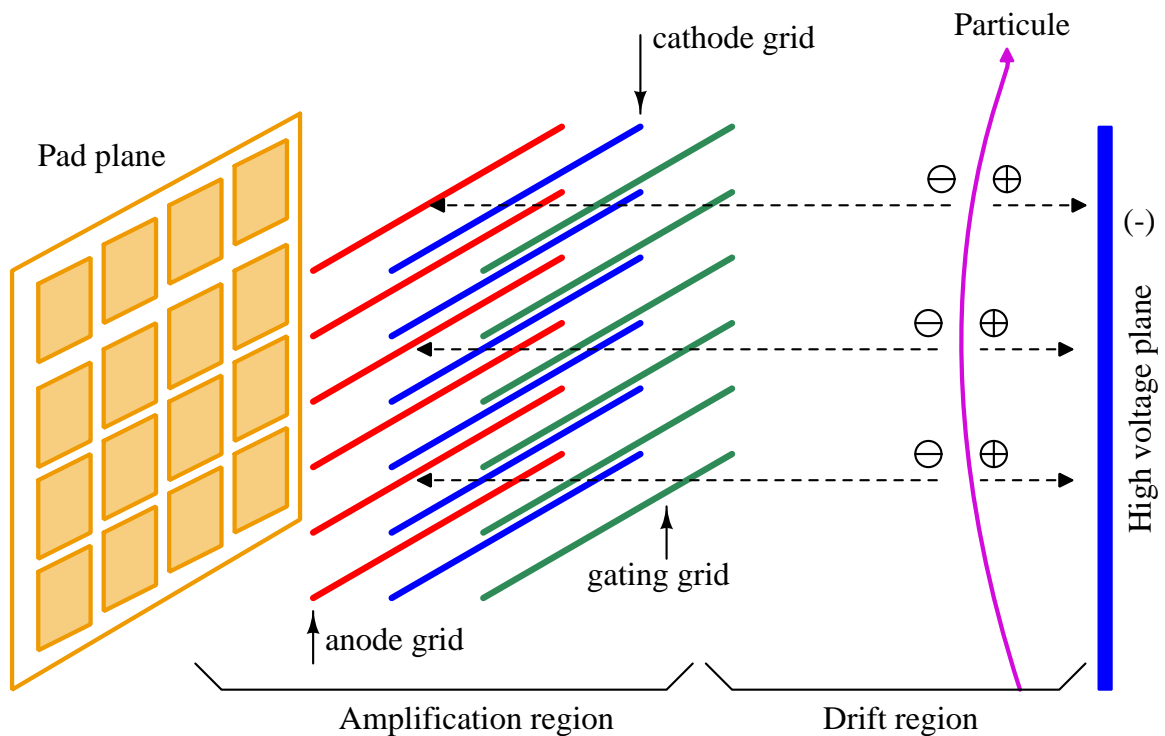


Figure 5 – Multi-Wire Proportional Chambers schematic.

Source: HERNÁNDEZ (2015).

The anode grid accelerates the primary electrons generated from the crossing particle ionization with enough energy to produce multiple secondary gas ionizations. The read-out pads and the cathode grid collect the ions generated during the avalanche process but only the charge signal read-out pads are used in the trajectory reconstruction. A fraction of the generated ions in the avalanche can travel back towards the drift volume.

The function of the gating grid is to collect these free ions avoiding that them entering into the drift volume and distorting the uniformity of the electric field (ALME *et al.*, 2010).

2.2.3 TPC read-out electronics

A TPC read-out system diagram is illustrated in figure 6 (MUSA, 2007). Charged particles traversing the TPC volume ionize the gas along their path, liberating electrons that drift towards the end-plate of the chamber. The signal amplification is provided through avalanche effect in the vicinity of the anode wires of the readout chambers. The electrons and positive ions created in the avalanche, which move, respectively, towards the anode wire and the surrounding electrodes, induce a positive current signal on the pad plane. The current signal of a single avalanche, which is characterized by a fast rise time (under 1 ns) and a long tail (of the order of 50 ms), carries a charge that, in the ALICE TPC, can be as low as few fC.

The charge then is delivered on the detector impedance which behaves near like a pure capacitance of the order of pF. The shape of the signal tail, which is due to the motion of the positive ions, is rather complex and depends on the details of the chamber and pad geometry. This tail, causing pile-up effects, sets the main limitation to the maximum track density at which a MWPC can be operated (ALME *et al.*, 2010).

The readout of the signal is done by 570.132 pads that form the cathode pad plane of the readout chambers. The signals from the pads are passed to front-end cards (FECs), located 7 cm away from the pad plane, via flexible Kapton cables.

In the FECs a custom ASIC with 16 charge sensitive amplifiers channels, named Preamplifier Shaper (PASA) implemented in Austria Micro Systems (AMS) C35B3C1 0.35 μm complementary metal oxide semiconductor (CMOS) technology (SOLTVEIT *et al.*, 2012), transforms the charge signal induced in the pads into a differential semi-Gaussian voltage signal that is fed to the input of the ALTRO ASIC (MUSA, 2003; CERN, 2003). The operating circuit has a conversion gain of 12 mV/fC, an output dynamic range of 2 V, and produces a pulse with a shaping time of about 190 ns.

The ALTRO ASIC was manufactured in the ST Microelectronics 0.25 μm CMOS technology with six metal and three poly-silicon layers. Each ALTRO contains 16 channels operating concurrently that digitize and process the input signals. The ALTRO chip contains 16 instances of the TSA 1001 analog to digital converter (ADC) from ST Microelectronics in the form of 8 ADC intellectual property (IP) blocks (ALME *et al.*, 2010).

This ADC has differential inputs and works at a clock frequency of 10 MHz with a resolution of 10 bits, while consuming around 12 mW. The digitized signal is then processed by a set of circuits that perform the baseline subtraction, tail cancellation, zero-suppression,

formatting and buffering into the ALTRO ASIC. The readout can take place at any time at a speed of up to 200 MByte/s through a parallel 40-bit-wide back-plane bus linking the FECs to the readout control unit (RCU), which interfaces them to the data acquisition (DAQ), the Trigger and the detector control system (DCS) (ALME *et al.*, 2010).

To be concise the description of current ALICE TPC readout will be ceased with this level of detail and better and deeper analysis will be done in respect to the future readout systems which is a relevant part of this work.

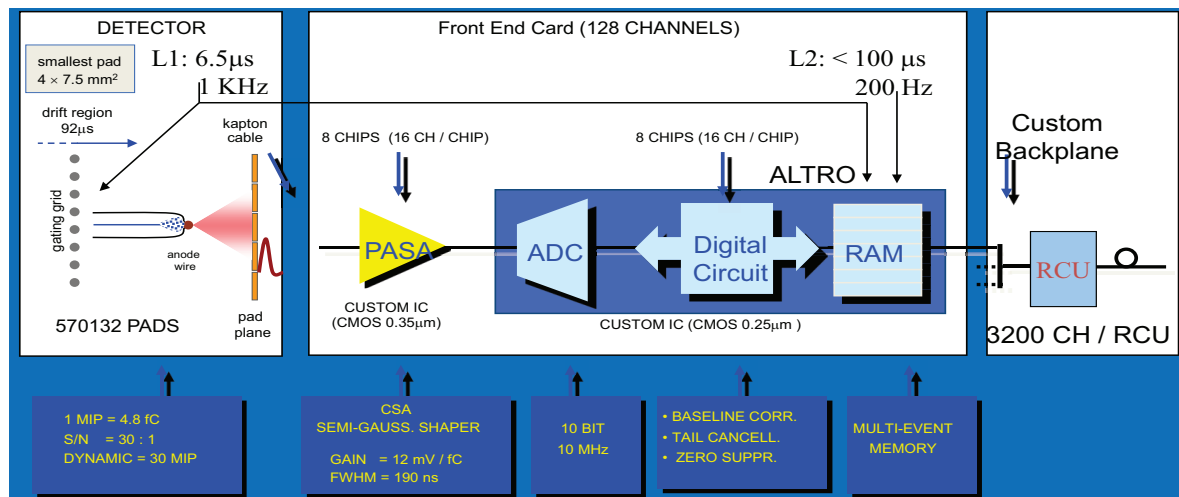


Figure 6 – Block diagram of the ALICE TPC front-end electronics.

Source: Musa (2007).

2.2.4 MWPC limitations

The MWPC technology used in the ALICE TPC has several limitations and some of these were discussed in ALICE (2013) and are briefly cited in the following list:

1. The maximum drift time of ions from the amplification region to the gating grid of the TPC MWPC is about $180 \mu\text{s}$. In order to provide efficient ion gating, the gating grid must be closed for $180 \mu\text{s}$ after the end of the electron drift. Additionally, a $100 \mu\text{s}$ past protection is applied to avoid event pile-up. This sets a first limitation of about 3.5 kHz to the maximum readout rate of the present TPC.
2. The anticipated particle rates at the wire chambers would reach $100 \text{ kHz}/\text{cm}^2$, for which space charge effects in the amplification region result in a few percent gain drop, thus deteriorating the dE/dx performance of the detector.
3. Operating the TPC in ungated mode, i.e. leaving the gating grid continuously open, would result in a severe buildup of space charge in the drift volume due to back drifting ions.

One solution to overcome these limitations of the MWPC is the change of the sensing and multiplying element used in the detector. One good alternative is the gas electron multiplier (GEM).

The GEM was introduced by Sauli (1997). It is a micro-pattern gas detector (MPGD) and consists of a thin, metal-clad polymer foil, chemically pierced by a high density of holes (typically 50 to 100 per mm^2). On application of a difference of potential between the two electrodes, electrons released by radiation in the gas on one side of the structure drift into the holes, multiply and transfer to a collection region.

Each hole in the GEM acts as an individual proportional amplifier. The multiplier can be used as a detector on its own, or as a preamplifier in a multiple structure; in this case, it permits to reach large overall gains in harsh radiation environment (SAULI, 1997; HERNÁNDEZ, 2015). The GEM structure diagram is shown in the Figure 7 (CERN, 2018).

In the GEM, most of the ions are collected rapidly in the upper side of the GEM foil and the signal induced in the pads is created by the movement of electrons between the foil and the pads. Therefore the induced signal has a negative polarity (KARLEN *et al.*, 2001; HERNÁNDEZ, 2015).

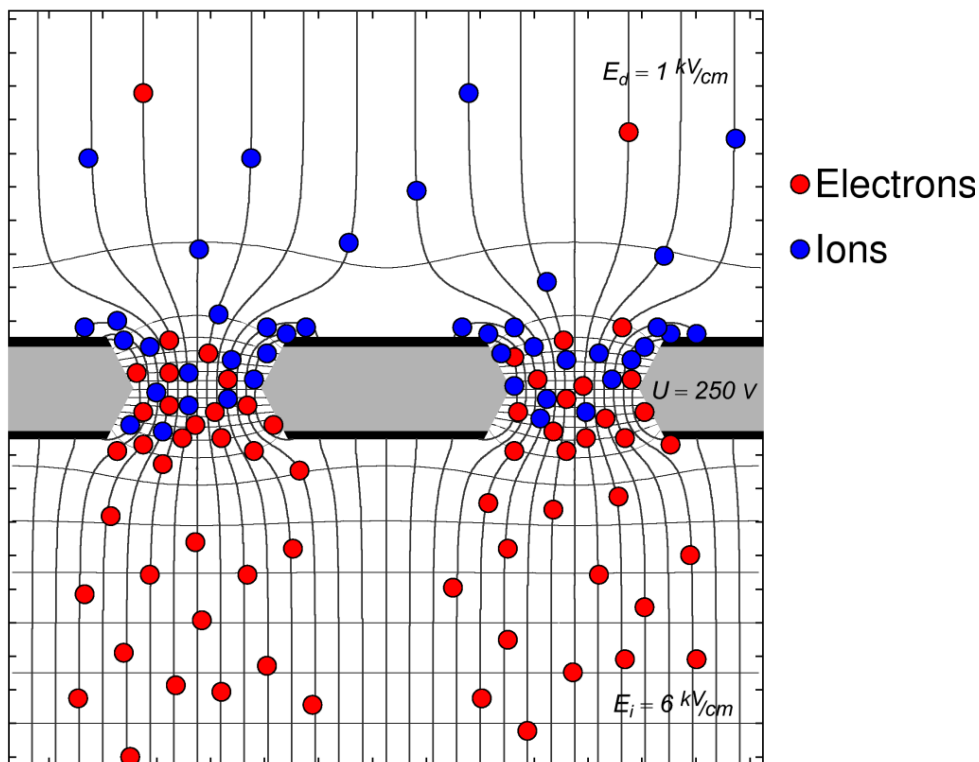


Figure 7 – GEM structure diagram.

Source: CERN (2018).

2.3 The ALICE detector update scenario

Aiming to increase the luminosity in the experiments, the management committee of the LHC accelerator approved a program of a series of updates for the ALICE detector (ALICE; APPELSHÄUSER; LIPPMANN, 2013; ALICE, 2013).

The basis of the update is the increase of read-out event rate to 50 kHz. And is still desirable to achieve improvements in the resolution and tracking efficiency maintaining the excellent particles identification ability of ALICE detector.

To accomplish with this, the present MWPC based readout chambers will need to be replaced by GEM detectors which feature intrinsic ion blocking without additional gating and exhibit excellent rate capabilities. As discussed before, the MWPC have several limitations. This implies in the replacement of the existing front-end electronics to accommodate the new GEM requirements and to provide the full flexibility of a continuous readout digital system. The existing field cage as well as most of the services of the MWPC based TPC will likely remain after the replacement to GEM.

The ALICE TPC readout was made with a pair of the PASA and ALTRO ASICs and there were several limitations in relation to this structure in the system upgrades (ALICE; APPELSHÄUSER; LIPPMANN, 2013; ALICE, 2013).

In respect to the analog front-end, the PASA shaping-amplifier usually reads signals with a positive polarity, while its dynamic range for negative polarity, as those produced by GEM detectors, is limited to about 100 times the noise, therefore is not adequate to accommodate the TPC signals (dynamic range 900:1) (ALICE; APPELSHÄUSER; LIPPMANN, 2013; ALICE, 2013; HERNÁNDEZ, 2015).

In relation to signal processing and data output, the ALTRO ASIC does not support continuous read-out. Running trigger-less, with parallel memory access in a continuous read-out mode is a requirement for the TPC upgrade (ALICE; APPELSHÄUSER; LIPPMANN, 2013; ALICE, 2013; HERNÁNDEZ, 2015).

Is also important to state that the new read-out unit requires an increasing number of channels per chip from 16 (currently used) to 32, reducing the chips per board in a ratio of 4 to just one for the equivalent task (8 to two in MCH and 20 to 5 in TPC), a relevant improvement in respect to integration and density.

2.4 The need of a new ASIC

In the context of research and development for TPC and gaseous detectors, a new chip has been developed after PASA deployment, named Super-ALTRO that overcomes the first limitation. The Super-ALTRO is a further evolution of the ALTRO chip, now

manufactured in 130 nm technology. It combines in a single silicon die the PASA and the ALTRO functionality, including more processing functions and can operate with both positive and negative polarities (ASPELL *et al.*, 2012).

The new readout system for the upgraded TPC could be built on the basis of the current TPC readout and the Super-ALTRO chip. However, a new improved version of the Super-ALTRO chip, including the support of a continuous readout scheme would be needed. In this concern, it worth mentioning that the continuous readout might become a limitation for the integration of the PASA and digital chip in the same substrate (ASPELL *et al.*, 2013; HERNÁNDEZ, 2015). Updates in drivers, output connections and digital signal processor (DSP) should also be done.

High power consumption of the ADC analog blocks and the main amplifier of PASA are also main limitations for full integration of 32 channels. The power consumption of super ALTRO is 47 mW per channel. A chip with 32 super-ALTRO channels would dissipate about 1.5 W.

This power usage complicates the integration of noise sensitive analog circuits and digital circuits, because noise coupling to sensitive analog nodes is critical (HERNÁNDEZ, 2015). The PASA chip needs 90 dB on the input of isolation considering 20 μ V of input signal amplitude and 1.5 V of voltage supply. A chip dissipating 1.5 W can also be problematic for the detector integration and cooling, as thousands of them will be running in a confined space.

The area consumption of the super-ALTRO channel is another limitation for full integration of 32 channels. In this case the area per channel is around 4 mm² and for 32 channels, the total chip area will be 128 mm² (ASPELL *et al.*, 2013; HERNÁNDEZ, 2015). For large size chips (greater than 100 mm²), the yield and the number of chips per wafer fall dramatically. The ALICE experiment needs about 1.5 million channels implemented with about 57.000 chips and this strongly affect the costs and budget for the project (HERNÁNDEZ, 2015).

To overcome these limitations, the design, fabrication and experimental test of new ASIC named SAMPa have been proposed, which can be used for signals detection in the TPC. The circuits will support both positive and negative polarities, with 32 channels per chip and continuous data readout with smaller power consumption than the previous versions. The output data rate will also be increased up to 3520 Mbps using eleven 320 Mbps differential scalable low-voltage signaling (SLVS) serial links.

The MCH is other important detector of the ALICE experiment which request a read-out electronic upgrades (ALICE; APPELSHÄUSER; LIPPMANN, 2013; ALICE, 2013). The SAMPa chip would be a common readout front-end chip for the TPC and MCH. In this way, it will reduce the implementation cost of the electronics upgrade project.

Since TPC and MCH have different specifications of detector capacitance, noise, sensitivity, peaking time, DSP, chaining and communication, the new readout front-end ASIC should be configurable for both detectors.

The MCH consist of 156 MWPC chambers with more than one million electronic channels. This MWPCs are with cathode pad readout, the so-called Cathode Pad Chambers. The system consists of 5 tracking stations, with each station being composed by 2 chambers (ANTONIOLI; KLUGE; RIEGLER, 2013). It is important to note that due to the MWPC, SAMPA also need to have selectable polarity and a configurable DSP.

The muon chambers will use 17.000 front-end boards containing two 32-channel SAMPA chips each. It is planned that the cards will be connected to 500 gigabit transceiver (GBT) read-out boards multiplexing the SAMPA serial output links of 40 front-end cards into one multi gigabit serial GBT link and forwarding the data to the common readout unit (CRU)(ANTONIOLI; KLUGE; RIEGLER, 2013).

These facts show the strong need for a new ASIC, which is a large mixed signal chip, highly configurable and never built before. Due to the extent and diversity of the tasks involved, the project was divided into two major parts. First, there is the analog front-end, composed mainly of charge sensitive amplifier (CSA), bias, voltage reference and ADC. After, there is the digital section, implementing the signal conditioning, configuration, testing, compression, storage, packaging and communication functions.

The work of HERNÁNDEZ (2015) is already a relevant achievement in the direction of the development of the ASIC, where noise and power supply rejection ratio (PSRR) improvement techniques for the front-end are discussed tested and further applied to the design of the real SAMPA front-end analog amplifier.

However, a large part of the chip is still not addressed, which mainly relates to the digital side. Also, the external acquisition system for testing the chip and carrying out irradiations to verify the project's applicability is very important.

In parallel with the described ALICE upgrade scenario, other experiments were also planning to modernize their electronic systems, such as CMS and ATLAS. In these, it was also considered the implementation of a configurable multichannel mixed signal chip with ADCs and digital signal processing that was named Gas Detector Digital Signal Processor (GdSP).

The work of Naaranoja (2014) was aligned with the GdSP project, where limitations and possible improvements to the Super-ALTRO architecture were discussed. Although, it was decided to not use direct digital analog conversion, going to a simplified approach based on time over threshold and constant fraction discriminator (CFD). This has driven the system to became very different from SAMPA not implementing digital filters of similar function due to the distinct data characteristics in this case (KUPIAINEN, 2013;

ROSA, 2017; MATVEEV, 2020; ASPELL *et al.*, 2018).

Other detectors outside CERN also needed a chip for signal acquisition and processing in a configurable way, such as the Relativistic Heavy-ion Collider (RHIC) Solenoid Tracker at Brookhaven National Laboratory (BNL) (SHEN *et al.*, 2018) and the Nuclotron-based Ion Collider Facility (NICA) at Dubna (VERESCHAGIN; MOVCHAN; ZAPOROZHETS, 2020; FATEEV *et al.*, 2019).

The SAMPA project should accommodate these needs, being a complete closed solution applicable to this kind of detector environment and the interactions there present.

In this way, the digital section of SAMPA emerged as a relevant pending structure to be achieved, which have been a common motivation for three extensive works which happened in parallel.

The work of Velure (2019) deals with system analysis, proposal of the digital block and part of its RTL development, focusing mainly on its final compression, buffering and communication structures. This work also implemented a wide part of the data acquisition system used in functional tests of SAMPA.

Mahmood (2020) is also an important contribution to the overall project, where a wide set of irradiations were done in structures developed by the present work, which the measurements were essential for the SAMPA results due to the cross-sections obtained and observations realized.

With this scenario, part of the ASIC development was still not covered, also the design methodology in several sections of the implementation should be addressed. The next chapter will describe the proposed ASIC, its main objectives and internal structures aiming to cover the cited needs.

3 SAMPA ASIC design

The project involving the SAMPA chip development started in 2013 at the Polytechnic School of the University of São Paulo and it was named as "Design of an ASIC for digital signal acquisition and processing for the ALICE experiment time projection chamber". This project was also further extended to a wider objective as the design of instrumentation electronics for high energy particle physics gaseous detector experiments.

The final main goal of the project was the development and delivery of a complex ASIC to be mass produced and installed in the CERN ALICE experiment during LHC long shutdown 2 (LS2) solving several electronic requirements for the ALICE upgrade, as discussed in the previous chapters.

The LHC run 1 had its data collection up to 2012, after that there was the long shutdown 1 in 2013 and 2014. Then LHC had the run 2 going up to 2018, being followed by the long shutdown 2 where this work is involved.

The schedule of LS2 is shown in figure 8. LS2 is the time window where the detectors can have massive electronic upgrades. The SAMPA chip schedule had to match this, including the delivery of final application ready devices by 2018-2019, therefore the project had firm deadlines. It is important to note that the insertion of SAMPA is one of the key aspects in the ALICE upgrade.

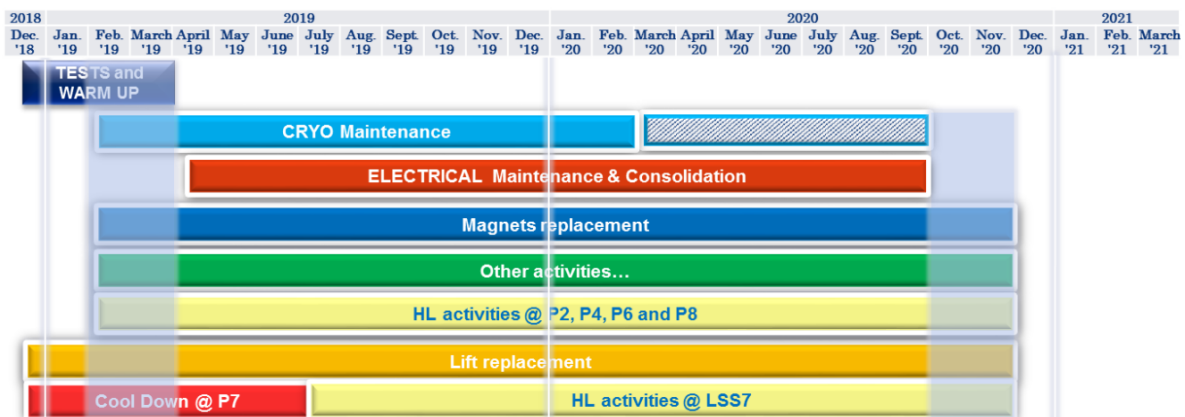


Figure 8 – LHC long shut-down 2 schedule.

Source: JIMENEZ *et al.* (2016).

In this way, the present chapter aims to briefly introduce the aspects involved in SAMPA development and after describe its internal components and structure. Both analog and digital subsections will be addressed but the digital blocks will have further extra attention due to their relevance to this work. A historical review of the SAMPA development versions will be also presented, clarifying the path used to achieve one design

of such size and complexity.

The next subsection will quickly cover the basic operation and components involved in electronic front-ends for gaseous detectors.

3.1 Readout front-ends for gaseous detectors

In the chapters 1 and 2, the motivation of SAMPA ASIC design was discussed. In this section, the architecture of a generic read-out front-end is presented and further, its electrical specifications and characteristics.

The initial element in the input chain is the detector element, which can be a MWPC or a GEM in the pad plane. This element will inject small charge variations in the chip input.

The charge signal generated on the pad plane can be modeled as a pulse current source (in the order of 1 ns) in parallel with a capacitance, which is intended to model the detector capacitance (SPIELER, 2005). As the input signal is very fast and weak it is important to notice that the electronics for direct processing of fast low amplitude signals can be very complex and expensive both in area and power.

In this way, one better solution can be the insertion of an analog pre-processing stage, before the analog-to-digital conversion and digital signal processing, composing the front-end.

The concept of analog read-out front-end will be defined as a set of blocks that makes feasible the signal flow to the digital converter starting from a direct connection between the chip and the pad-plane (HERNÁNDEZ, 2015).

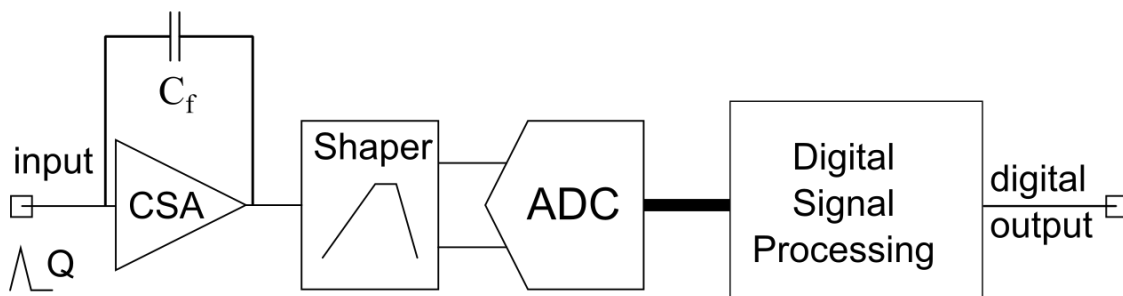


Figure 9 – Block diagram of a front-end and its readout chain.

Source: HERNÁNDEZ (2015).

A front-end for gaseous detectors is usually composed of a CSA, a Semi-Gaussian pulse shaper and at the end, a connection to the analog-to-digital converter, like a buffer

or gain amplifier. A typical block diagram of the electronic read-out system for this application is shown in figure 9.

The sensed input charge signal (Q) is conducted to the chip input and then integrated on a feedback capacitance C_f of the CSA, which produces a step voltage signal at its output with amplitude approximately equal to Q/C_f .

The step signal is fed to the shaper where a band-pass filter $H(s)$ composed by a first-order high-pass filter (differentiator) and a multiple order low pass filter (integrator).

The transfer function $H(s)$ is defined aiming the generation of a Semi-Gaussian pulse with amplitude proportional to the input charge in response to the step input signal produced on the CSA output.

After the shaper, with proper buffering and driving, the signal can be directed to the analog to digital converter, and further to the digital signal processor.

SAMPA uses an architecture very similar to the reference shown in figure 9. The block diagram in figure 10 provides a high level view of the ASIC.

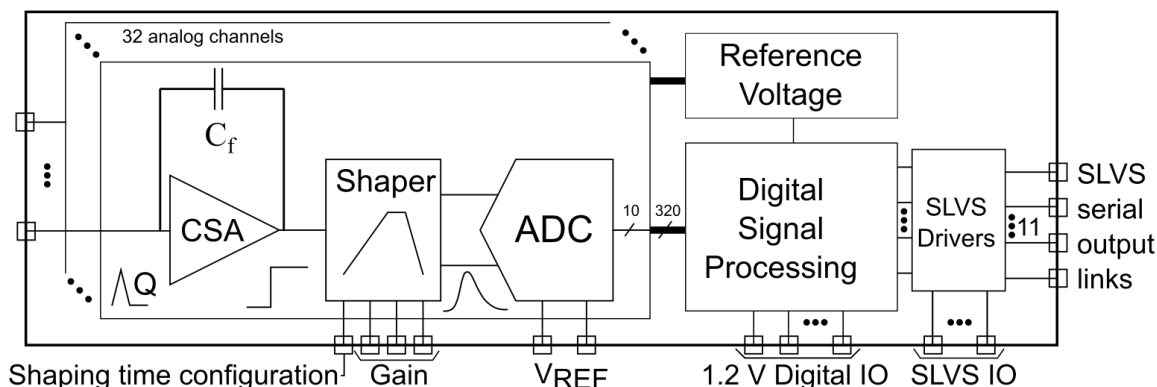


Figure 10 – SAMPA simplified block diagram with 32 channels.

Source: The author and HERNÁNDEZ (2015).

In figure 10 is possible to see that SAMPA has 32 analog front-ends with 32 ADCs sharing a common reference voltage source.

The outputs of the 32 ADCs are connected to a digital signal processing block, which is one of the greatest targets of analysis here. It includes the parallel filtering for all the channels and has as its output up to 11 high-speed digital links.

The input and output drivers used in these links are based on the scalable low-voltage signaling standard (JEDEC, 2001) and in SAMPA can work nominally up to 320 Mbps. The work HERNÁNDEZ *et al.* (2017) validates and shows the improvements implemented in these drivers.

In the next section, the description of the blocks used in SAMPA will start to take place, initiating with the charge sensitive amplifier.

3.1.1 SAMPA analog front-end

The front-end is composed of a configurable positive/negative polarity CSA with a capacitive feedback C_f and a resistive feedback R_f connected in parallel, a pole-zero cancellation (PZC) network, a high pass filter, two bridged-T second order low pass filters and a non-inverting stage, as shown in the block diagram of figure 11 (HERNÁNDEZ, 2015).

The first shaper is a scaled-down version of the CSA and generates the two first poles and one zero. A copy of the first shaper connected in unity gain configuration is implemented in order to provide a differential mode input to the next stage (HERNÁNDEZ, 2015).

The second stage of the shaper is a fully differential second-order bridged-T filter and it includes a common-mode feedback (CMFB) network (HERNÁNDEZ, 2015).

The non-inverting stage adapts the direct current (DC) voltage level of the shaper output to match the full dynamic range of the ADC. It consists of the parallel connection of two equally designed Miller compensated amplifiers (HERNÁNDEZ, 2015).

The gain, polarity and shaping time of the front-end are configurable through logic external input pins (HERNÁNDEZ *et al.*, 2020).

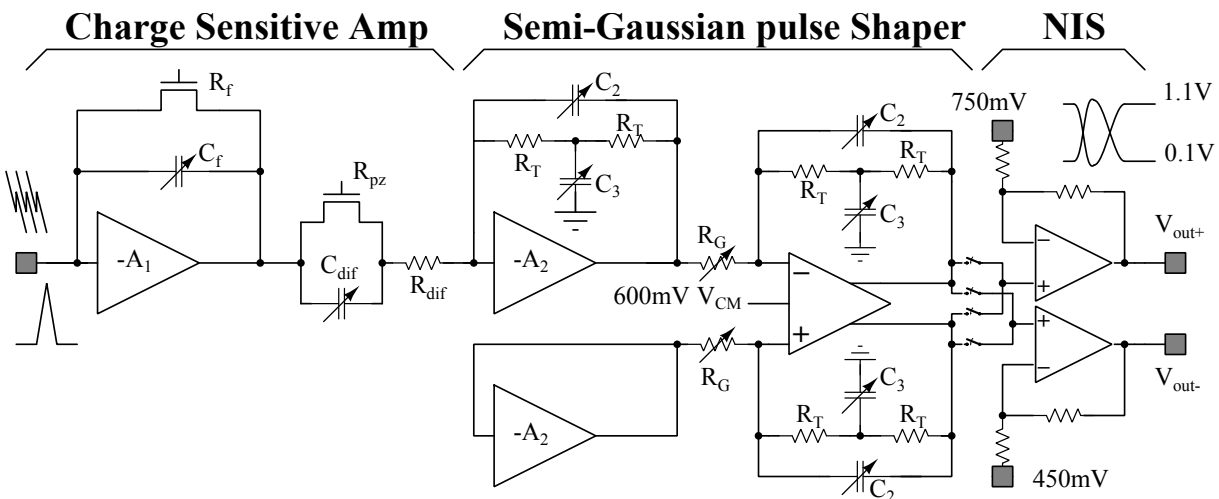


Figure 11 – Block diagram of the analog front-end.

Source: Sanches and Velure (2018), HERNÁNDEZ (2015).

3.1.2 Analog to digital converter

The ADC is based on a split capacitor fully differential SAR topology. The SAR strategy allows for low power with reasonable high sample rates and resolution for this application. The ADC has a resolution of 10-bit and a sample rate up to 20 Msamples/s.

Table 1 – Specifications of the new front-end ASIC (SAMPA)

Specification	TPC	MCH
voltage supply	1.25 V	1.25 V
polarity	Positive/Negative	Positive/Negative
detector capacitance (Cd)	18.5 pF	40 pF - 80 pF
peaking time (ts)	160 ns	300 ns
shaping order	4th	4th
equivalent noise charge (ENC)	$< 600 e@ts=160 \text{ ns}^*$	$< 950 e@Cd=40 \text{ pF}^*$ $< 1600 e@Cd=80 \text{ pF}^*$
linear Range	100 fC or 67 fC	500 fC
sensitivity	20 mV/fC or 30 mV/fC	4 mV/fC
non-linearity (CSA + Shaper)	$< 1\%$	$< 1\%$
crosstalk	$< 0.2 \%@ts=160 \text{ ns}$	$< 0.2 \%@ts=300 \text{ ns}$
ADC effective input range	2 V _{pp}	2 V _{pp}
ADC resolution (NB)	10 bits	10 bits
sampling Frequency	5/10 MSps	10 MSps
integral non-linearity (INL)	$< 0.65 \text{ LSB}$	$< 0.65 \text{ LSB}$
differential non-linearity (DNL)	$< 0.6 \text{ LSB}$	$< 0.6 \text{ LSB}$
effective number of bits (ENOB)**	$> 9.2 \text{ bits}$	$> 9.2 \text{ bits}$
CSA + Shaper + ADC		
power consumption (per channel)	$< 15 \text{ mW}$	$< 15 \text{ mW}$
channels per chip	32	32

* $R_{esd} = 70 \Omega$

** @0.5 MHz, 10 MSps

3.2 The SAMPA application specific signal processor

The SAMPA application specific signal processor is a multipurpose block involving clock generation, chip configuration, data filtering, compression, time stamp control, packet generation, buffering, multi-chip communication and data serialization. These tasks must be performed in parallel for the 32 digitized channels and after packet generation, this data should be sent out in a configurable amount of high speed serial links operating independently from the others.

The digital core and its blocks will be the main focus here and it is important to clarify that it is also widely named in high energy physics (HEP) and ALICE community as SAMPA DSP. This is an acceptable name that will continue to be used due to its development history but in the actual versions, there is no software at all running in this core.

The choice for a core without software was made targeting a system with no program counter, aiming to increase resistance to upsets. It also do not have a program memory, which would need to be hardened, using a considerable additional area. The present core is very configurable through protected register units, being possible to reuse

it in several HEP experiments, with different demands in respect to filtering, processing and data rate.

This session will describe the architecture and building blocks of the digital core detailing its main characteristics and general functions. The figure 14 shows the simplified block diagram of the digital block. The graph also shows the SAMPA main clock domains and the most relevant operational frequency of each block using a color legend.

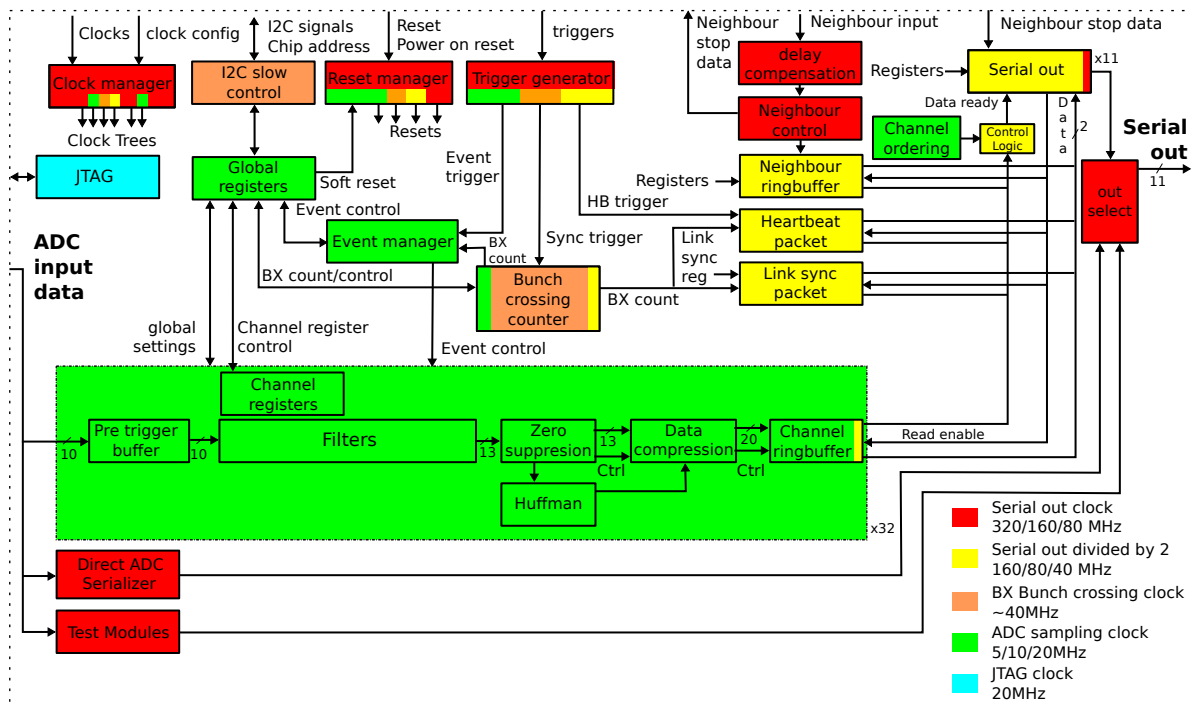


Figure 14 – SAMPA application specific signal processor simplified block diagram.

Source: Sanches and Noiye (2021).

Some of the cited frequencies are derived from others, including the serial output clock division by two, that is extensively used in the buffering to output section. SAMPA can supply all the necessary clocks just using one single serialization clock input if needed. Thus, the reference maximum input clock is 320 MHz.

It is also relevant to mention that majority of the blocks in SAMPA are connected to the clock trees in the presented way to save power. The processing is made in a continuous pipeline flow and most of the enabled sections work in a steady operational fashion, where the involved blocks are fed just with the minimum needed clock frequency, not wasting power.

The description of the chip operation can be started by the ADC data bus, from where the data is initially registered and sent to 3 main possible paths. The first is the standard mode (the packet based mode), which directs the input to the pre-trigger buffer that starts the processing pipeline.

The second option is the usage of direct ADC data serialization to the SLVS

outputs (HERNÁNDEZ *et al.*, 2020; SANCHES; VELURE, 2018). The third option is a set of debug and test features to get direct access to these internal pins from outside of the chip, depending on the configuration used (SANCHES; VELURE, 2018). The direct serialization module and the test modes are simpler functions and focusing on the most interesting and complex scenario, the packet based mode will be mainly addressed.

3.2.1 Pre-trigger buffer

The SAMPA chip can also be used with an externally provided trigger signal; in this scenario it is often needed to compensate the delay between the triggering event and the reception of the trigger signal on the device.

This compensation is done by delaying and storing the incoming data by a similar amount of time as the trigger signal was delayed. If one also wants to look at data before the triggering event, it is viable to add more delay. It is possible to store the data by up to 192 ADC conversion cycles, corresponding in time to 9.6 μ s, 19.2 μ s and 38.4 μ s respectively at sample clocks of 20 MHz, 10 MHz and 5 MHz (SANCHES; VELURE, 2018).

The pre-trigger buffer module uses a 10x192 bit dual port SRAM to provide a programmable delay chain for the samples, permitting the chip to accommodate a wide range of delay values in the trigger signal.

The delay can be externally defined in run-time through inter-integrated circuit (I2C) bus programmable chip register *PRETRG*, with a maximum delay of 192 samples (SANCHES; VELURE, 2018).

The top left circuit in figure 15 normalizes this programmable delay so it can be used for addressing the memory. The upper limit for the normalized value is set by the size of the memory and the lower one is dependent on restriction in the memory core. It is not possible to read and write to the same memory address so the minimum distance between the read and write pointer needs to be one, which due to intrinsic delay in the memory gives a delay of 2 so one delay needs to be subtracted from the programmable delay value when the memory is used for delaying.

The top right circuit in figure 15 generates the write pointer. It increments on each clock cycle and rolls over at the maximum address of 191.

The middle left circuit in the figure 15 calculates the current read pointer from the write pointer. The read pointer is calculated by subtracting the programmable delay value from the current write pointer.

The bottom circuit in the figure 15 shows the main data path of the module. If the programmable delay is set to zero, the data from the input is passed directly to the output. If the value is one, it is passed through a single word register due to the memory

being unable to read and write at the same address.

When the programmable delay is larger than one, the data is passed through the implemented memory circular buffer (SANCHES; VELURE, 2018). If the memory is not in use or the channel has been turned off, the memory is also disabled, saving power.

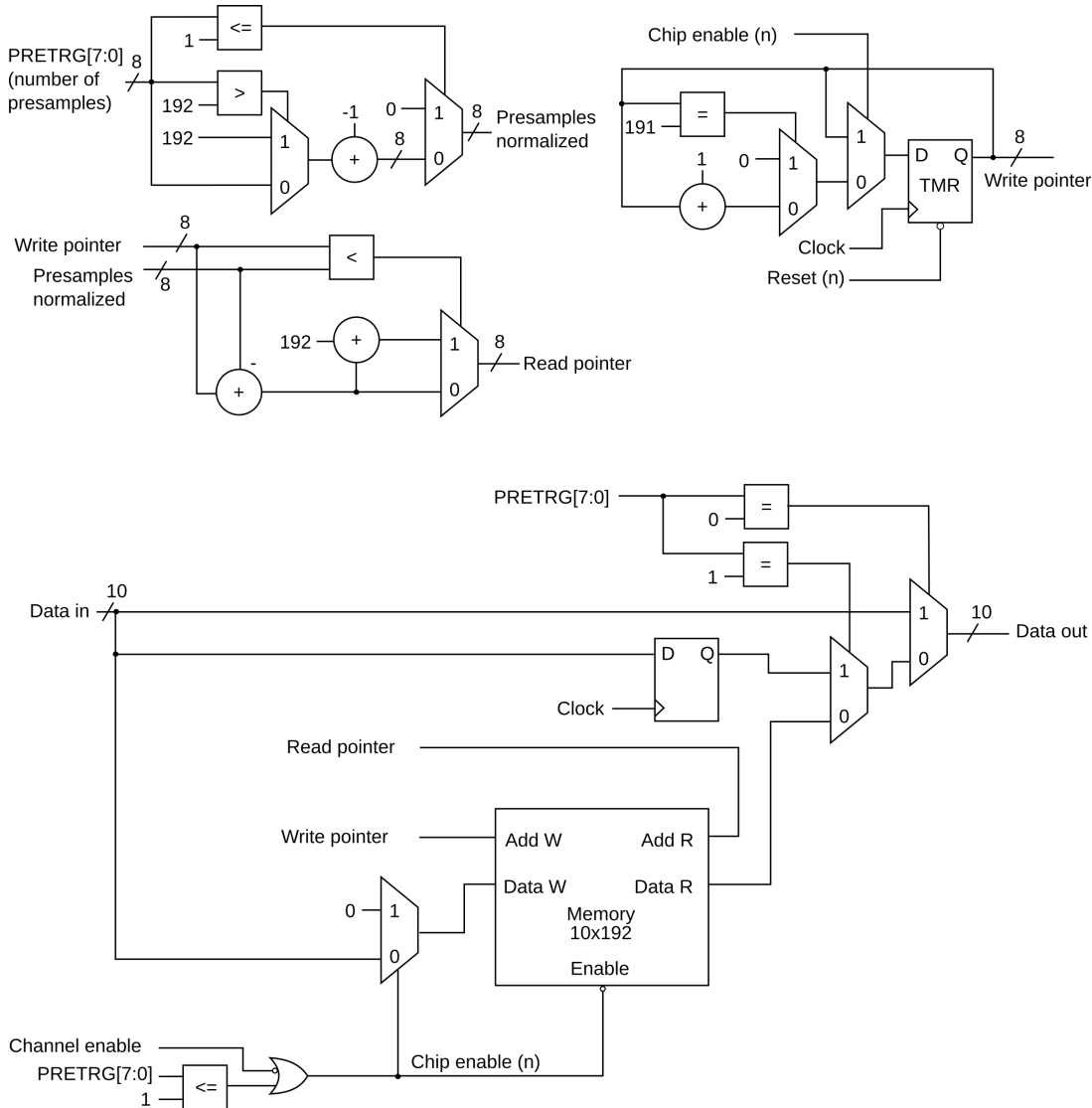


Figure 15 – Pre-trigger buffer schematic.

Source: Sanches and Velure (2018).

The delayed data output is then fed to the filters block that contains the set of per channel filters available on the ASIC. The description of this complex block will be the target of the next section.

3.2.2 Filters

The filters module is responsible for concatenating and interconnecting the different elements actuating in the digital signal conditioning in the SAMPA. The figure 16 provides a block diagram of this module, showing its internal components.

The baseline is not exactly a fixed level and shows dependence with several operational conditions and also to process variations, but after the chip enters in steady operation, out of the real experiment, this level is practically maintained, varying mostly due to changes in voltage, temperature and due to the inputs itself.

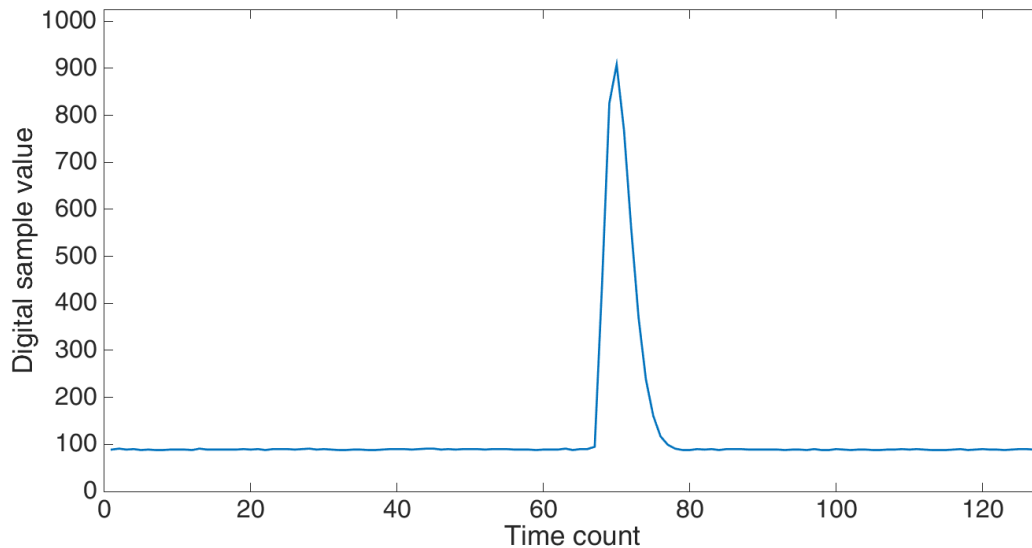


Figure 17 – A single input pulse captured at 160 ns shaping time and 20 mV/fC gain. The discrete time scale is in steps of 100 ns, referring to a 10 MSps conversion.

Figure 17 shows a typical input pulse of 80% of the dynamic range collected at 160 ns shaping time and 20 mV/fC gain configuration. This pulse sits over a baseline of around 88, which is around 8.6% of the maximum acceptable input value. The unit of the graph is unsigned ADC least significant bits (LSBs) varying between 0 and 1023.

It is possible to observe that the baseline is stable and just a small noise contribution causes some fluctuations around its average value. In this case, it is easy to decide where there is a pulse or not, permitting the direct application of a fixed threshold level to zero suppress the data out of the pulse region.

Unfortunately, due to several effects in the real detector (MÜNNING *et al.*, 2016; APPELSHAEUSER *et al.*, 2016), the baseline can fluctuate in several manners during the acquisition. Figure 18 shows an example of a full 1k sample time window from the work MÜNNING *et al.* (2016) where the common mode effect baseline shift on GEM based detectors is addressed.

In figure 18, it is possible to observe dozens of pulses along with a baseline with medium fluctuations. The amplitude of the changes can easily mask a considerable part of the smaller pulses, or on the other hand, may deeply degrade the compression efficiency of ZSU (HERNÁNDEZ *et al.*, 2020; SANCHES; VELURE, 2018; BREGANT *et al.*, 2017). These facts motivate the research and insertion of baseline correction filters in the digital

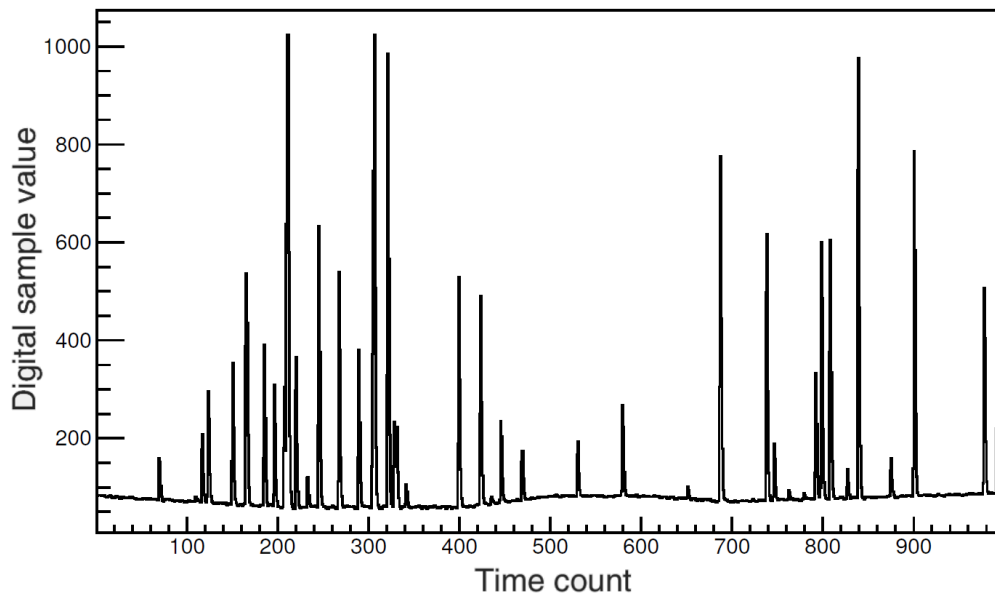


Figure 18 – Illustration of one time window with several pulses.

Source: MÜNNING *et al.* (2016).

signal processor. The next section starts with the first filter in the data path.

3.2.4 The BC1 filter

There are several kinds of perturbations that can affect the baseline in a gaseous detector system. One possible and common class of perturbation causes slow variations, affecting up to hundreds of samples due to its low frequency (up to 1 kHz). Multiple phenomena can contribute to these variations including artifacts created by systematic effects, like those related to triggering of the detector, drifts in temperature or voltage and also by environmental differences (due to the distinct chip locations in the experiment).

These effects should be attenuated and because of that, the BC1 filter was proposed, providing several resources to remove these slower fluctuations. The filter is an inheritance of the work Garcia (2012) and has been improved in relation to its data-path, available options and internal filtering protection.

The BC1 filter uses three main strategies to operate on the input signal, the first and simplest is the fixed pedestal (FPD) subtraction, which basically moves the signal by a known I2C configurable constant.

The second strategy is based on a look-up table named pedestal memory (PM), this is a SRAM IP with 1024 addresses of 10 bits words (ARM, 2020). The memory allows the implementation of any function of the time $f(t)$ in an acquisition window, permitting the subtraction of known systematic effects of the detector, these can be measured in run time in windows without pulses. The pedestal memory can also be used to remap the

input values to programmed values $f(D_{in})$ in a look-up fashion, permitting the correction of non-linearity and other effects.

The third BC1 strategy is named variable pedestal (VPD) subtraction, this uses an IIR digital filter to auto-calibrate the baseline and perform the removal, the VPD filter will be addressed in the next section with more details.

BC1 can join the efforts of the three different cancellation methods, generating rich data-path alternatives which can solve a wide range of problems. The BC1 operation is configured through the I2C register DPCFG[3:0] and provides the combined options listed in table 2 (SANCHES; VELURE, 2018).

Table 2 – Main operational modes of the first baseline correction filter

Configuration (DPCFG[3:0])	Data-path operation
0x0	$D_{in} - \text{FPD}$
0x1	$D_{in} - f(t)$
0x2	$D_{in} - f(D_{in})$
0x3	$D_{in} - f(D_{in} - \text{VPD})$
0x4	$D_{in} - \text{VPD} - \text{FPD}$
0x5	$D_{in} - \text{VPD} - f(t)$
0x6	$D_{in} - \text{VPD} - f(D_{in})$
0x7	$D_{in} - \text{VPD} - f(D_{in} - \text{VPD})$
0x8	$f(D_{in}) - \text{FPD}$
0x9	$f(D_{in} - \text{VPD}) - \text{FPD}$
0xA	$f(t) - \text{FPD}$

In table 2, D_{in} is the input data and the look-up function $f(\bullet)$ is the output of the pedestal memory inserting the argument (\bullet) as the address (ARM, 2020; SANCHES; VELURE, 2018). Per example, the configuration 0 would perform the simplest filter operation, the constant subtraction from the input data. Configuration 5 on the other hand will perform time variant subtraction over the input data minus the auto calibrated IIR variable pedestal. This targets reductions in both systematic errors and slow random variations.

The simplified filter block diagram is presented in figure 19. The top part of the diagram shows the implementation of the options presented in table 2. The pedestal memory is shown at the bottom and the IIR filter at the right side. The next section will cover the VPD IIR filter.

3.2.4.1 The VPD filter

The variable pedestal is an infinite impulse response digital filter targeted to filter the high frequency components of the signal, obtaining only the baseline and slow variation signals in the output named as VPD.

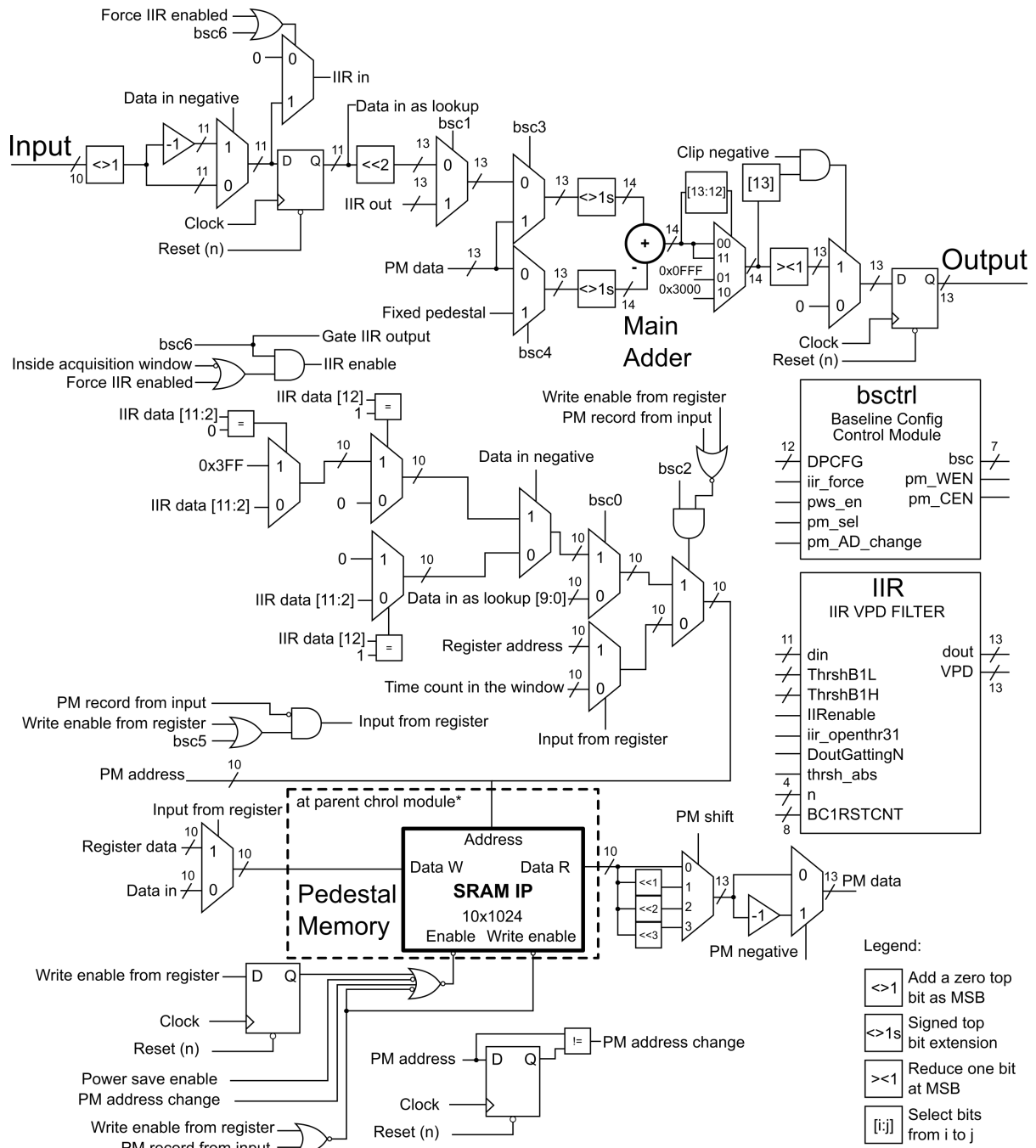


Figure 19 – Block diagram of BC1 top level.

Source: The author (SANCHES; VELURE, 2018).

Having the VPD, it is possible to obtain the output signal D_{out} by subtracting the VPD from the input D_{in} , as shown in equation 3.1:

$$D_{out} = D_{in} - VPD. \quad (3.1)$$

The VPD is calculated using a compact and resource friendly strategy based on an accumulator and a single sample register for the delay in the feedback loop (GARCIA, 2012). Figure 20 illustrate the simplified schematic block diagram.

In the diagram, it is clearly possible to see the output being calculated from the subtraction of VPD. The VPD is further calculated with the weighted sum of the $dout_{next}$ deltas in the accumulator variable named as Sum .

On the other hand, it is quite difficult to understand the filter behavior from the feedback schematic as is an IIR filter. To better analyze this loop, the VPD transfer function $G(z)$ was calculated and is presented in equation 3.2. In this equation, the number of taps exponent was denoted as N and it is relevant to note that the factors 2^{-N} could be implemented easily by right shifts.

$$G(z) = \frac{2^{-N}z^{-1}}{1 - (1 - 2^{-N})z^{-1}} \quad (3.2)$$

Equation 3.2 numerator shows a weighted delayed signal and in the denominator, the low pass behavior is notable by the pole $(1 - 2^{-N})$.

The transfer function is controlled by N and with bigger values, the response will be slower, corresponding to a longer time influence on the output signal. SAMPA implements this filter with configurable N up to 15, as an improvement of ALTRO ($N = 1$) and Super-ALTRO ($N \leq 7$) (BOSCH *et al.*, 2003; GARCIA, 2012).

For the reader convenience, the filter output transfer function was also obtained and shown as $H(z)$ in equation 3.3, where N is the number of taps.

$$H(z) = \frac{1 - z^{-1}}{1 - (1 - 2^{-N})z^{-1}} \quad (3.3)$$

The VPD filter may operate continuously, but in the real experiment the input data is not just the baseline, containing also pulses. The pulses can elevate the baseline estimation, especially the bigger ones.

One alternative to this question is to use thresholds and just run the VPD calculation when the signal is in a specific configured range.

The BC1 implementation contains 2 options, absolute and relative thresholds. The relative thresholds are set around the last obtained baseline, while the absolute are in

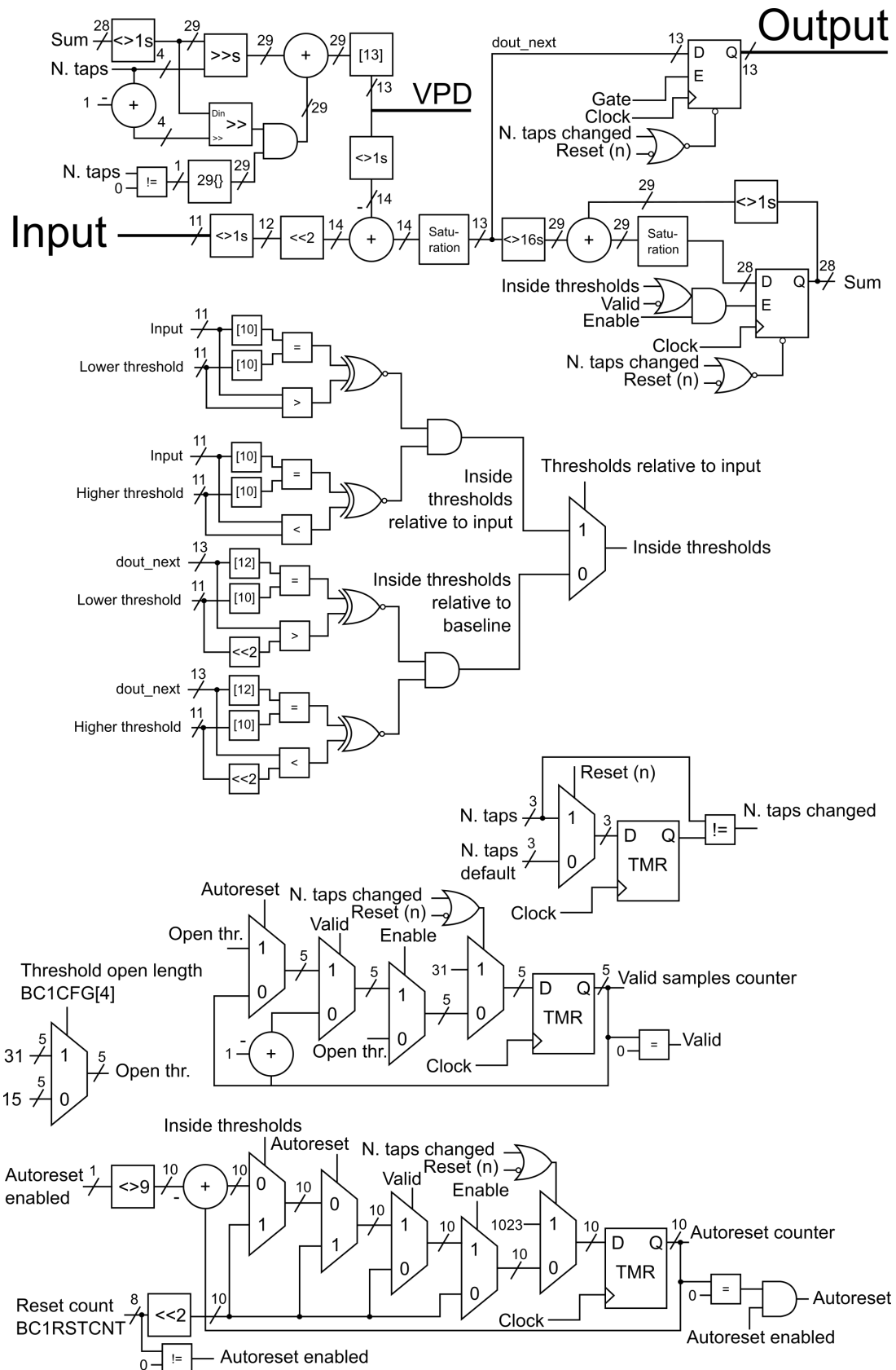


Figure 20 – BC1 internal IIR variable pedestal filter block diagram.

Source: The author (SANCHES; VELURE, 2018).

relation to zero. These options are implemented in the tree of comparators at the middle of figure 20, which culminate to control the *Sum* register enable signal.

Some detectors present slow variation tails in the pulses that can not be addressed by BC1; the next section addresses one alternative to cope with that, the IIR digital shaper.

3.2.5 The digital shaper

Changes in the converted pulse shape can be prejudicial for the system, especially in the case of slow decaying tails and undershoots. A deep variation after a pulse can distort the values measured of a closer pulse. Similar artifacts can also happen in the presence of long tails, but in this case the new pulse could happen over the tail of the last one. This would virtually increase its amplitude, implying in erroneous results (GARCIA, 2012).

A possible solution to this problem can be achieved with the inclusion of a set of IIR filters with adequate calculated coefficients aiming to digitally reshape the pulses (BOSCH *et al.*, 2003).

The work Bosch *et al.* (2003) proposed the use of three single order direct form II filters IIR sections in series to implement this block. This was optimized in Garcia (2012) where the implementation was changed to a 4th order filter with the transposed direct form II architecture, which introduces less noise to the system.

SAMPA also uses the last architecture due to the fact that the zeros effectively precede the poles in series order. This helps in the case of the poles give a large gain at some frequencies, and the zeros often provide compensating attenuation. This is especially true for filters with sharp transitions in their frequency response; the sharp transitions are achieved using near pole-zero cancellations close to the unit circle in the z .

SAMPA has also a big improvement concerning the general usage of this filter, where the last two sections gained one extra multiplier coefficient and a morphing capacity to second order section (SOS). With the SOS several standard filters can be better implemented which could expand the use of this block to low pass, band pass and other useful filters.

The equation 3.4 shows the transfer function of the filter in case of the standard mode, while equation 3.5 contains the SOS implementation. It is possible to clearly see the difference between them in the last polynomial, containing the terms with z^{-2} . Also, there is the signed coefficient multiplier (SCM), a Boolean configurable option controlling the coefficient resolution.

$$\left\{ \begin{array}{l} H(z) = \frac{1-L_1z^{-1}}{1-K_1z^{-1}} \cdot \frac{1-L_2z^{-1}}{1-K_2z^{-1}} \cdot \frac{L_{30}-L_3z^{-1}}{1-K_3z^{-1}} \cdot \frac{1-L_4z^{-1}}{1-K_4z^{-1}} \\ \left\{ \begin{array}{l} \forall 0 \leq K_i, L_i < 1 \quad \text{if } SCM = 0 \\ \forall -1 \leq K_i, L_i < 1 \quad \text{if } SCM = 1 \end{array} \right. \end{array} \right. \quad (3.4)$$

$$\left\{ \begin{array}{l} H(z) = \frac{1-L_1z^{-1}}{1-K_1z^{-1}} \cdot \frac{1-L_2z^{-1}}{1-K_2z^{-1}} \cdot \frac{L_{30}+L_3z^{-1}+K_4z^{-2}}{1+K_3z^{-1}+L_4z^{-2}} \\ \left\{ \begin{array}{l} \forall 0 \leq K_i, L_i < 1 \quad \text{if } SCM = 0 \\ \forall -1 \leq K_i, L_i < 1 \quad \text{if } SCM = 1 \end{array} \right. \end{array} \right. \quad (3.5)$$

Where L_i , K_i and L_{30} represents the per channel filter coefficients, all with 13 bit resolution (fixed point between 0 and 1). SAMPA also includes a new functionality which accepts coefficients of signed values using also 13 bits (two's complement between -1 and 1). This new option is activated with the SCM configurable input and the options are shown as $SCM = 0$ and $SCM = 1$ in transfer functions of equation 3.4 and 3.5. The implementation of the SCM mode has empowered the filter to implement generic transfer functions expanding the horizons of this block further than just tail cancellation.

Figure 21 shows the digital shaper simplified block diagram focusing on the differences between the SOS mode active or not. When inactive, the filter reduces itself to four first order IIR units.

It is also possible to observe the strong similarity between the components used in the second order section and in the last two first order pairs. This fact motivated one optimization made in SAMPA, where this last second order option was implemented with reuse of the existing components.

The strategy used to do the conversion is shown in figure 22. This implementation considerably expands the filter capabilities with the cost of a few multiplexers. All the existing multipliers and adders were reused permitting the improved device to be fit in the SAMPA area.

Figure 22 focus on the last part of the digital shaper, the second order section. The signal $SOS = 1$ activates the conversion to second order and the SCM option is also shown, where it mainly affects the operation of the multipliers inputs to accept signed coefficients.

The next section addresses the FIR baseline correction filter.

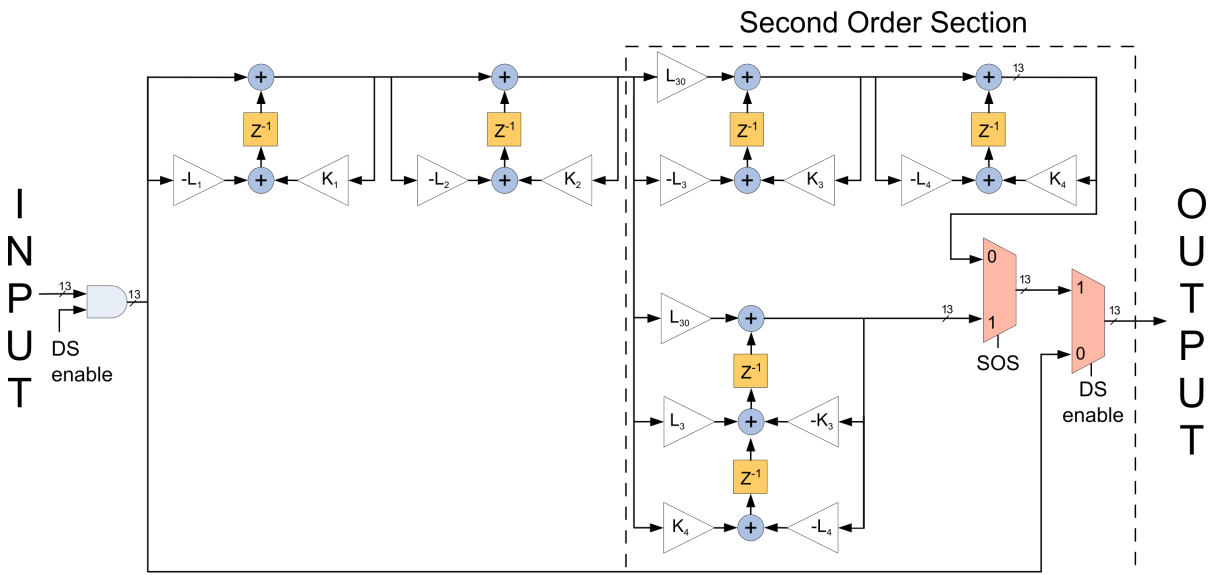


Figure 21 – Digital shaper simplified block diagram.

Source: The author. Extended from Garcia (2012).

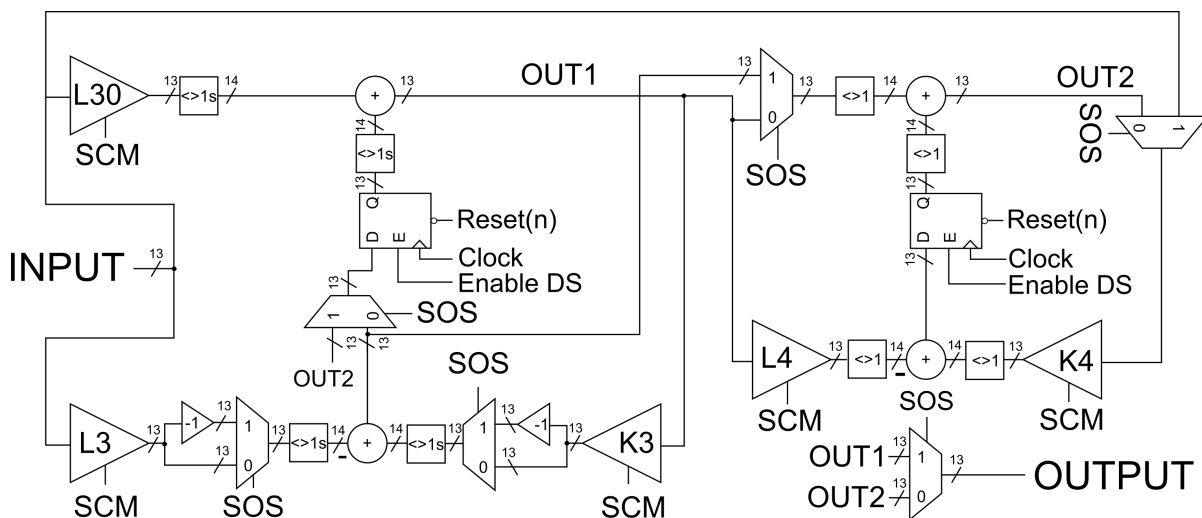


Figure 22 – Implementation of the second order section.

Source: The author (SANCHES; VELURE, 2018).

3.2.6 The BC2 filter

Fast and non-systematic fluctuations can affect the signal and change its baseline. These variations can affect and reduce the efficiency of the compression, possibly causing data loss. In this scenario, a secondary baseline filtering can be beneficial.

An alternative, in this case, is to perform a quick estimation of the baseline in the moments without pulses and then subtract it from the main input signal. To cope with that, a low-pass FIR filter can be applied, but only enabled in the adequate samples out of the signal pulses. To perform this enable decision, threshold ranges can be used.

The diagram in figure 23 shows the top level of the BC2 filter. Its central block is a moving average FIR filter, that is commanded by the filter control block, which determines if the sample is valid or not basing on pre-samples, post-samples and a set of programmable thresholds (SANCHES; NOIJE, 2020; ADOLFSSON *et al.*, 2017; GARCIA, 2012; BOSCH *et al.*, 2003).

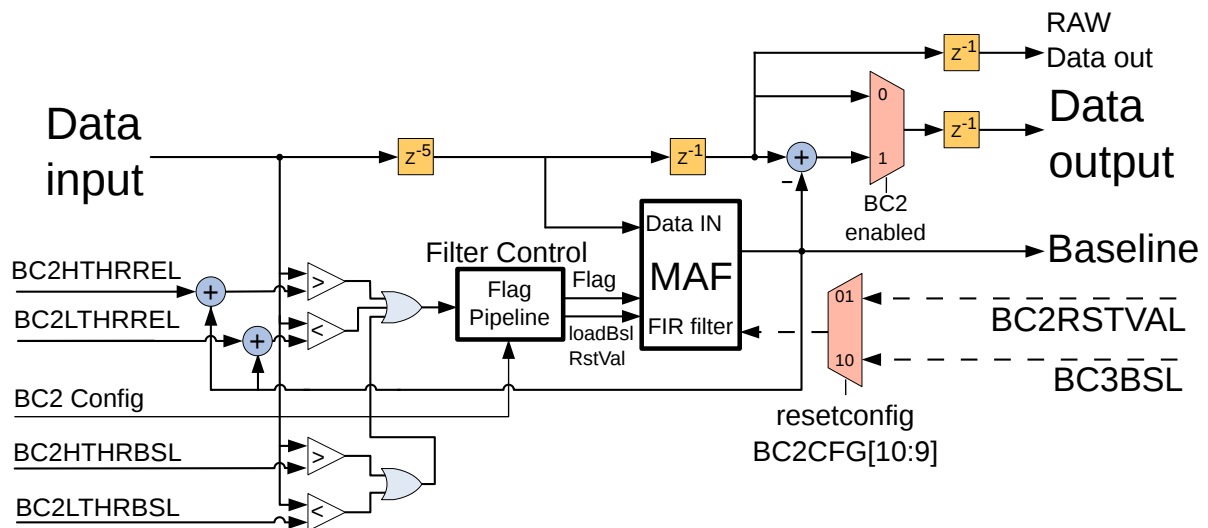


Figure 23 – The FIR baseline correction filter main block diagram.

Source: The author (SANCHES; VELURE, 2018).

There is a set of four thresholds, each pair limiting the edges of a range. The first pair perform absolute value comparison and the second works in a relative manner, including the last estimated baseline to translate the defined threshold range around the average.

The thresholds prevent changes in the calculated baseline due to the arrival of signal pulses. This scheme removes non-systematic perturbations of the baseline that are superimposed on the signal. At the output of this filter block, the signal baseline should be stable with an accuracy of one least significant bit.

The obtained baseline is then subtracted from the delayed data (to match the filter pipeline delay) providing as data output a signal, ideally just with the charge pulses

received in the input, which are ready for compression.

The proposed filter is an improvement of the previous work by Garcia (2012). That design had no BC3, and showed problems due to baseline being lock outside the calculation thresholds after fast variations and specific biased fluctuations, which moves the average to out of the range (NAARANOJA, 2014; BOSCH *et al.*, 2003). These phenomena interrupt the moving average filter update, needing special care in threshold selection, which leads to bad artifacts and tight trade-offs in the filter parameters.

The first contribution of this modified version targeting the solution of these problems is the insertion of a feedback loop between the last two baseline correction filters, where the baseline obtained by another filter can be used for restoring the baseline of BC2 to the operational range. The incoming data for this option is shown in the block diagram controlled by the BC2CFG register providing the BC3 estimated value (BC3BSL) to the BC2 core filter.

Another two options have also been inserted, focusing on the filter be independent of other blocks, one based on a previously configured reset value for the baseline, which needs to be selected by the user. This selection is not so straightforward as the expected values can change in run-time due to common-mode effects.

Due to the above difficulties, the BC2 filter received a last option, now based on self-estimation for the baseline in case it gets locked out of its calculation relative thresholds. This filter includes one programmable watchdog which evaluates if it is on track of the signal or not. If locked out of the expected configuration longer than a configurable period of time, the filter activates the auto-reset procedure. This auto-reset is not actually a reset but an automatic run-time re-estimation of the filter operation point basing on the same FIR filter structure already available, obtaining a solution with a small increase of power and area.

3.2.6.1 The MAF filter

The core of the baseline correction block in question is an FIR implementing a moving average filter (MAF) commanded by the obtained flags from the filter control block.

Figure 24 provides a schematic of the MAF data path with emphasis on its output, which is the estimated signal baseline. The diagram also shows the extra multiplexer (MUX) options at the top to implement the baseline restore feedback from *BC3BSL* and *BC2RSTVAL* where the bottom right MUX provides the source selection defining the *Baseline reset value*. The watchdog based auto estimation is implemented reusing the flag *Outside threshold* shown at the top left (SANCHES; NOIJE, 2020).

The filter was optimized to reduce the number of adders and to the complete

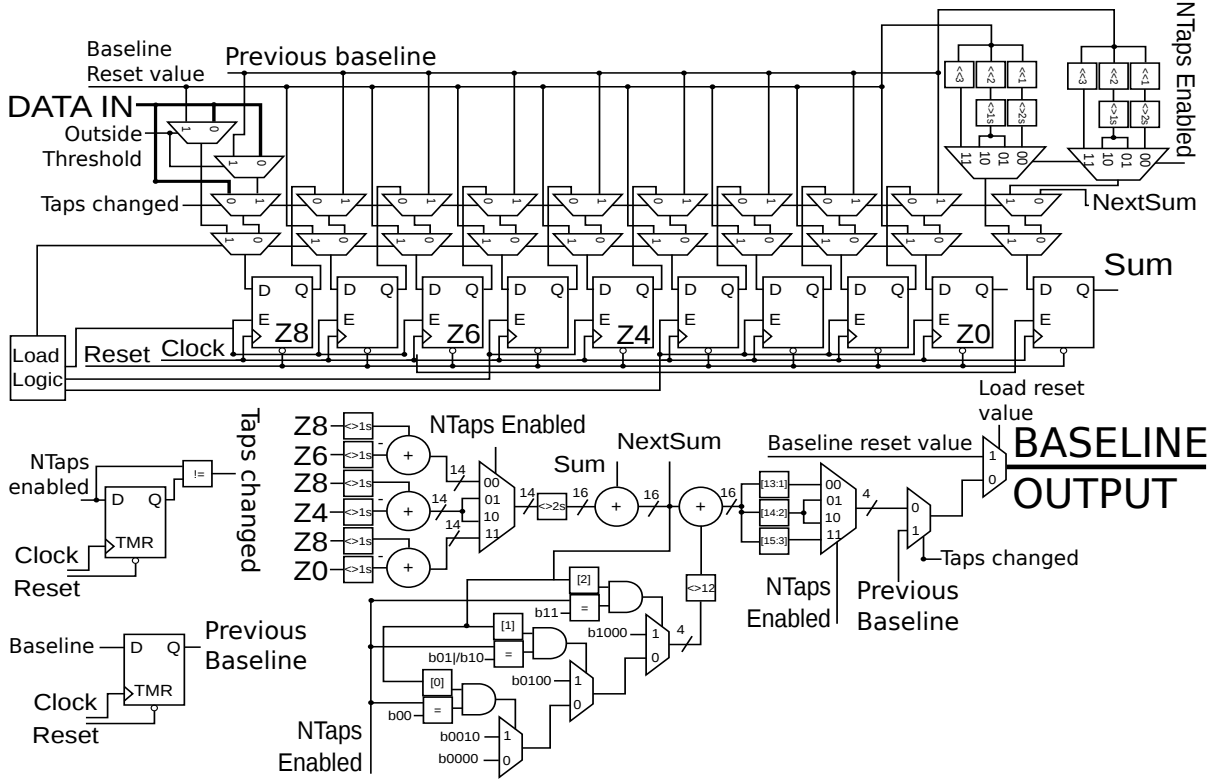


Figure 24 – The baseline correction MAF block schematic.

Source: The author (SANCHES; VELURE, 2018).

removal of multipliers/dividers. This was possible by restricting the filter total number of taps M to a power of two. Figure 24 shows a filter diagram for configurable lengths from 2 to eight (ADOLFSSON *et al.*, 2017; HERNÁNDEZ *et al.*, 2020).

$$H(z) = \frac{1}{M} \frac{(1 - z^{-M})}{(1 - z^{-1})} \quad (3.6)$$

The idea behind the cited data-path reduction is the calculation of the moving average transfer function (3.6) using just two adders as described by (3.7) for the accumulator variable Sum (RIBEIRO *et al.*, 2013; HERNÁNDEZ *et al.*, 2020).

$$Sum(z) = x + z^{-1}Sum - xz^{-M} \quad (3.7)$$

Where x is the input and M is the number of taps in the filter. The variable Sum is proportional to the desired baseline value; to obtain the final value it must be divided by the number of taps. In this case, as M is a power of two, this last division was performed with very low cost using right shifts.

The filter operates by updating the estimation of the baseline with the last acquired value and removing the value of an old sample determined by the filter length. In this way, to implement this filter, a data delay line is needed and with *length* M as its size. On the

other hand, this implementation is very economic and avoids the use of extra $(M - 2)$ adders to perform the average, saving power and area.

Finally, it is important to describe the watchdog behavior which is implemented as a 10 bit down counter. Each time the input signal enters in the configured threshold ranges, it causes the counter to be reload with an I2C programmable value. If the filter lost track of the input, the counter will decrement, eventually going down to zero.

If the watchdog counter achieves zero, one of the three available watchdog actions is performed. The first is the reload of filter baseline from a I2C register, the second is the auto-re-estimation using the own BC2 MAF and the last one is the usage of the BC3 filter obtained baseline level.

The next section addresses the operation of the new nonlinear BC3 filter implemented in SAMPA.

3.2.7 The BC3 filter

Conventional linear filters like the BC1 and BC2 have been used in the past at particle detector experiments and are useful for the task (GARCIA, 2012; NAARANOJA, 2014; ALME *et al.*, 2010), but in some exceptional cases they can end up under a failure mode where the baseline of the signal shifts to outside the thresholds of the filter and the filter stops to operate (NAARANOJA, 2014). In general, the filter has a maximum slope that can be handled before it needs to be reconfigured and the thresholds changed.

A new nonlinear filter named BC3 has been included in SAMPA using an architecture that does not need to have any thresholds. This makes the baseline tracking free of dead areas and also reduces the need for fine-tuning of configurations (MÜNNING, 2015a; MÜNNING, 2015b; MÜNNING *et al.*, 2016)¹.

The main idea behind this filter is to always follow the baseline, but with a limited slope configurable per channel. The slope parameter can be set individually for the up and down slope on a per channel basis by I2C.

Equation 3.8 shows the output signal $h(t)$, which can be expressed as a function of the input $x(t)$ and the tracked slope baseline value $g(t)$:

$$h(t) = x(t) - g(t). \quad (3.8)$$

The baseline $g(t)$ is obtained updating an initial estimation of equation 3.9a using increments or decrements as described in equation 3.9b. The values $BC3SLU$ and $BC3SLD$ are configurable and determine respectively the step of the filter tracking in up and down directions.

¹ Thanks to Konstantin Münnig for the excellent ideas, contributions and simulations about this filter.

$$g(0) = x(0) \quad (\text{arbitrary}) \quad (3.9a)$$

$$g(t) = g(t-1) + \begin{cases} BC3SLU \uparrow & \text{if } x(t) > g(t-1) \\ 0 & \text{if } x(t) = g(t-1) \\ -BC3SDL \downarrow & \text{if } x(t) < g(t-1) \end{cases} \quad (3.9b)$$

These filter coefficients also constrain a maximal slope for BC3 (as BC2 had), but $x(t)$ exceeding it causes only a time-limited deviation. As the filter does not have acceptance thresholds it also does not stay constant during an input pulse so the output pulse will be slightly affected and soon the filter will be full in track again.

Figure 25 illustrates the standard behavior of the filter when changes of the baseline and different input pulses are applied (SANCHES; VELURE, 2018).

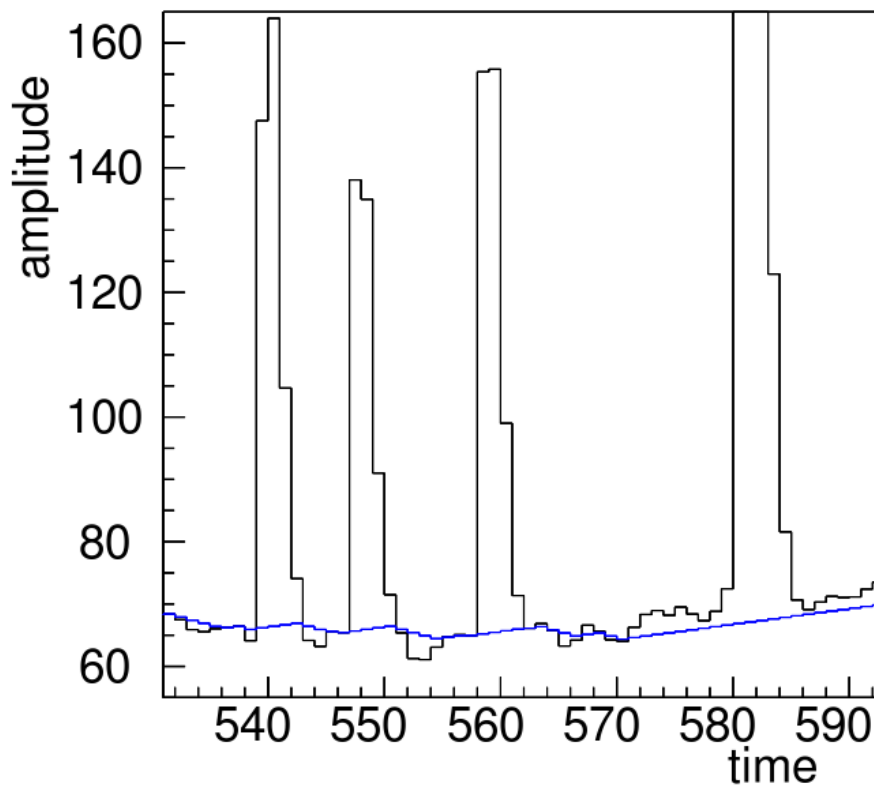


Figure 25 – BC3 filter signals.

Source: Sanches and Velure (2018).

In addition, it is important to note that the BC3 filter is very simple and resource-friendly for digital hardware implementation, which permitted its inclusion in the already very area constrained SAMPA. The novel BC3 presents an average area reduction of 55% in comparison to a filter of similar application like BC2 (GARCIA, 2012; SANCHES; NOIJE, 2021).

3.2.8 Compression

The amount of data generated in the 32 channels, running continuously in parallel, is very high and the receivers may not have enough bandwidth to accommodate this.

SAMPA implements three compression modes trying to reduce this data rate. The first and most classical is the zero suppression controlled by a threshold (HERNÁNDEZ *et al.*, 2020; GARCIA, 2012).

The zero suppression scheme just sends the data that hits a specified threshold level named *ZSTHR*. The data sections over the threshold will be named as clusters and these signal slices can also be extended by receiving additional samples around the events. SAMPA permits the inclusion of up to three pre-samples and a range from zero to seven post event samples (SANCHES; VELURE, 2018; HERNÁNDEZ *et al.*, 2020).

SAMPA also includes a filter for glitches by a minimum event length configuration. This avoids the triggering by single noise peaks generating useless clusters. SAMPA can also merge clusters near its neighbors (SANCHES; VELURE, 2018).

When running in zero suppression mode, SAMPA will remove all data between the detected clusters, saving bandwidth. With this removal, there is a need to insert in each cluster two additional variables, the first is the timestamp of the event, enabling the receiver to reconstruct the data positioning. The second variable is the cluster size, which is written to permit the receiver to find the next cluster.

The zero suppression is a powerful lossy compression scheme that can strongly reduce the data rate, depending on the inputs, previous filtering and its configurations. SAMPA also have a new secondary compression mode capable of reducing the bandwidth, this was named as cluster sum.

In the cluster sum strategy, SAMPA detects the cluster in a similar way to the zero suppression, but now it does not send the full data of the event. SAMPA calculates the sum of the samples with 20 bit resolution and sends just this 20 bits, together with the event length and time stamp. This clearly reduces the cluster data with respect of the standard zero suppression.

SAMPA also includes a loss-less compression scheme based on a look-up table (LUT) implementation of the efficient Huffman encoding. In Huffman mode, the difference between the actual sample and the last one is calculated for each incoming sample; after that, the value is searched in the code look-up table.

If it is found in the table, Huffman replaces the data with a variable length encoding of it, which was previously stored in the table. The encoded version is usually smaller than the original, possibly reducing the output bandwidth. On the other hand, if the data is not in the table, the algorithm adds a marker in front of the data and sends it out.

A good strategy in this scenario is to consider the expected data behavior to create an efficient table using the Huffman algorithm, in a way that the block would operate in a near optimum condition, replacing the most frequent codes with the smaller codifications (HUFFMAN, 1952).

It is important to note that the compression block was not implemented with a full 1024 code book for the input data range due to space limitations. This author has proposed a solution reusing the data shaper filter coefficients of four channels to create this LUT (with Huffman, there is no need for run-time tail cancellation). This table represents a major part of the block, where with this strategy, Huffman fitted in SAMPA².

After compression, a stream of clusters will be ready for serialization. But to permit their identification on the receiver side, a header needs to be included, labeling and storing the clusters in packets. The next section describes these steps and the chip communication protocol.

3.2.9 Buffering and output protocol

The data acquisition in the ASIC has two main modes, trigger based and the continuous read-out. The triggered mode works based on an input signal which activates the data storage for a configurable amount of ADC conversion cycles. This period is called time-window and can be as long as a 1024 samples. The continuous mode works in a similar way, but there is no need for external triggering; the chip is always active and acquiring data samples, auto triggering itself at the end of each time window.

When a time window finishes, the chip creates a new packet header, which is responsible to identify the data collected in terms of size, time-stamp and origin.

Each SAMPA channel was designed including two dedicated SRAM blocks for packet buffering, the first is designated to store the cluster data stream, having 6144 words capacity (SAMPA uses 10 bit words). The second is the header memory, responsible to store packet headers up to the moment they will be sent. This memory is smaller and stores 256 words (about 51 packet headers).

The author has proposed this dual memory system in a way to reduce the probability of buffer overflows in the headers memory, which could cause loss of data tracking in the system. In the proposed solution, the data do not compete with headers for buffer space, implying in a much smaller chance of header overflow. The system may have data bursts, but they will be handled with the data memory space, being the headers free to register the events and even the occasional occurrence of overflows in data memory.

A SAMPA packet consists of a header, possibly followed by a variable length

² This solution was accepted and used by Velure (2019) to a successful RTL implementation of this block.

data stream. The packet header is composed of 5 words (50 bits) and includes several information fields depending on its type.

A very important packet type is the data packet; this usually contains a payload with information measured during a time window. Figure 26 shows the format specification of a data packet header.

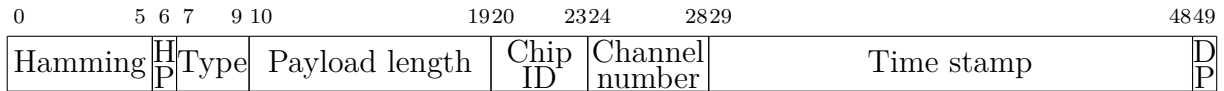


Figure 26 – Format specification of a 50 bit data packet header (The numbers on the top of the packet indicate the bit index counting from zero).

As SAMPA has multiple channels, each packet identifies which channel was the data source using the field *Channel number*. Additionally, multiple chips can be in use and, in this way, the input pins *hadd[3:0]* can be used to set the hardware address of the device (between 0 and 15), that is sent in the field *Chip id*, properly identifying the data in relation to chip and channel of measurement.

The packets will be received much after the real measurement and they can be buffered in several devices in the path, SAMPA adds a timestamp of 20 bits to each packet to identify the acquisition time. This time value is generated from a counter running at the LHC particle bunch crossing frequency (approximately 40 MHz) which is an important global reference in the experiment.

A variable quantity of information is expected to be inserted in each payload, as the activity in each channel may fluctuate and different compression may be applied, thus the field *Payload size* contains the number of 10 bit words of this packet payload. This value can be from zero to 1023, but an extension to bigger sized packets is also available encoding an extra bit in the packet *Type* field. Table 3 lists the possible packet types in SAMPA.

Table 3 – List of the available packet types

Packet <i>Type[2:0]</i>	Data Packet	Extended Size	Heartbeat	Sync	Trigger too early	Data Overflow
0			X			
1	X					X
2				X		
3	X				X	X
4	X					
5	X	X				
6	X				X	
7	X	X			X	

In table 3 it is possible to see that most of the packet types are data packet, where the differences include distinct kinds of it, as the extended size version, which can go over the 1023 size with this extra flag. The trigger too early type is another interesting case, where the chip receives a trigger in the run-time of an acquisition in progress. This packet informs the receiving side that the trigger was received in this circumstance, but the data will be acquired as requested.

Data bursts may possibly happen in the chip input depending on the experiment activity. This can lead the buffer data memory to be full in some configurations when the input bandwidth can be much higher than the output. SAMPA can notify the receiver that the buffer has gone full and a packet of data was discarded using the Data Overflow packet type, allowing the proper future tracking of this artifact.

There are also two special packets named Heartbeat and Sync. The first is a packet with no payload used to notify the receiver that the chip and the communication is operational. The Heartbeat can also be requested by slow control or by a dedicated pin and the packet carry the time stamp of the event.

Finally, the Sync is a constant packet with zero payload size and a very specific alternating pattern written in its timestamp field (0xAAAAA). This oscillating pattern together with the fact that the packet does not vary at all helps the receiver to synchronize the link and proper align its decoders to the correct header start position.

The chip always initiates the link operation using a Sync packet and keeps sending this whenever there is no useful data to be serialized out, this allows the receiver to be synchronized and read for data packets. Each of the eleven serial outputs has the ability to send its own Syncs and is totally parallel and independent of the others.

This author has proposed the present protocol and it also received several protections to properly operate in the experiment environment, where single events can affect the block and the data flow.

Each packet created in SAMPA has its header protected using hamming code for single error correction double error detection (SECDED); this can correct up to one error in the header and indicate if there is an uncorrectable double error. With this, most of the headers will be properly decoded, allowing adequate data flow. The receiver can also resynchronize and align to the next correct packet in case of a double error corrupt the header.

The encoder is implemented in parallel, generating the protection parity code in a single clock cycle. The encoded value is written in the 6 bit field *Hamming* indicated in the beginning of figure 26.

To limit the overhead, the payload data do not receive error correction capabilities, on the other hand, an even parity bit is added, which can be used by the receiver to check

if there is an error in the payload. This bit is noted as *DP* in figure 26.

An extra even parity is also added to the full header, allowing the quick check for errors using the bit *HP*, written just after the *Hamming* code field at figure 26.

This protected packet based communication is an important SAMPA contribution not available on its predecessors (BOSCH *et al.*, 2003; GARCIA, 2012), where in addition SAMPA operates with a configurable amount of independent differential serial links, in place of the old parallel bus used before.

SAMPA can run with at least one and up to eleven active serializers, where depending on this amount a different division of input processing channels will be attributed to each serial output. Table 4 shows the mapping between channels and serial outputs (SO), depending on the number of enabled links.

Table 4 – Mapping between channels and serial outputs depending on the number of enabled links

Channel	Number of links enabled											
	1	2	3	4	5	6	7	8	9	10	11	
0	SO0	SO0	SO0	SO0	SO0	SO0	SO0	SO0	SO0	SO0	SO0	SO0
1	SO0	SO0	SO0	SO0	SO0	SO0	SO0	SO0	SO0	SO0	SO0	SO0
2	SO0	SO0	SO0	SO0	SO0	SO0	SO0	SO0	SO0	SO0	SO0	SO0
3	SO0	SO0	SO0	SO0	SO0	SO0	SO0	SO0	SO0	SO0	SO0	SO1
4	SO0	SO0	SO0	SO0	SO0	SO0	SO0	SO0	SO1	SO1	SO1	SO1
5	SO0	SO0	SO0	SO0	SO0	SO0	SO0	SO1	SO1	SO1	SO1	SO1
6	SO0	SO0	SO0	SO0	SO0	SO1	SO1	SO1	SO1	SO1	SO1	SO2
7	SO0	SO0	SO0	SO0	SO1	SO1	SO1	SO1	SO1	SO1	SO1	SO2
8	SO0	SO0	SO0	SO1	SO1	SO1	SO1	SO2	SO2	SO2	SO2	SO2
9	SO0	SO0	SO0	SO1	SO1	SO1	SO1	SO2	SO2	SO2	SO2	SO3
10	SO0	SO0	SO0	SO1	SO1	SO1	SO2	SO2	SO2	SO2	SO2	SO3
11	SO0	SO0	SO1	SO1	SO1	SO1	SO2	SO2	SO2	SO2	SO3	SO3
12	SO0	SO0	SO1	SO1	SO1	SO2	SO2	SO3	SO3	SO3	SO3	SO4
13	SO0	SO0	SO1	SO1	SO1	SO2	SO2	SO3	SO3	SO3	SO3	SO4
14	SO0	SO0	SO1	SO1	SO2	SO2	SO2	SO3	SO3	SO4	SO4	SO4
15	SO0	SO0	SO1	SO1	SO2	SO2	SO3	SO3	SO3	SO4	SO4	SO5
16	SO0	SO1	SO1	SO2	SO2	SO2	SO3	SO4	SO4	SO4	SO4	SO5
17	SO0	SO1	SO1	SO2	SO2	SO3	SO3	SO4	SO4	SO5	SO5	SO5
18	SO0	SO1	SO1	SO2	SO2	SO3	SO3	SO4	SO4	SO5	SO5	SO6
19	SO0	SO1	SO1	SO2	SO2	SO3	SO3	SO4	SO4	SO5	SO5	SO6
20	SO0	SO1	SO1	SO2	SO3	SO3	SO4	SO5	SO5	SO6	SO6	SO6
21	SO0	SO1	SO1	SO2	SO3	SO3	SO4	SO5	SO5	SO6	SO6	SO7
22	SO0	SO1	SO2	SO2	SO3	SO4	SO4	SO5	SO5	SO6	SO6	SO7
23	SO0	SO1	SO2	SO2	SO3	SO4	SO4	SO5	SO6	SO6	SO7	SO7
24	SO0	SO1	SO2	SO3	SO3	SO4	SO5	SO6	SO6	SO6	SO7	SO8
25	SO0	SO1	SO2	SO3	SO3	SO4	SO5	SO6	SO6	SO7	SO7	SO8
26	SO0	SO1	SO2	SO3	SO4	SO4	SO5	SO6	SO7	SO8	SO8	SO8
27	SO0	SO1	SO2	SO3	SO4	SO5	SO5	SO6	SO7	SO8	SO8	SO9
28	SO0	SO1	SO2	SO3	SO4	SO5	SO6	SO7	SO7	SO8	SO8	SO9
29	SO0	SO1	SO2	SO3	SO4	SO5	SO6	SO7	SO8	SO9	SO9	SO9
30	SO0	SO1	SO2	SO3	SO4	SO5	SO6	SO7	SO8	SO9	SO9	SO10
31	SO0	SO1	SO2	SO3	SO4	SO5	SO6	SO7	SO8	SO9	SO9	SO10

Each active serializer will continuously check for available packets in its attributed channel list using table 4 mapping in a round-robin loop. If ready data is found in a channel, the serializer will request it from the buffer memory, transmitting it using its output link.

It is important to note that if a heartbeat packet is requested, it has priority and is always sent in the serial link zero. Also, synchronization packets will be sent by any link which is not busy with other packet types, keeping the receiver alive and in sync.

SAMPA additionally provides a channel reordering scheme, and several other output capabilities which will be omitted from here for compactness and due to the small connection with the next chapters. In case of extra interest please see (ADOLFSSON *et al.*, 2017; SANCHES; VELURE, 2018; HERNÁNDEZ *et al.*, 2020; VELURE, 2019).

The next sections will introduce the ASIC development path through its main tape-outs, addressing the SAMPA fabricated prototypes and their key characteristics.

3.3 The SAMPA prototypes

During the development of the SAMPA project, several real prototypes were implemented and manufactured.

In this section, the most important tape-outs will be discussed following the history of the development of the ASIC from the first multi-project wafer (MPW) to the final solution delivered to CERN.

It will focus mainly on the digital part, but some neighboring blocks with relevant system importance will also be quickly mentioned.

3.3.1 SAMPA MPW 1 prototype

The SAMPA MPW 1 was the first silicon prototype of the blocks that should be used in the complete version of SAMPA and was fabricated in order to get an estimate of the process performance and how these blocks would interact to each other with respect to noise and crosstalk. This MPW was also a very important source of information in relation to the digital core and its measurements both in normal environment and when exposed to radiation.

This tape-out used the Taiwan Semiconductor Manufacturing Company (TSMC) 130 nm process and was composed of three very different chips, which will be briefly described next, providing a general outlook of how the mixed signal ASIC needed by CERN could be achieved.

The first chip was a pure analog project, containing the initial part of the front-end, this block is just included here for completeness as it plays an important role in the full ASIC, but has no contributions from this thesis.

The figure 27 shows a photo of the chip 1, where five similar front-end channels can be seen, placed as rows. The box labeled "A" identifies the charge sensitive amplifier

and the box "B" shows the shaper (HERNÁNDEZ, 2015). Each single channel row has $2300\ \mu\text{m} \times 150\ \mu\text{m}$ and the full chip 1 area is approximately $4\ \text{mm}^2$.

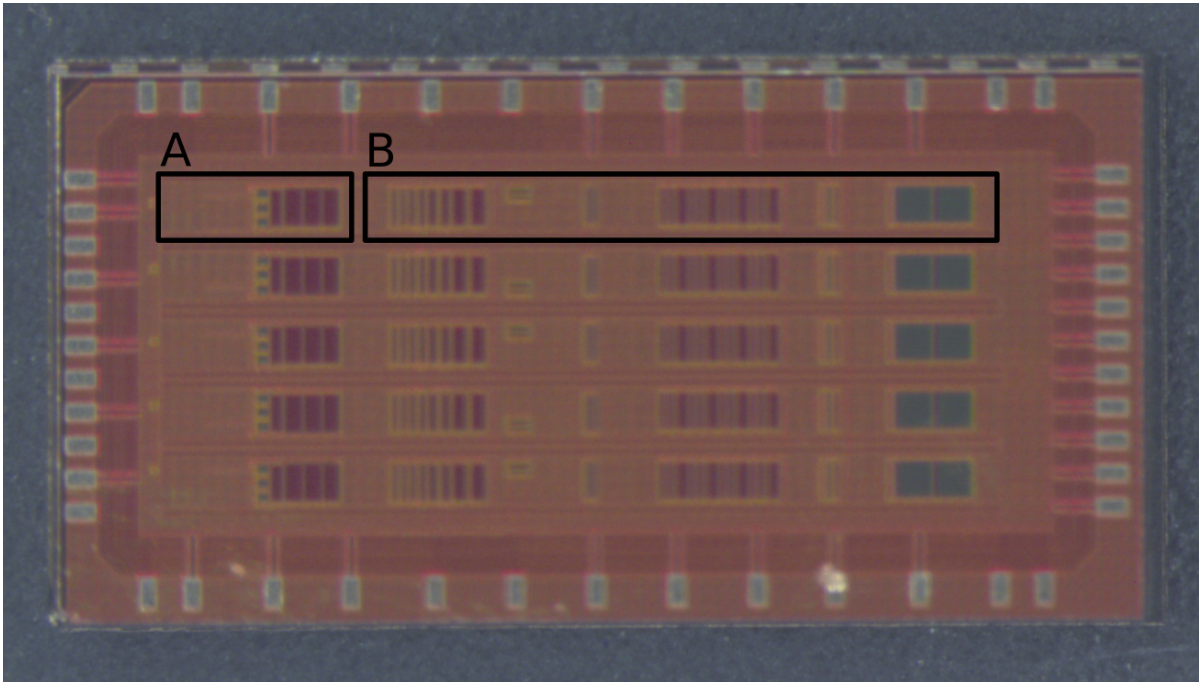


Figure 27 – Photo of the MPW1 front-end test chip with its 5 analog channels.

Source: Alex Kluge and the author.

The MPW1 chip 1 was very successful and it is the fundamental test part used in the first thesis related to SAMPA, the work of HERNÁNDEZ (2015).

In the MPW1 chip 1, the present author had just worked in the measurement phase and so this will not be further mentioned here, the results were successful and served as base for our publication Barboza *et al.* (2016). For the remaining chips that will follow, this author contributed with a considerable greater design participation. Continuing in the system signal path order, the analog to digital converter will be the next discussed block.

The MPW1 chip 2 was a multi-purpose test prototype that included three very important parts of SAMPA, the analog to digital converter, the SLVS receiver and the SLVS transmitter. The drivers were discussed in the work HERNÁNDEZ *et al.* (2017), already presented by this author in International Symposium on Circuits and Systems (ISCAS) 2017, and to minimize this section, will be omitted.

In the figure 28 the full chip 2 is shown, where the total area consumption was approximately $3\ \text{mm}^2$. The ADC block is marked with a black rectangle where it is possible to see the two big metal-insulator-metal (MIM) capacitor arrays from the DAC at the top left and right. In the bottom part of the rectangle, there is a row shaped structure that is the successive approximation logic where the author had also contributed in the ADC³.

³ The final SAMPA ADC block had as contributors Hugo Hernandez, Bruno Sanches, Rafael Moraes and Ronaldo Wilton.

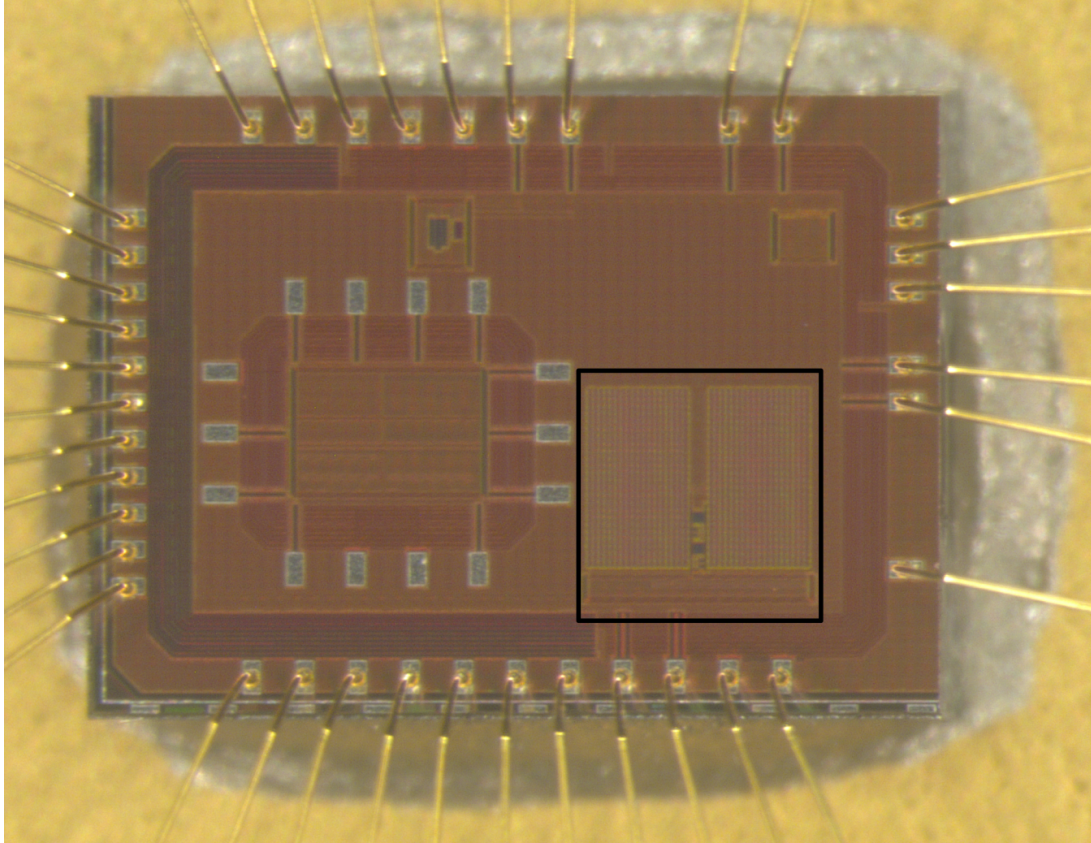


Figure 28 – Photo of the MPW1 - chip 2 - The ADC test chip.

Source: Alex Kluge and the author.

The ADC is mainly shown here due to the fact that it is the main data source to the SAMPA digital core and the cited successive approximation logic will be further addressed in the present work.

Finally, chip 3 was the last in this MPW, being designed as a miniature version of the full SAMPA, containing three complete channels, including the front-end, ADC and digital processing core. Figure 29 shows a micro-photography of this chip, which is substantially bigger than the previous chips using an area around 17 mm^2 .

In the figure 29, the "A" labeled box marks the area with 3 front-ends (HERNÁNDEZ, 2015), that are followed by 3 analog to digital converters in the region "B", being then connected to the digital signal processing block, labeled with the rectangle "C".

This author also created a test block marked as "D" with the remaining MPW area. That was composed of a long shift register with 15000 flip-flops (of the smaller type available in this design kit). This shift register was included aiming for radiation resistance testing and in a better understanding of this process. It is important to cite that, at that time, TSMC 130 nm was being used for the first time by SAMPA designers and also the collaboration was changing to TSMC foundry.

The inclusion of this block was very relevant and further had shown to be critical

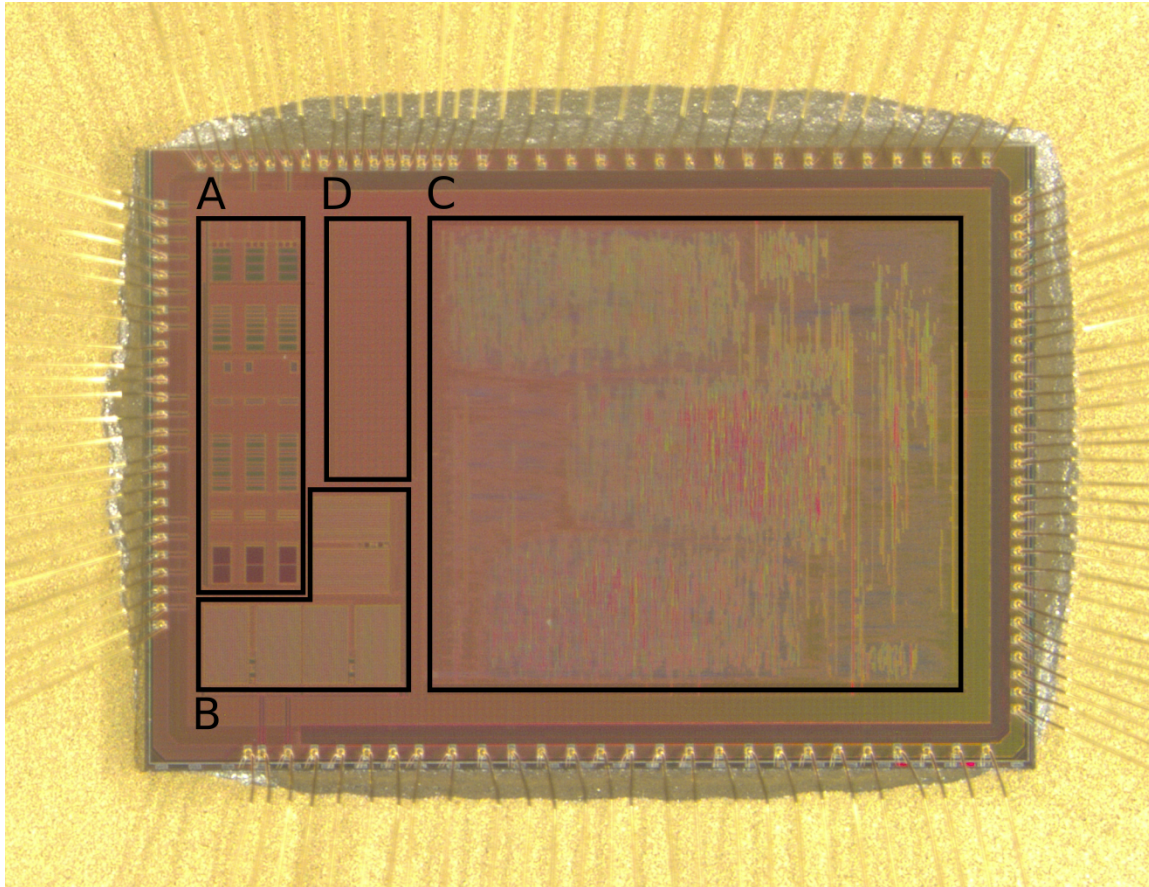


Figure 29 – Photo of the MPW1 chip 3.

Source: Alex Kluge and the author.

as it allowed very early radiation testing of this project (MAHMOOD *et al.*, 2018), being used as a reference up to its end. The next section continues with the SAMPA V2 full chip prototype.

3.3.2 SAMPA V2 prototype

With the promising results of the MPW1 (HERNÁNDEZ, 2015; BARBOZA *et al.*, 2016), the ALICE collaboration interest in the full SAMPA increased, culminating in the extension of the supporting project by the research agency. After several months of design, the initial prototype of the 32 channels ASIC was ready to be submitted and was named as SAMPA V2.

SAMPA V2 was equipped with most of the requirements needed by the CERN ALICE Collaboration in its time (ANTONIOLI; KLUGE; RIEGLER, 2013; ALICE; APPELSHÄUSER; LIPPMANN, 2013), including the filters, memory and serializers described in section 3.2.

The design was fabricated by TSMC and sent to the Institut de Physique Nucléaire d'Orsay to be further diced and wire bounded directly on dedicated printed circuit boards.

This kind of board mounting approach was made focusing on fast testing, due to its reduced packaging time and also to make the radiation tests with protons and heavy ions viable.

Figure 30 shows one of the SAMPA V2 wafers. This was an engineering run and, in this way, the full wafer area was dedicated exclusively for this project. The process used was TSMC 130 nm with 7 metal layers. At this time, the fabrication was performed using the multi layer mask (MLM) technological strategy, reducing the number of full masks by a factor up to four and saving costs.

As the full run was dedicated to this project, the tape-out could be managed to include the full SAMPA V2 and several additional test blocks, without additional expressive costs per area, as usual in a MPW.

The mask reticle had 9.6 mm x 15.0 mm and carried the complete SAMPA V2 along with an analog test chip of 32 front-end channels (without the ADCs or DSP), a chip with a single ADC and other chips with smaller test blocks as the reference voltage generator and the SLVS high speed drivers.

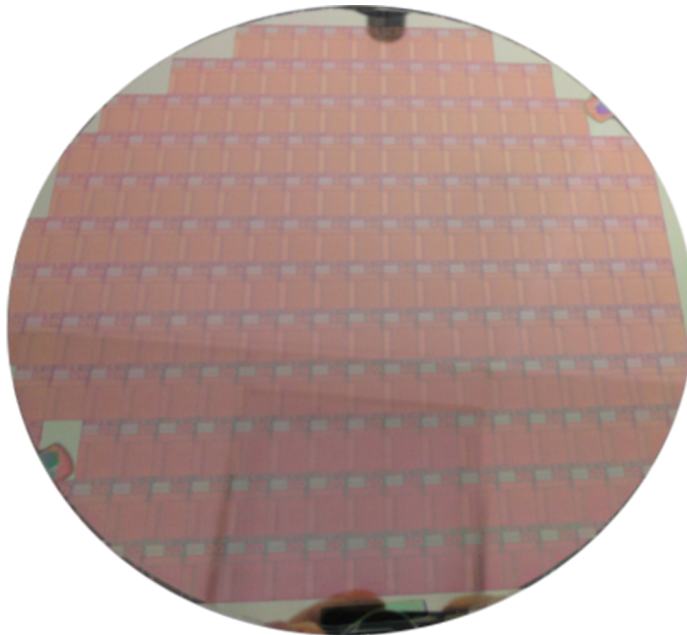


Figure 30 – Photo of the SAMPA V2 wafer.

Source: the author and the Institut de Physique Nucléaire d’Orsay.

Figure 31 shows a photography of the SAMPA V2 die. In the image, it is possible to see (from left to right), the 32 analog front-ends connected to 16 pairs of ADCs that are followed by the big signal processor at the full right side. The full chip dimensions were 9.53 mm x 8.94 mm totalizing an area of more than 85 mm².

The SAMPA V2 prototype was a successful prototype with respect to its specifi-

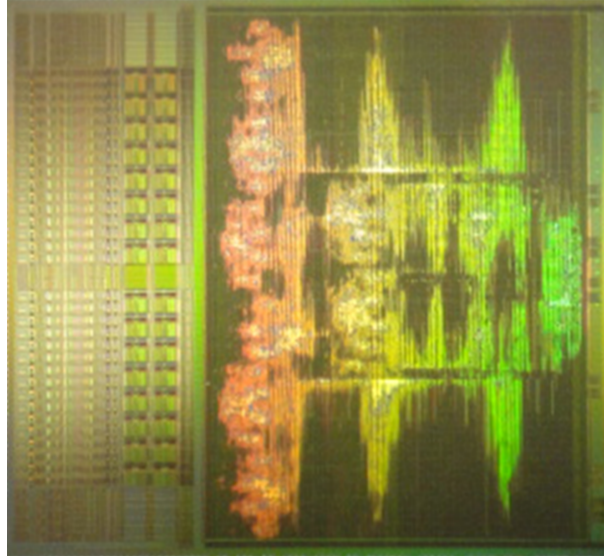


Figure 31 – Photo of the SAMPA V2 die.

Source: the author and the Institut de Physique Nucléaire d’Orsay.

cations culminating in our publication (ADOLFSSON *et al.*, 2017). This ASIC proved that the big challenge imposed by the integration and mixed system design in this project could be surpassed (ANTONIOLI; KLUGE; RIEGLER, 2013; ALICE; APPELSHÄUSER; LIPPMANN, 2013).

However, the chip was not fully accepted by the ALICE collaboration due to several reasons; these included post tape-out specifications changes, both in analog and digital core.

In relation to the analog core, changes in pile-up resistance were requested and the ADC also received improvements. These changes are out of the scope of this work and will not be analyzed (HERNÁNDEZ, 2015; HERNÁNDEZ *et al.*, 2020; BREGANT *et al.*, 2017).

Regarding the digital block modifications, the initial changes were about the data formatting and radix representation (BREGANT *et al.*, 2017; SANCHES; VELURE, 2018).

Improvements and corrections in higher input pulse data occupancy scenarios were done in the packet buffers (BREGANT *et al.*, 2017; SANCHES; VELURE, 2018). Cases with multiple chips were also addressed and modified in order to the system be capable to better handle data bursts coming from the neighbors SAMPAs in chained mode⁴ (SANCHES; VELURE, 2018).

The radiation tolerance was also not compatible with the requirements of the

⁴ The work of the verification engineer Raul Acosta Hernandez was essential in this step, being the full testbenches and high coverage just reached due to its extensive simulations.

detector (MAHMOOD *et al.*, 2018)⁵. Therefore, joining all these artifacts justified the need for new SAMPA versions.

3.3.3 SAMPA V3 and V4 prototypes

After the evaluations and tests of SAMPA V2 (BARBOZA *et al.*, 2016; ADOLFSSON *et al.*, 2017; MAHMOOD *et al.*, 2018), the chip was qualified and several of its weaknesses revealed. These points pushed for several refactorings and analyses in the new designs.

With the feedback of the single event latch-up investigation techniques discussed further in this work, a new version of the digital signal processor was developed and used in the full layout of SAMPA version 3 (SAMPA V3).

The ALICE collaboration also wanted to have a chip with better analog front-end pile-up rate immunity which triggered the development of a new front-end⁶.

SAMPA version 4 (SAMPA V4) was the final result of the analog changes, including the new modified front-end and sharing the same digital signal processor design as SAMPA V3. This core already implemented corrections and improvements, being possibly more tolerant to the radiation single event effects.

The tape-out of SAMPA V3 and V4 were very audacious steps as the designs had major modifications in dozens of square millimeters, going direct to a mass production runs, without having been tested through an MPW before. Since the ALICE and CERN schedules were tight, this was needed and the fabrication was performed assuming the risks involved, trusting in the simulations and in the designer's accumulated experience.

Figure 32 shows the final SAMPA V4 die photography with a descriptive text overlay. The pad ring pinout is illustrated along with the identification of the charge sensible amplifier, shaper, ADC and digital signal processor blocks. The full chip achieved more than 36 million transistors.

The resulting dies were packaged in 352 pins ball grid array (BGA) capsules to attend the tight board space requirements from ALICE MCH. An image of a ready device is shown in figure 33 measuring just 15 mm x 15 mm.

To finalize this section, the silicon areas of the main building blocks of SAMPA are presented in the table 5, allowing the reader to position the present work in relation to SAMPA chip.

The SAMPA V4 design was evaluated in a production readiness review (PRR) by an external committee invited by CERN on 20/02/2018. The chip was approved for

⁵ These facts, measurements and corrections are discussed in sections 3.4.4 and 4.2.

⁶ This was performed by the original front-end engineer Hugo Hernandez in a complement of its work HERNÁNDEZ (2015).

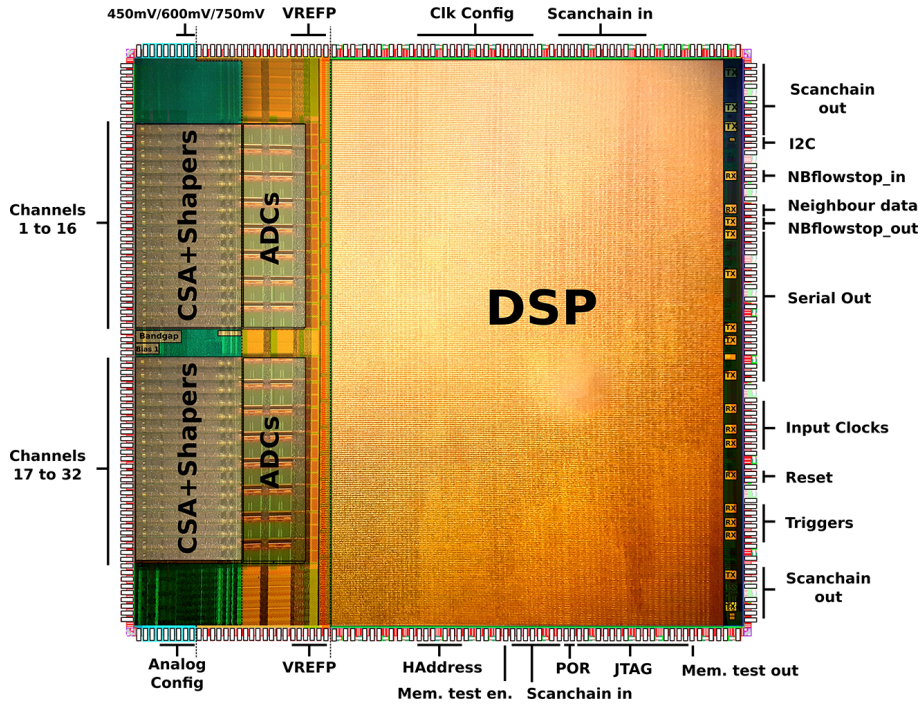


Figure 32 – Photo of the SAMPA V4 die.

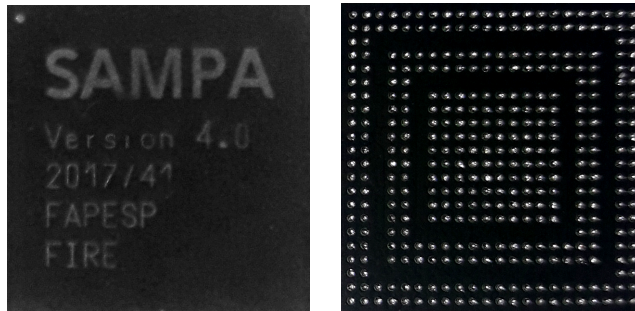


Figure 33 – Final SAMPA V4 15 mm x 15 mm BGA package.

Table 5 – SAMPA silicon areas

Block	Width [μm]	Length [μm]	Area [mm^2]
I2C Driver	72	41	0.003
SLVS Receiver	142	82	0.012
SLVS Transmitter	154	112	0.017
Power on Reset	159	229	0.036
Bandgap	305	222	0.068
ADC	451	323	0.146
Front-end	1559	193	0.301
DSP (32 channels)	5897	8536	50.337
Full SAMPA chip	9534	8944	85.272

usage in the experiment and its mass production was authorized (LLOPART *et al.*, 2018; ALICE TPC COLLABORATION *et al.*, 2021). This was a remarkable step for this project, which the achievement correlates with this work and its findings. The next sections will

address the proposed radiation tolerance automated optimizer and the single event latch-up avoidance strategies used in SAMPA.

3.4 Radiation tolerance improvement

This section will be dedicated to the description of techniques used in the literature and in this work to obtain better tolerance to the failures while operating in radiation environments.

Initially, the technological node influence is briefly discussed and after general strategies for digital systems are shown. Further, an automated method for increasing the error tolerance is presented using digital synthesis tools along with artificial intelligence algorithms and hardware description languages.

Finally, a method for detecting possible single event latch-up sites in the ASIC is also proposed based on the knowledge acquired in SAMPA V2 development and debugging.

3.4.1 Process technology nodes

With the technology nodes scaling, the device silicon size is being reduced and, in this way, changes are expected to happen with respect to the radiation resistance of the transistors and the system itself.

Initially evaluating the total ionizing dose effects, the figure 34 compares the data from a compilation over several articles in the Institute of Electrical and Electronic Engineers (IEEE) Nuclear and Space Radiation Effects Conference (NSREC) radiation effects data workshop records (DODD *et al.*, 2010). In figure 34, open symbols represent functional failures, while the other symbols are related to failures due to device parameter deviation.

Analyzing the total ionizing dose (TID) failure level with respect to the technology, it is possible to see that in this analysis it has been viable to achieve a growing level of dose resistance along the technology scaling in this range.

In the figure 34 is also visible that the nodes under 180 nm clearly had a big increase in the tolerance in comparison with their neighbors and especially around the node 130 nm, the one used in the development of this work (chosen due to the adequate cost versus density balance and also because of CERN preferences and previous technological and radiation analysis).

Another very important class of radiation interaction in electronic devices is the single event effects. This class of events aggregates the several kinds of disturbances that can be caused by a single ionizing particle strike. To better divide the possible consequences, some of the events correlated with the present work will be briefly described:

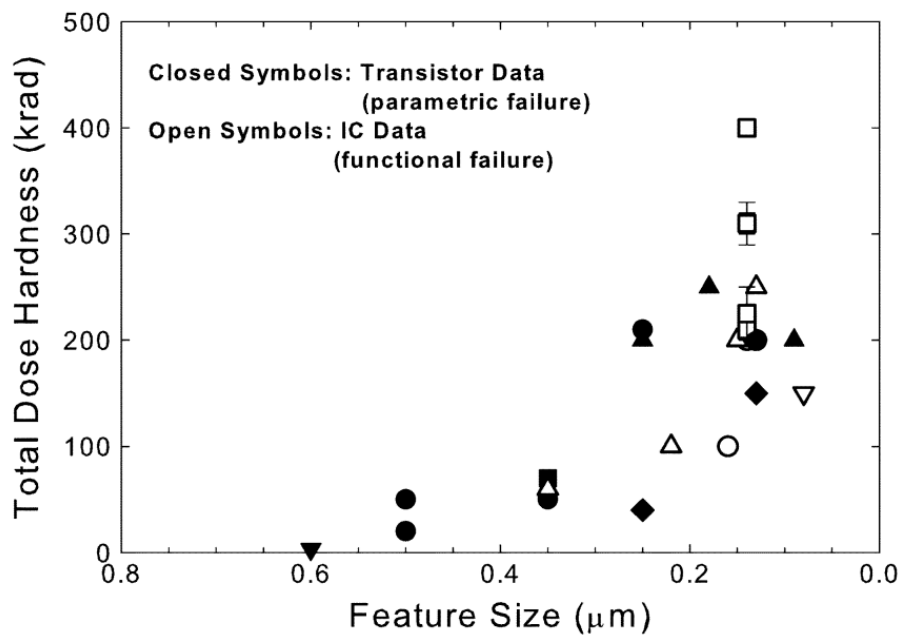


Figure 34 – TID failure level scaling trend for digital CMOS technologies.

Source: Dodd *et al.* (2010).

the single-event upset (SEU), the single-event transient (SET) and the single event latch-up (SEL).

A SEU is an eventual change of state of a bit due to the particle strike. The occurrence of a SEU is possible when the collected fraction of the charge produced by the interaction can considerably modify the amount of electric charge stored on a sensitive node. A sensitive node is defined as a node in a circuit whose electrical potential can be modified by internal injection or collection of electrical charges (NICOLAIDIS, 2011). Usually, an information bit is associated with a voltage level, some cases stored in a capacitor, in other cases at some kind of feedback gate network.

SEUs are usually linked with the state of a system, on the other hand, the undesired logic change in a combinatorial path due to the charges deposited by the interaction with radiation is named as single event transient.

A single event transient can happen in several portions of the logic possibly causing distinct consequences, per example, if in between registers there is a chance that the error propagates through the combinatory logic and arrive at the destination register, being stored and propagated in the next cycles. In this case, the transient is similar to an upset in the destination register. Another possibility is that the transient is gone before the next setup time of the destination, in this circumstance no error may appear. The system effect of the transient in this situation will be very dependent on the timing and energy of the interaction.

There is also the case of transients in the combinatory logic from inputs to registers,

this can be similar to the register to register combinatorial error path if the logic in this path is related to a synchronous input. On the opposite side, there is the case of asynchronous inputs, commonly used as triggers, resets and others low latency signals. In the asynchronous case more care needs to be taken as any sufficiently long transient in the signal can propagate and generate system problems, and this erroneous event even not necessary need to be clocked in by any register to take place. The last cited case is the transient in combinatorial logic related to the calculation of system outputs, which is particularly important due the possibility of failure propagation to domains outside the chip in question.

The cited single event effects are linked to the logic domain of the circuit but there are other kinds of effects like the SEL which can cause problems beyond the logic domain, affecting even the power rails of the chip.

A single event latch-up is when an ionizing particle can trigger the parasitic silicon-controlled rectifiers formed in CMOS process, due to the implants in sets of NMOS and PMOS transistors. After triggering, if enough voltage exists between the device VDD and VSS, it can remain activated permanently (up to system power shut-down).

Depending on the dissipated energy the latch-up can be destructive or not, but in general, it will cause at least functional failures due to the inserted low impedance device between VDD and VSS draining a big current and probably causing voltage drops.

Focusing back on the single event effects in the logic, the figure 35 shows the evolution of simulated critical linear energy transfer (LET) value for several technology nodes in respect to SRAM single event upsets and unattenuated single event transients. The scenario, in this case, is quite different than the encountered in the dose effects; here there is a decreasing threshold LET. This sensitivity happens in both silicon on insulator (SOI) and bulk CMOS processes and affect SET and more expressively the SEU.

The bulk process is more sensitive, being the SOI an option for extra resistance. Also comparing the single event transients and the upsets, the single event upsets tend to be more sensitive than single event transients and this happens for both SOI and bulk CMOS.

This goes exactly in the direction of the present work as the redundancy and the developed algorithms are primarily targeted to reduce the single event upsets and its consequences in the system.

3.4.2 Strategies

Techniques and softwares capable of evaluating or increasing the radiation tolerance are becoming very important, especially when running in the design phase.

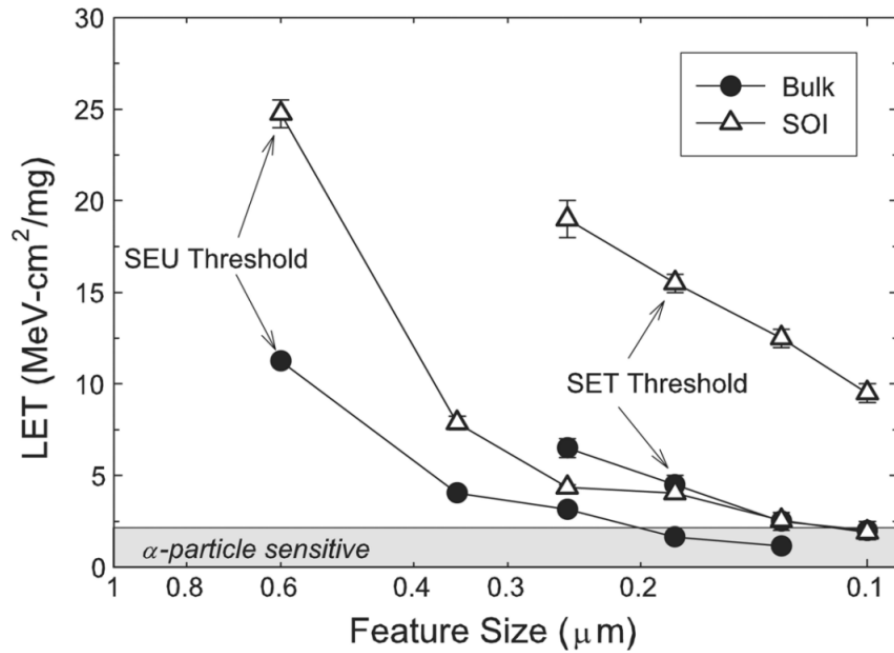


Figure 35 – Simulated critical LET for unattenuated transient propagation and SEU threshold LET as a function of scaling for bulk and SOI CMOS technologies.

Source: Dodd *et al.* (2004).

This is a frequent need in space, medical, high availability and in physics experiments like the one in this work, where there are trade offs like reliability, data rate, area and other specifications while running in an environment with radiation.

There are several reasons for this increased importance and it is possible to cite that characterizing the behavior and error rate during the design phase is critical for avoiding undesirable results, especially when the circuit prototype or the final product is tested, which could lead to extra fabrication cycles and loss of market opportunities (NICOLAIDIS, 2011; MAHMOOD, 2020). Also, interactive error rate estimation during the design cycle is one major way for making the necessary tradeoffs, determining the circuit critical parts and selecting the most efficient mitigation approaches for meeting a reliability target at minimal cost in terms of power, speed, and area (NICOLAIDIS, 2011).

To accomplish this, software and hardware tools at several levels may be required. Examples of these compiled from Nicolaidis (2011) are cited in the following list:

- Technology computer-aided design (TCAD) tools for characterizing the transient current pulses produced by alpha particles and secondary particles.
- Cell failures in time (FIT) estimation tools to guide the designers of memory cells and cell libraries for meeting their error rate budget at minimal cost, and for providing the cell FIT to the higher level estimation tools.

- Spice-level FIT estimation, usually for evaluating the impact of transient pulses in sequential cells and in combinatory logic or mixed signal blocks.
- Gate-level FIT estimation tools for characterizing modules and IP blocks.
- RTL FIT estimation.
- System on chip (SoC) FIT estimation, for taking into account the functional metrics variation at the SoC level.
- Fault injection in hardware platforms for accelerating the FIT estimation task at IP level and SoC level.
- Soft-error mitigation approaches at hardware level including error detecting and correcting codes, hardened cells, self-checking circuits, double sampling approaches and instruction-level retry.
- Soft-error mitigation approaches at software level, operating system level, as well as check-pointing and rollback recovery.

There are several techniques applicable in systems similar to the ones involved in this thesis and which correlate to improvements in hardware, for example: error correction codes, bit interleaving, periodical refresh/resetting, triple modular redundancy, time redundancy or even redundancy at the software level, being the latter two applicable in some specific cases, but not used in the present work due to the design choices in data-path and the absence of software in SAMPA design.

The next section will address the artificial intelligence based optimizer using the cited redundancy strategies in order to coordinate the insertion of protection on selected devices aiming for specifically defined metrics.

3.4.3 Automated radiation tolerance improvement

The process of increasing the tolerance for the errors caused by the interactions with radiation is full of options and, with the increasing design complexity of the systems, it can become difficult for the designer to understand the cause effect relations when developing the circuits.

At the same time, there are several trade-offs in micro-electronic design, being the power, area and cost very typical ones. In the case of adding redundancy, it is clear that it can directly increase the area, and very likely the power. In relation to the cost, this may also increase because the yield will fall with the area. The redundancy added is not included aiming to fix failures in the fabrication, but run-time ones; since only fully

operational chips are approved for final usage, reducing the yield and impacting in more production cost.

Each design will have its own restrictions but taking SAMPA as an example there were different specification trade-offs factors, where one of the most important ones is that the chip should fit in a small board in the muon chamber experiment, being this board very limited in width, as so, SAMPA was delivered in a BGA package trying to maximize the useful surface, but even with that the area of the chip was an important constraint.

In complement to the area constraint, there was the budget limitation also restricting the area in some way and at the same time, the users of the chip would like to have as much data memory as possible to accommodate bursts of detected pulses in the buffers with minimal or zero data loss.

The involved particle physics experiments are also in confined spaces with very tight cooling specifications and, as the system would contain hundreds of thousands of channels, it is mandatory to respect a specified level of power consumption.

With these trade-offs and a system with several hundreds of blocks, the difficulty to search and find a feasible solution increases and, in this direction, automated procedures emerged as an option to simplify and optimize this kind of design flow.

SAMPA DSP and several other digital systems around the globe are developed using HDLs like Verilog, VHDL, System Verilog and others. This can open several new options for automation as these languages present several typical ways to describe hardware that can be linked to an optimizer.

During the coding of the present work, when implementing registers or a block that would possibly need protection, the recommendation for the designer was to use a standard notation for this declaration and maybe for the subsequent attributions and usages. With this approach, specific tools could scan the developed HDL and try to understand and interchange the possible alternatives to add redundancy and protection, or even remove it to prioritize another trade-off variable or region of the ASIC if needed.

3.4.3.1 Redundancy options

There are several alternatives to protect a block from single events with redundancy and these can be implemented manually or by automated processes, in this section two methodologies will be addressed aiming to ease these alternatives and increase the designer productivity. The first methodology uses HDL macros and in house developed codes. A second possibility is also shown using state of art external tools to make the optimizer more extensible.

A typical way to mitigate the problems caused by single events is the use of redundancy and a frequent solution is the implementation of triple modular redundancy

(TMR). This approach is based on the triplication of the vulnerable entity followed by the addition of a majority voter to decide the output value. The majority voter is then able to correct one error in any of the three replicated blocks, trusting in the other two.

Figure 36 illustrates the triplication of a fundamental storage element in digital designs, the data flip flop (DFF). Figure 36 (a) shows the single DFF and Figure 36 (b) demonstrate a possible TMR implementation with a single clock.

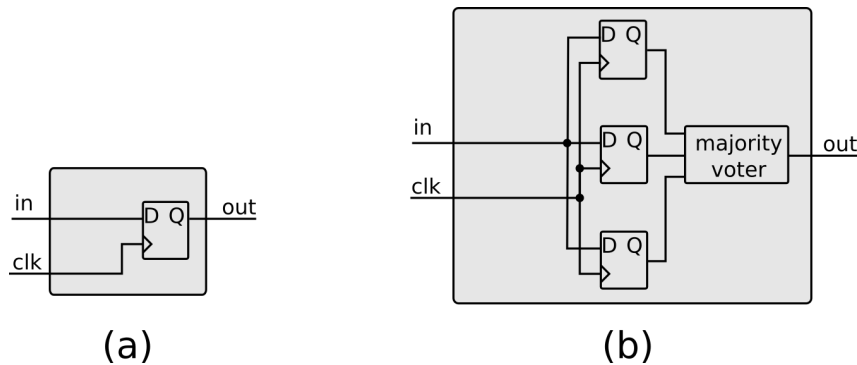


Figure 36 – A TMR DFF implementation block diagram, in (a) a single standard DFF and in (b) its TMR implementation.

The replication increases the minimal area of the entity by several times but on the other hand, can be a simple alternative to protect the DFF from single errors per TMR.

The insertion of TMR in a system can be a long and massive task with several chances of pitfalls if made in a pure manual fashion. Typical problems are related to the strong similarity in the signals which cause error prone modifications in the code and the lack of constraints to the synthesis software, which may remove the TMR in its optimizations and several other issues.

One improvement in this step is proposed in this work for the SAMPA design including specific developed macros for register variable declarations. Figure 37 shows a set of Verilog macros used in SAMPA code, including the triplication with the *TMR* and the *NOTMR* version of it⁷. The *NOTMR* is an option available for the designer which does not add redundancy and also guides the future optimization tools to not protect that area since the user is stating that it is not needed.

The figure 37 also provides the macros for the attributions, which should replace the normal usage of the attribution operator in HDLs when the designer needs to perform value changes, in this way the compiler will use the adequate signal in each case, for example, the TMR voter output or the corrected output bit in case of an encoded bus.

To clarify the macro insertion procedure, a simplified application example is presented in the figure 38. At the left, a $N = 32$ bits counter is coded and, at the right, its

⁷ Arild Velure and the ALICE experiment electronics coordinator Alexander Kluge have strongly contributed in respect to definitions, coding and redundancy in SAMPA project.

```

// The TMR register definition
`ifndef REMOVE_TMR
  `define TMRINST(HIGH,LOW,NAME) reg [HIGH : LOW] NAME
`else
  `define TMRINST(HIGH,LOW,NAME) wire [HIGH : LOW] NAME;
  reg [HIGH : LOW] NAME``_TMR[2:0];
  voting_nbit_3reg #(.SIZE((HIGH)-(LOW)+1)) NAME``_voter
    (.A(NAME``_TMR[0]), .B(NAME``_TMR[1]), .C(NAME``_TMR[2]),
     .out(NAME))
`endif
// The NOTMR register definition
`define NOTMRINST(HIGH,LOW,NAME) reg [HIGH : LOW] NAME

// The Modified TMR assignment
//   to be used in place of Verilog attribution
`ifndef REMOVE_TMR
  `define TMR(NAME, RANGE, ASSIGNMENT) NAME RANGE <= ASSIGNMENT
`else
  `define TMR(NAME, RANGE, ASSIGNMENT) { NAME``_TMR[0] RANGE,
    NAME``_TMR[1] RANGE, NAME``_TMR[2] RANGE} <= {3{ASSIGNMENT}}
`endif

// The NOTMR assignment, the standard Verilog attribution
`define NOTMR(NAME, RANGE, ASSIGNMENT) NAME RANGE <= ASSIGNMENT

```

Figure 37 – The TMR macro.

<pre> 1 2 3 4 // A 32 Bit Counter 5 module counter32(clock, clear, qout); 6 7 // Ports 8 input clock; 9 input clear; 10 output [31:0] qout; 11 12 // Regs 13 reg [31:0] cnt; 14 15 always @ (posedge clock) 16 begin 17 if (clear) 18 cnt <= 32'd0; 19 else 20 cnt <= cnt + 1; 21 end 22 23 assign qout = cnt; 24 25 endmodule </pre>	<pre> 1 `include "voting_nbit_3reg.v" 2 `include "tmr.v" // defines TMR macro 3 4 // A 32 Bit TMR Counter 5 module counter32(clock, clear, qout); 6 7 // Ports 8 input clock; 9 input clear; 10 output [31:0] qout; 11 12 // Regs 13 `TMRINST(31,0, cnt); 14 15 always @ (posedge clock) 16 begin 17 if (clear) 18 `TMR(cnt,, 32'd0); 19 else 20 `TMR(cnt,, cnt + 1); 21 end 22 23 assign qout = cnt; 24 25 endmodule </pre>
---	---

Figure 38 – Example of the TMR macro usage in a counter.

triplicated version, using the proposed macro approach is presented.

It is possible to verify that only minor changes are needed in the codification style and, with this, a great standardization occurred in the TMR addition procedure. These facts can help to considerably facilitate the job of the designer and also provide well defined structures that can be parsed by softwares and scripts.

The same macro based approach can be applied to other kinds of redundancies and protection schemes; in this work, some extra macros were developed increasing the options for the designer or the optimizer. The basic alternative was the TMR already shown, but as it does not protect for multiple bit errors, the penta modular redundancy

(PMR) macro was included, where a quintuplication occurs if needed, as in an important or very sensitive block. In PMR the redundancy can recover up to two errors per PMR.

The TMR, PMR and upper levels of replication can be very area hungry and as an option to that, a new macro set was included, not basing the protection on replication but now in encoding, being named as hamming modular redundancy (HMR). In this case, there are extra bits added using hamming encoding (SKLAR, 1995; PROAKIS, 2001) in a way that an automated inserted recovery block can correct up to one bit error per hamming encoded block (SKLAR, 1995).

The HMR set has several options and they are identified by an integer stating the number of parity bits starting as low as HMR3. The amount of added extra bits strongly depends on the encoding used and the signal being protected, where the bus size is an important parameter. As an example, HMR4 can protect a signal of up to 11 bits by adding 4 bits of redundancy (using hamming(15,11) code), and extending the redundancy bits by one, HMR5 can protect signals up to 26 bits of length (using hamming(31,26) code) (SKLAR, 1995; PROAKIS, 2001).

The above examples illustrate that with extra macros several possibilities can be selected, enriching the search space for the design, but also needing more effort to find an optimized balanced solution for large projects. This motivates the creation of an automated optimizer to ease this task being this the target of the next section.

Before going to the optimizer description, as a complement to the cited implemented redundancy macros, an alternative set of protection options will be addressed using a connection to an external tool know as triple modular redundancy generator (TMRG) (KULIS, 2017).

TMRG is a tool created by Kulis (2017), in CERN Electronic Systems for Experiments (ESE) group at the microelectronics section at a date after the release of SAMPA. This custom software has as its main purpose the automation of the process of triplicating digital circuits, freeing the designer from manually introducing the TMR code at the implementation stage (KULIS, 2017). The tool only helps to insert the triplication and has no connection to decisions or optimizations; it is a nice operational tool that aim to simplify the massive tasks involved in manual triplication.

TMRG also helps to ensure that triplicated logic is maintained through the electronic design automation (EDA) design flow if specific recipes are followed. Finally, the tool still streamlines the process of introducing SEE in digital gate level simulations for final verification and sensitivity testing (KULIS, 2017).

The tool also extends the possible redundancy options including the combinatory logic in addition to the registers and memory elements, which may open several other alternatives and important situations for the optimizer.

Figure 39 will be used as a reference for this analysis where (a) shows an initial combinatory logic block with non triplicated inputs and outputs. If there is enough area and the blocks around it are going to be triplicated, one possible applicable solution is shown as (b). In this case, the logic and its interfaces are fully triplicated providing a high level of protection. Figure 39 (c) also shows an interesting situation, still supposing that the blocks around will be triplicated but this block in specific will not, in this way, the inputs are decided via majority voter, sent to just one instance of the block and then the outputs are triplicated.

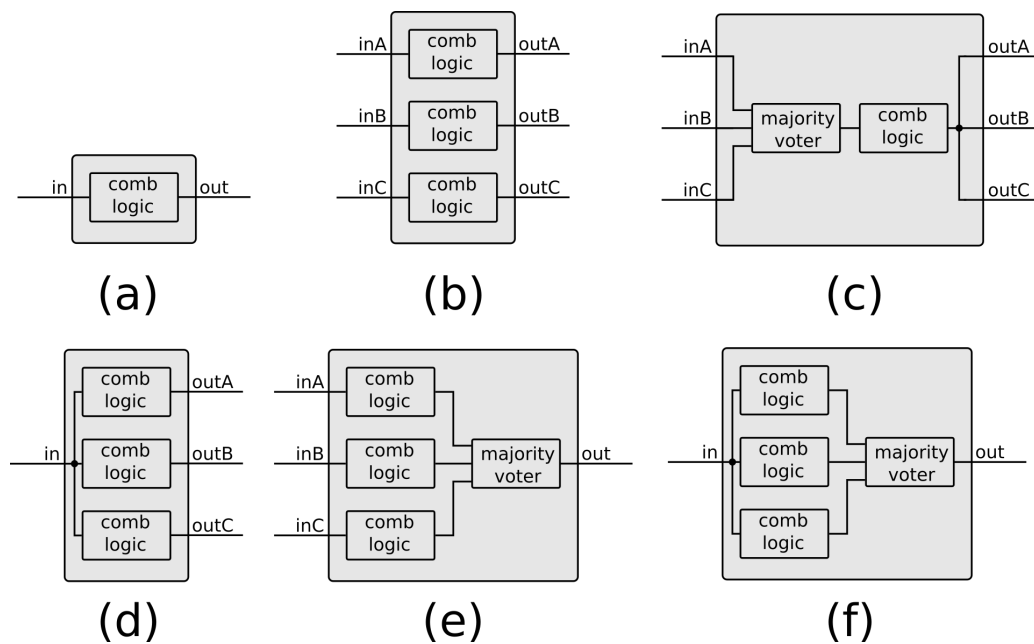


Figure 39 – Several alternatives for TMR and its connection in combinatory logic blocks.

Source: Adapted from Kulis (2017).

The following cases refer to situations where some of the blocks around are not going to have their interface triplicated. Figure 39 (d) illustrates one possible implementation when there is non triplicated inputs and triplicated outputs are needed. Figure 39 (e) does the opposite, where due to the lack of triplicated outputs, a set of voters may be added. Finally, figure 39 (f) presents a triplicated logic implementation for a block in the middle of non-triplicated interfaces. The last case (f) can promptly replace (a) without changes in the neighbors.

Another relevant choice to be done in the design protection is the interconnection between the sub-blocks. Figure 40 shows alternatives for voter insertion in this case. Figure 40 (a) illustrate a simple interconnect which can be transformed in to the one in figure 40 (b) after triplication. To add extra protection to SEEs, a voter is added recovering each of the possible signals from the other two and properly refreshing the triplet of values before entering in the next block.

Now analyzing the case of the transformation from Figure 40 (c) to Figure 40 (d),

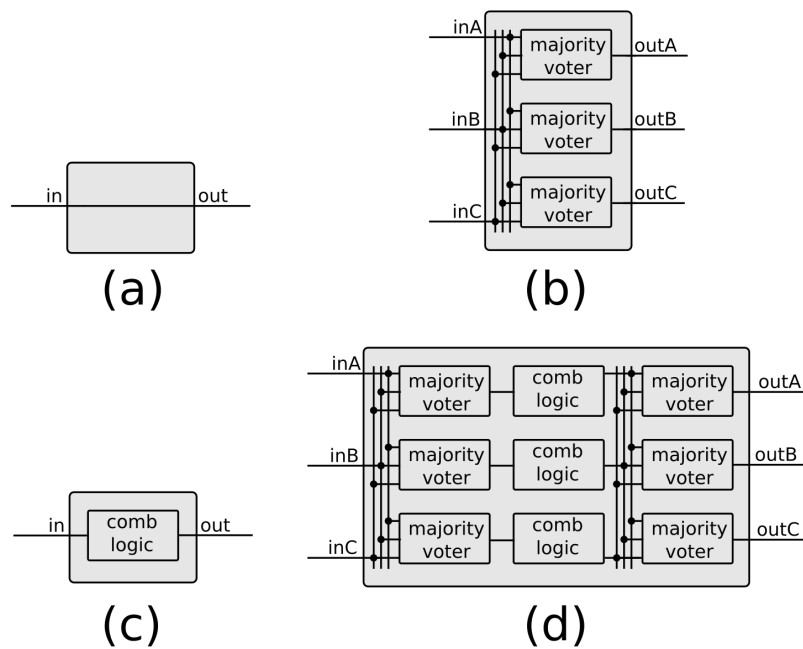


Figure 40 – Comparisons between some alternatives for connections and voting.

Source: Adapted from Kulis (2020).

it is possible to recognize a similar pattern from the protection provided from figure 39 (a) to figure 39 (b), but now inserting a set of majority voters around it, as in figure 40 (b), reducing the chances of error propagation in the logic, by filtering it as soon as possible.

Finite state machines are also very important elements to be protected and figure 41 compares some of the available options. Figure 41 (a) shows a simplified view of a state element with combinatory feedback, but without any protection. One possible action for improvement is shown in figure 41 (b), where the full initial block is triplicated. In this case, it is assumed that the blocks around have also triplicated interface.

Unfortunately, the solution in figure 41 (b) may not be protective enough as there is no feedback between the finite state machine (FSM) replicas and SEE errors may persist without being corrected. With some extra area, a better solution can be used, with inter FSM voters. Figure 41 (c) shows a modified version of figure 41 (b) including voters preceding the memory elements, where a single error in the next state logic can now be filtered using the other two branches.

Figure 41 (d) and (e) show alternatives for situations where the interface to the block is not going to be redundant. In this case, one relatively cheap alternative is to replicate just the state registers and vote its outputs. Figure 41 (d) shows a possible implementation (KULIS, 2020). As only the memory elements are protected, a single event transient in the voting element or in the combinatory logic may cause unfixed errors that may propagate to other blocks.

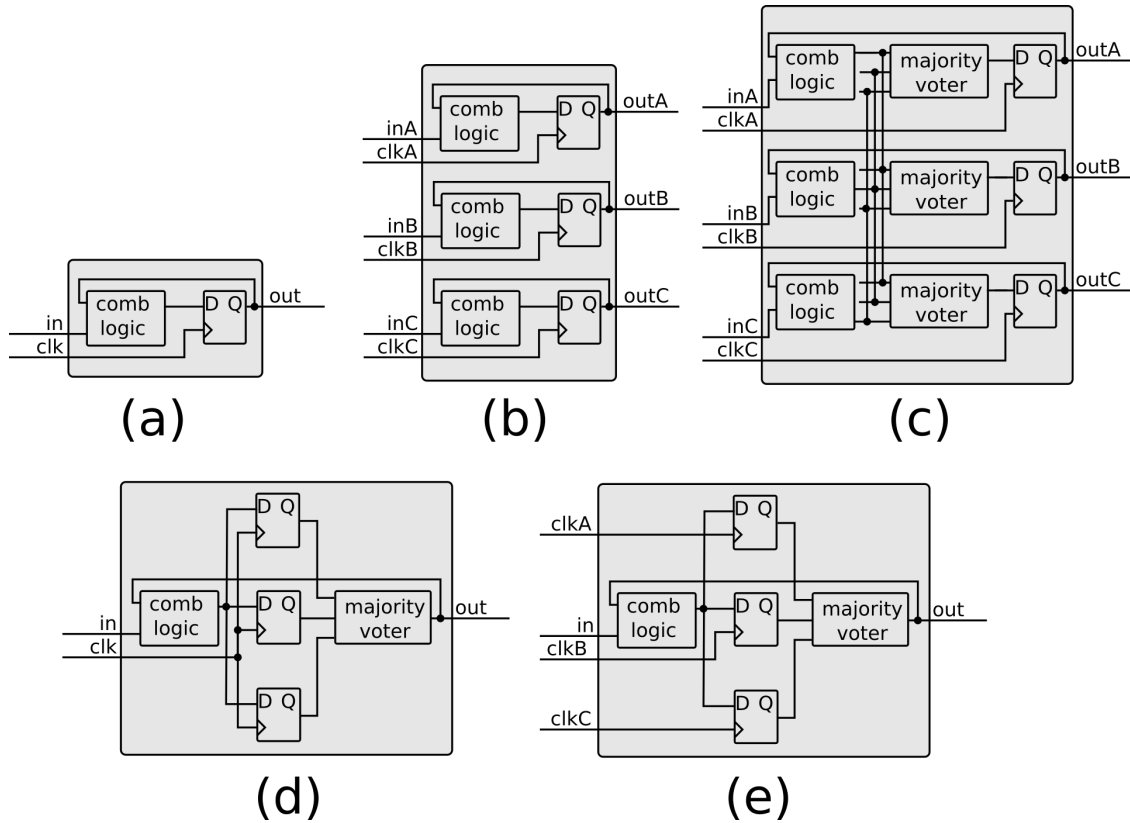


Figure 41 – Implementation of redundancy in finite state machines.

Source: Adapted from Kulis (2020).

In a way to mitigate these errors, figure 41 (e) shows an alternative using replicated clock domains. These clocks may have skew or phase differences providing redundancy in time and possible filtering transients due to the smaller chance of a transient occurs in two different moments.

Figure 41 (e) has also additional vantages due to the clock redundancy, but on the other hand, it is harder to implement and error prone in the physical implementation. The additional two clock domains waste extra power and area and may cause overheads in systems with several modes of operation as SAMPA, which uses multi mode multi corner (MMMC) analysis and implementation (CADENCE, 2019).

Several alternatives have been proposed using the developed macros and, as described in this section, TMRG is also a relevant automation tool for redundancy insertion in the code, but both solutions only aim in changes in the sources and can not choose the proper combinations or evaluate metrics to meet design targets. In this way, design experience and proper guidance are needed, where these tools are not closed solutions for design protection (KULIS, 2017; KULIS, 2020).

Digital systems like SAMPA can have hundreds to thousands of blocks and each one of them may have several protection options and tradeoffs; these facts can create strong difficulties for the designer to choose between the alternatives. In this direction,

the next section addresses an optimizer to help the search for solutions in this enormous problem space.

3.4.3.2 The optimizer

Suppose that a compilable HDL code was developed and a designer wants to add protection to single events in this solution. There are several redundancy options available and it is hard to manually implement and evaluate that set. A possible way to ease this process can be based on a software that parses the HDL code, mapping possible points to apply changes or include the proposed macros and test the proposed solutions.

The changes can be in several levels but one common option should be to protect or not, and also choices between the level of redundancy to apply, like single bit correction per bus, triplication or more.

These operations may be in opposite directions on several of the initial power and area usual constraints (minimization) and, in this way, optimization problems can be stated. One possible problem can be: maximize the protection while respecting the area and power limits. Or other alternatives like, satisfying the error rate while minimizing the power and satisfying the area. Many other options depending on the design can also be the case.

These multiple possible scenarios along with designs including several blocks of different sizes, speeds and bus widths really push to a solution based on automated algorithms.

The main point is that with a big amount of blocks, registers and options to change, along with the fact that the solution is not analytic or closed form, it makes extremely difficult to find a static solution for that, and in this way, artificial intelligence algorithms were elected as a strong candidate for the optimization in question.

Also, since each single candidate solution there is the need of building the synthesized hardware schematic to create an estimation of the area and power with the technological information, the outputs are really problem sensitive, non-linear and bad-behaved.

To complete the scenario, the input variables are discrete and in majority, sets of options for the internal redundancies. This makes algorithms for continuous inputs possibly behave poorly, which directed this work to the use of evolutionary algorithms based on discrete chromosomes as the preferred solution for this optimization problem.

In this work, genetic algorithms were selected due to good performance on discrete non-linear problems and also because of their strong capacity to move out from local solutions using mutation (MELANIE, 1999; SIVANANDAM; DEEPA, 2008).

With this choice, the first step is to transform the problem into a representation

expected by the optimization algorithm and build the evolutionary loop, defining operations to feedback fitness information for next generations and selections (SIVANANDAM; DEEPA, 2008).

The problem in question is composed of an HDL code, a set of constraints and a fitness function that should return how good a solution is with respect to the others. This function also can be written aiming to minimize some design output variable or result.

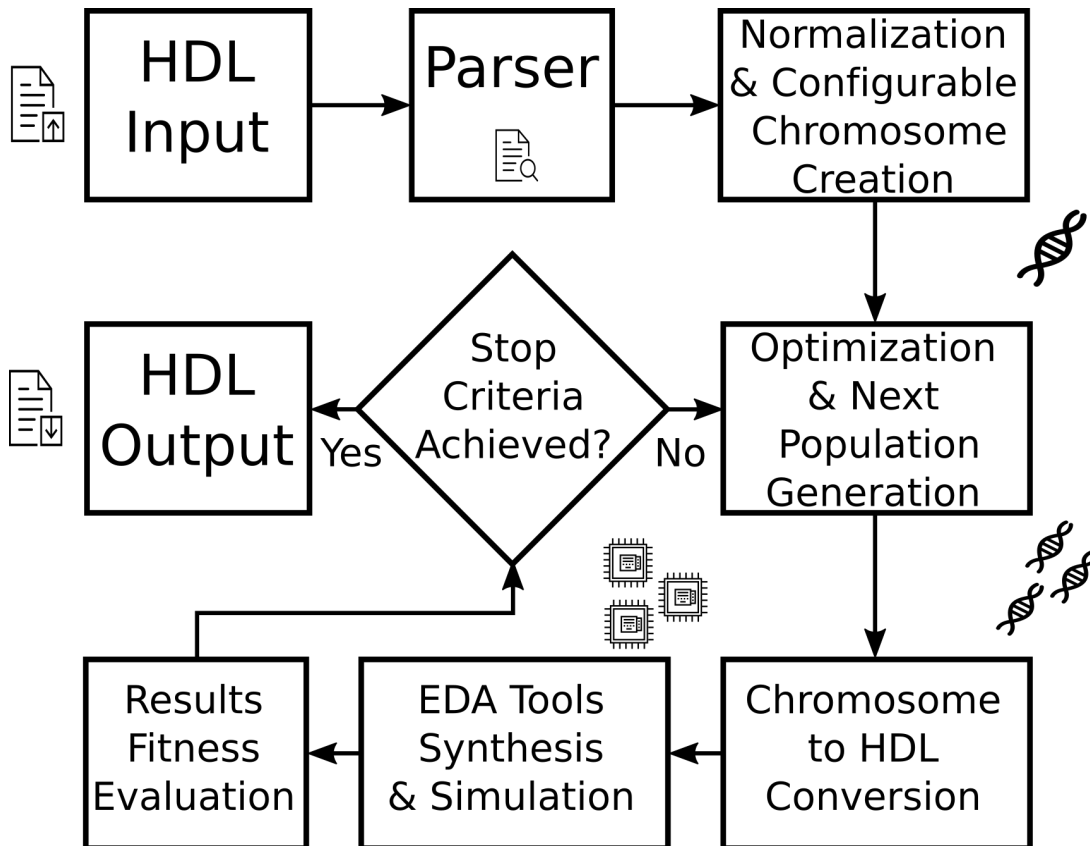


Figure 42 – Block diagram of the proposed optimization loop.

Figure 42 shows the block diagram of the proposed optimization flow. It starts with the HDL source inputs which go to a parser that identifies the possible redundancy insertion points. This set of detected entities will be evaluated and the applicable redundancy options will be listed (for each location).

With the problem information defined, it is possible to enter in the chromosome creation block. In this step, the problem will pass through a normalization operation which will define a mapping between the problem and the chromosomes within a conversion function.

This step is based on composing a full chromosome by concatenating smaller genes, where each gene will be linked to a specific part of the design, controlling its implemented protection level.

A possible simple example can be done using the code in figure 38, which provides

a 32 bit counter. Suppose that a hypothetical target design has three 32 bit counters, the first and the last one are involved in noncritical tasks and the middle one is a crucial part of the system and must have a very low fail rate.

Consider also that for the 32 bit counter, the detected redundancy options for the single register group were TMR, PMR and HMR. HMR must properly encode the full range of the 32 bits, using HMR6 or bigger. Also, a relevant option is to not include redundancy, so composing a total of four alternatives, as mapped to binary coded genes in table 6.

Table 6 – Redundancy to bits mapping

Redundancy Option	Encoded Gene
NOTMR	00
HMR	01
TMR	11
PMR	10

Table 7 shows some examples of applications of table 6 encoding. The full chromosome is the concatenation of each sub-block gene. The first line shows the case of the three counters not going to be triplicated, the second line shows the design being fully triplicated, the last two lines show cases where the central important block will be implemented with PMR (quintuplicate registers). It is important to note that these are just examples.

Table 7 – Example of chromosomes for the set of counters

Example Case	Counter 1 Gene	Counter 2 Gene	Counter 3 Gene	Chromosome
Fully unprotected	00	00	00	000000
Full TMR	11	11	11	111111
HMR PMR HMR	01	10	01	011001
TMR PMR TMR	11	10	11	111011

With the chromosome mapping and encoding defined, it is possible to go to the population generation step where an initial random population of chromosomes will be created using the information from the parsed source codes and available redundancy options.

The proposed HDL represented by each chromosome will be sent to a working directory and synthesis tools will be run to obtain a gate level netlist and satisfy the timing, electrical and technological requirements (for every single individual in the population).

This step is very computational intensive and may take from several seconds to days in large designs like the full 32 channel SAMPA. The synthesis procedures ran in this work were based on commercial state of art softwares from Cadence, using the Encounter, Genus and Innovus implementation flow (CADENCE, 2019).

After the EDA tool flow has been concluded, it is possible to process several of the involved logs and reports. Also, with the parsing of the resulting gate level netlists, variables and metrics can be obtained, being finally fed to a fitness function.

The fitness function will return a real number representing the fitness qualifier for that solution, which may be calculated using several aspects from the output design including power, area, timing, simulation results and also single event tolerance.

This function is fully configurable and, in the present work, it has been chosen as a mix between area and power, where the area was weighted by 60% and the power by 40%. Additionally, to include the influence from the single events the function also implements a penalty factor, which is calculated using the computed faults in radiation tolerance.

This penalty factor is obtained using a set of testbenches and simulations that are run with the resulting implemented gate level solutions of the EDA tools. After the solution is built, Mentor Graphics Modelsim (Mentor Graphics Corporation, 2016) is called and after a reference simulation, other simulations are run including fault injection of several kinds including single events and multiple bit errors. At the end, the results are accounted and the designs with smaller tolerance receive bigger penalty factors, which reduces the fitness of that individual in the population.

Creating populations of solutions and further qualifying them makes a way to elect the best individuals; with these individuals it is possible to generate candidates for a new generation of solutions.

The next generation is based on chromosome mating (recombination) and mutation performed over selected individuals from the last population. The selection operates in a way to prioritize the best adapted chromosomes (HAUPT; HAUPT, 2004). The newly created chromosomes can then fill a new population pool which should be evaluated again (SIVANANDAM; DEEPA, 2008).

The implemented algorithms also include an option to carry a part of the best fitted individuals directly to the new population. This quantity is configurable and usually set as a small number, near four.

Repeating these procedures for several generations can improve the best fitted chromosome (HAUPT; HAUPT, 2004; SIVANANDAM; DEEPA, 2008). This best adapted individual also represents the desired optimized solution, which at the end can be converted back to HDL and used in the real world situation, solving the proposed optimization problem.

The next section will address details of the genetic algorithm operation and variations of the execution to support other flows.

3.4.3.3 Genetic algorithm details and extensions

At each generation, the genetic algorithm performs mutations and cross-overs with the population individuals, but these operations may not happen, being governed by probabilities known as p_m and p_c , the mutation and cross-over probabilities respectively.

The behavior and search path of the algorithm are related to the values of these probabilities, as for example, bigger values of p_m tend to increase the chance of the algorithms get out of stuck local maximums, and several other possible scenarios for the probabilities, problems and fitness functions.

For this work, the selected values for these probabilities were $p_m = 0.00175$ and $p_c = 0.3$, defined after a deep research over these parameters, where moderate high initial cross-over rate was chosen for faster initial convergence.

This work also included modifications in the genetic algorithm, implementing dynamic parameter selection strategies for p_m and p_c . These techniques aim for both convergence and final solution refinement in the same evolutionary run.

The algorithm was run in 3 phases and controlled by a finite state machine. This machine was responsible to manage the dynamic p_m and p_c selection and the phase transitions.

In the initial phase, the algorithm sets the default parameters p_m and p_c (as cited before) and starts to evaluate the conditions for a state change. These conditions are based on 3 variables: the number of generations, the standard deviation of the population fitness and the rate of improvement achieved in the last runs.

The state machine will proceed for the next phase if a configurable number of iterations have been run or the population is not well spread or the algorithm ceased to improve the output fitness.

Phase 2 increases the p_m aiming to spread the solutions and explore the search space again and try to unlock some chromosomes from local maximums; optionally the p_c can also be changed. Phase 2 is not mandatory and may be bypassed directly to phase 3.

Phase 3 is reached if the algorithm runs for enough time or if the improvement rate achieved one specified threshold range. This phase is focused on solution refinement around the obtained designs. To allow this refinement to settle, the p_m and p_c are reduced and the genetic algorithm is run up to its end.

The stop criteria used here is also based on multiple criteria. These include a maximum number of generations, a threshold value for the best fitness value and the continuous evaluation of the solution improvement. If the algorithm detects that no gain happens for a predefined amount of time, the optimization is finished.

Following the described definitions, the genetic algorithm has achieved practical

results while it was simply integrated into the design environment, easing the interface with the system designers.

The next section will address several final specific cares, taken and recommended here to other designs aiming for success in real silicon implementations with radiation tolerance.

3.4.3.4 Topics on the back-end design

The back-end implementation of a synthesized HDL design can be performed in distinct ways aiming to improve the tolerance to errors caused by radiation. One approach can be based on the usage of hardened cells, while others may rely on the redundancy and strategies inserted in the HDL, where the final implementation can be done using foundry distributed standard cells.

Hardened cells are usually larger and maybe slower than the default versions normally provided by the foundries; also these cells may not be so well characterized. Several processes do not have these cells available or restrictions and legal issues can be a deterrent, implying in costs, delays and project cancellation.

This reinforces the advantage of using the standard cell redundancy approach, as in this work. The foundry cells are already validated and usually have good speed versus area balance, but this approach triggers the need of extra verification.

The logic synthesis and layout are in general processes based on automated softwares which rely on logic conversions, Boolean algebra and logic minimization. The redundancy added in order to prevent errors can be accidentally removed by the minimization steps in these softwares, making the system vulnerable without being noticed.

Is also important to cite that the TMR cells and modules can be modified by timing optimization, changing its behavior and possibly reducing the protection.

Depending on the design needs, the clock and reset trees may also be triplicated. If this is the case, the process needs to be properly monitored and guided during the back-end design flow, verifying the connection of each triplicated leaf to one clock domain. This multiple tree approach can prevent that single event transients on the clock or reset pass into all the subsequent sequential logic replicated cells, avoiding a considerable amount of errors.

Another relevant point is that timing and logical design failures in redundant structures do not appear at simulation, if they occur only in one branch of the system. In this way, the testbenches and validation will need to take special care over this topic. Some alternatives are the inclusion of specific assertions and the monitoring of back annotated standard delay format (SDF) timing warnings and violations, but other techniques and softwares may also be needed.

The designers should take measures to prevent all these pitfalls, and in a way to contribute to future works, it is possible to suggest some of the actions taken here as recommended procedures that are cited in the following list:

- Behavioral and structural verification
- TMR aware timing analysis
- Check for the presence of triplicated blocks and flip-flops
- Check for the correct wiring of the clock/reset trees
- Parsing the netlist with scripts for cross-check
- Execution of formal verification tools
- Fault simulation and injection
- Functional impact of tolerated SEU
- Radiation testing as a final and qualifying metric

There are also post-manufacturing questions involving systems with protection implemented with hardware redundancy. Behavioral testing procedures may classify that a chip works perfectly fine, even if it has errors inside the logic. This may happen because it is possible that faults in the circuits like shorts, opens or transistors with wrong specifications occur in just one branch and the protected block may have several similar redundant branches.

In a scenario like this, the subsystem may probably work, and even without any apparent problem. But when the device is exposed to an environment with radiation, it can possibly suffer from single event upsets or transients and in this way the device may fail with just one bit error, even if it had additional protection or redundancy.

These errors can happen because one or more of the redundant blocks was already faulty from manufacturing and the faults along with the error caused by radiation may generate real perceptible failures, propagating through the system and possibly generating functional interrupts and bigger problems.

Thus it is relevant to notice that the implementation of testability structures using design for test (DFT) is critical in chips with redundancy based protection and even more in one design which will have engineering runs with mass production like the SAMPA chip.

All SAMPA engineering runs had design for test scan chains, along with memory self-test to help the validation and to ensure, with a high coverage, that the system was manufactured correctly.

Our work (DE CARVALHO *et al.*, 2018) was developed targeting the SAMPA testing, including the presented types of redundancy based blocks. The paper described an in house low cost automatic test equipment with of the shelf components as a solution to check the SAMPA internal digital circuits, even considering the added redundancy. The vectors used for testing the design were generated using professional tools including Cadence Modus and Cadence Encounter Test, achieving a good DFF coverage of about 98% and being able to detect about 92% of the possible manufacturing faults in the design which had more than 125 thousands flip flops and 15 million nets.

The next section addresses strategies discovered during this work aiming to reduce the latch-up cross-section of the device.

3.4.4 SEL investigation and avoidance

SAMPA V2 tests showed that the chip was operational and provided promising results in relation to the system specifications (BARBOZA *et al.*, 2016; ADOLFSSON *et al.*, 2017), but unfortunately its tolerance to single event latch-ups was not enough for the application (MAHMOOD *et al.*, 2018; MAHMOOD, 2020), creating the need for an investigation over this topic.

This section aims in the search for the root cause of the latch-ups and also in presenting alternatives to solve the problem. Additionally, an approach for detecting this kind of problem is discussed, even in pre-tapeout phase and before radiation tests were used for evaluation.

In the case of SAMPA V2, the problems happened in practice (MAHMOOD, 2020) and with the irradiation tests results, several characteristics of the latch-up events were observed including some discrepancies that can help to find the faulty block.

First of all, current jumps were measured and they did not occur a single time per device, but the events happened eventually in sequences, usually spaced in time. Also it is important to cite that the current consumption has possibly a stair format due to the fact that several latch-ups may happen and they are cumulative in terms of current.

Another very interesting observation is that the current jumps do not seem to interfere very importantly with the functionality of the standard cell based blocks, including state machines and combinatory logic. The current jumps happened in several operational modes not showing a big correlation with the logic behavior or configuration.

The chip remained fully operational and readout could be made even during the latch-ups, a fact that made possible the usage of global and per channel register units to monitor and reevaluate the memory cross-section in run time.

An important fact was then obtained, the single port memory used to implement

the baseline correction filter pedestal memory was having fluctuations in its single event upset cross-section (MAHMOOD, 2020).

The cross-section of the pedestal memory was larger than the standard linear expected behavior with increasing fluence levels and it showed higher error rates in a not repeatable fashion. This was very unexpected with respect to the initial cross-section estimation, where no current jumps happened.

These facts drew attention to the SRAM memory. This memory was implemented with an IP block, used in this case to implement the memory needed in several blocks of the ASIC with increased area efficiency.

It is also relevant to state that current events like the measured in SAMPA V2 have not happened in SAMPA MPW1 and in that time no IPs were used, just standard cells, increasing the chance of the single port SRAM IP be the guilty block.

With these evidences, a possible next step could be to check and deeply inspect the implementation of this SRAM, but there is an additional problem; there are no layouts available for this kind of IP block, being then assembled in the foundry tape-out steps by external agents trusted by the IP provider.

This kind of implementation hiding agreement is quite common and can happen from blocks at HDL level (for encrypted sources) going up to the black box ones like the specific memory IPs discussed here. The question then is how to continue this investigation without knowing the internal circuit and the layout of the IP blocks.

Due to these facts the present section was prepared⁸, focusing on the proposal of a practical interactive process that can be applied to discover relevant information of the latch-up questions even not having the block layout.

The latch-up is an event that happens on the substrate and it is strongly correlated to parasitic structures due to the proximity of the transistors. In these places, an ion strike can possibly trigger the PNP device (RABAEY; CHADRAKASAN; NIKOLIC, 2003; NICOLAIDIS, 2011) causing intense current jumps.

These observations triggered the idea of inspecting the parasitic resistors that may influence the SEL occurrence. These also can be used as a parameter of decision or metric to decide which part of the ASIC is more sensitive.

The question then is how to deal with this comparison considering that there is no accessible layout of the devices. The very simple answer to this question is one important aspect for preventing this defect before the submission for tapeout.

The users can not see what is inside the IP black box, but the trick is that it was

⁸ In this direction an intense research was made by the author and the ALICE electronics coordinator Alex Kluge with technical feedback of Ronaldo Wilton. This research focused on the root causes and in alternatives for a methodology to state a candidate for being the SEL source.

possible to run design rule checks in the full design when in pre-submission stage, which include the IPs (at foundry side). Designers may change the design rule decks to target and point over regions with specific characteristics that could be more sensitive to SEL.

The remaining decision is which design rule to edit and what are the reasonable ranges of values that they should possibly have to increase the tolerance to radiation.

To address the above question, it is important to remember that the latch-up has a strong relation to the parasitic resistance in the wells and substrate (RABAEY; CHADRAKASAN; NIKOLIC, 2003). In this case, one viable rule would be related to the maximum acceptable distance to the contacts, which strongly influences the resistance values.

Fortunately, standard latch-up prevention is already a known practice and is part of the verifications that the foundry and process developers possibly do before releasing it to the users.

In the case of TSMC, test devices are verified following the specifications defined in Joint Electron Device Engineering Council (JEDEC) JC-40.2, which contains several procedures including over-voltage and over-current stimulus.

To stress even more the tests are done both at room temperature and at 125°C. The technology in question was approved and it is also widely used without latch-ups in standard non harsh environments.

From the foundry defined process design rules, there are almost two dozens of checks targeting latch-up preventing (LUP); inside this rule-set, one specific guideline was found to be very relevant for the analysis of the single event latch-up problem.

This specific rule is called LUP six, it guides the DRC verification tool to search for any point in an NMOS source or drain to a P well polarization contact (in the same P well) exceeding an arbitrarily defined distance δ .

Likewise, there is the PMOS version of the rule, which is also included in LUP six. It states to search for any point in a PMOS source or drain to an N well polarization contact (in the same N well) that may exceed δ distance.

In this way, the foundry controlled the resistances involved and successfully delivered millions of chips in this technology, but the problem is that in case of the single events, one external agent deposit extra energy in the thyristors and the resistance should be smaller, to prevent latch-ups.

The standard foundry defined rule uses a quite large δ distance having tens of microns as the smaller limit for the contact distance. Also, an aggravating factor was found in the case of SRAM IP latch-up problem, where targeting for more area efficiency, the IP and foundry process developers made an exception to this rule. This exception allowed

the increase of the LUP six tolerable value in more than 33% in mask regions denoted as SRAMs.

In the search for the guilty block(s), one good automated parameter was found to be used as a guide and a suspected SRAM IP block was elected to be inspected carefully due to its LUP exceptions found.

The following step taken was the evaluation of the LUP six design rule for a design that has successfully passed through the irradiation tests without latch-ups, the SAMPA MPW1.

The MPW1 test chip 3 had a digital core and this was fully made using standard cells. This is the same approach used for the part of SAMPA V2 digital core that was not composed by IPs, so with this test the base building blocks are checked.

Aiming in validating the proposed DRC based search, the design was evaluated for a series of decaying δ values from 20 μm to 700 nm trying to discover where the DRC tools would trigger errors. This could indicate thresholds for the distances used in the substrate contacts layout. It is also important to note that for all the fabricated designs there were no errors in the default foundry DRC checks, so any newly detected fault will be exclusively caused by these proposed deck changes.

Table 8 shows the compiled results for the standard cells evaluation at decaying values of δ . It is possible to see that the MPW1 had no violations for the cases where distances to the contacts were larger than a micrometer. The table also exposes the polarizing scheme in the decoupling capacitors cells, but as their δ is smaller than the majority of the standard cells they will not be further mentioned.

Table 8 – Compilation of the LUP six violations for the standard cells

δ in LUP [μm]	Default	20	15	10	5.0	2.5	1.0	0.7
STDCELL Violations	no	no	no	no	no	no	yes	yes
DECAP Violations	no	no	no	no	no	no	no	yes

The proposed technique successfully returned a reference δ range for the MPW1 chip 3 and this chip had not presented single event latch-up sensitivity in its previous irradiation (MAHMOOD, 2020). With these facts, one viable option should use the discovered δ range as a comparison metric with respect to the characteristics of the suspected SRAM IPs. In this direction, a new test set was made and ran for the SAMPA V2 layout⁹.

This implementation has used 130 SRAM memory IP instances with custom 10 bit wide buses, requested to better match the application in question. From these memory

⁹ Thanks for Ronaldo Silva and IMEC for the strong collaboration and patience in these verifications.

blocks, 32 are based on 6 transistor cell single port memory IPs and the other 98 are 8 transistor cell dual port SRAM IPs.

The most relevant IP with respect to area occupancy and number of instances in SAMPA is the dual port SRAM memory. As this is the most common it will be analyzed first, as the probability of problems appear could be bigger if it is the root cause.

Table 9 shows that in dual port memory IP the contacts are more distant in comparison to the reference stated by the MPW1 standard cell design. However, the increase in the distance is only in the order of very few micrometers.

Table 9 – Compilation of the LUP tests for dual port SRAM

δ in LUP [μm]	Default	20	17.5	15	10	5.0	2.5	1.0	0.7
Violations	no	no	no	no	no	no	yes	yes	yes

The dual port IP has some differences with respect to the standard cell δ , but for completeness, the other IP type should be also evaluated. This IP is used in the low frequency domain as the pedestal SRAM memory and it is single port with 10 bit data width. This memory is used by the baseline correction 1 digital filter.

Table 10 reveals the impressive results obtained for the single port SRAM memory IP, where clearly a strong difference appeared; the block presents a δ distance in the order of ten times the one found in the initial reference estimation at MPW1 (full standard cell based design).

Table 10 – Compilation of the LUP tests for single port SRAM

δ in LUP [μm]	Default	20	17.5	15	10	5.0	2.5	1.0	0.7
Violations	no	yes	yes	yes	yes	yes	yes	yes	yes

This larger distance is an important metric to complement the evidences and to help to state with more confidence that the guilty block is the per channel single port SRAM pedestal memory IP at BC1 filter.

It is worth observing that for the IP developer, it makes sense to have bigger δ distances (just barely respecting the rules) in this block as it is an important metric for technological advance, and IPs of this kind are in general blocks targeted for area efficiency. In the normal cases of use excessive substrate contacts will use extra cell area which could be used to implement more memory cells, but in an environment with radiation, this economy has shown to increase the single event latch-ups cross-section which may cause unacceptable losses for the users.

To conclude this section it is possible to state that the probable source of the SELs was the pedestal memory, which was the set of IPs with a clear difference from the others

in respect to the proposed evaluated parameter. The SAMPA V2 has approximately one quarter of its memory blocks implemented with the suspected IP, one per channel which may make the problem even worse, as the chip may have a bigger probability of having at least one memory with latch-ups, or even more than one at the same time stressing the power grid.

In order to continue this work and provide an ASIC resistant enough for the application in CERN, corrections were made and the suspected IP was removed. The single port block was replaced by a dual port alternative requested by this author. The resulting work generated a new version of the digital core which is used in SAMPA V3 and SAMPA V4. The measurements and irradiations of these chips are some of the main targets of the next chapter.

It is relevant to register that with the latch-up avoidance knowledge from this proposed methodology, one foundry MLM tape-out run could have been reduced, impacting in hundreds of thousands dollars savings.

The project time schedule was also a critical point in question which could had much more safety slack in case of these latch-up problems had been detected and solved before SAMPA V2 submission.

It is also important to cite that at least two other designs at CERN could have these facts as design advices where these findings may already had shown its contributions, for example in the CMS detector¹⁰, where the VFAT3 chip team states the importance of the memory IP selection and cites the detected latch-up fragility as an important turn point for newer runs (ROSA, 2017).

¹⁰ CMS is one of the four big CERN LHC experiments (as ALICE). CMS was the detector which identified the Higgs boson signs back in 2012.

4 Results and radiation tests

The present chapter will be divided into two main parts, the first will follow the SAMPA development path along with its results and irradiation tests. The second part will address measurements and analysis made over selected blocks chosen as a proof of concept for the optimizer proposed in this work.

The SAMPA project had many fabricated prototypes during its design. It was initiated by a reduced version in MPW1, passing through SAMPA V2, SAMPA V3 and SAMPA V4 which was the final version accepted to be used in CERN. Further, two additional versions have also been fabricated extending this project to other detectors, the MPW5 and finally SAMPA V5.

Aiming to check the applicability of the project, irradiation runs were performed in several of the prototypes, where these test results and their analysis will motivate most of the further discussions made in this work.

The main objective is to state the proper operation of the device in the experiment and also to validate this work. The results and irradiation procedures were made in partnership with Pelletron¹ and ALICE² collaboration. Here a considerable part of the measurement procedures involved will be compressed aiming to be concise as this thesis is focused on the digital signal processor development and in correlated methodologies.

4.1 SAMPA MPW1

The first prototype irradiated during this work was known as SAMPA MPW1 chip 3. This design was submitted with two other chips in middle of April 2014, being the dies fully produced in early August. The initial irradiation campaign was planned to occur after the functional tests made by this author at CERN which ended in February of 2015.

These tests in conjunct with the performance evaluation of the front-end were positive, showing a substantial agreement with the experiments requirements. Our paper Barboza *et al.* (2016) addressed the system architecture and have shown the measurements of this first prototype.

¹ Additional thanks to the great help of Physics Institute of São Paulo University (IFUSP), High Energy Physics and Instrumentation Center (HEPIC), Ionizing Radiation Effects Laboratory (LERI), Radiation Tolerant Integrated Circuits (CITAR) project and to the Pelletron accelerator team.

² Correlated measurements in the European accelerators involved were performed by Sohail Musa Mahmood. The work was supervised by professor Ketil Røed from University of Oslo (UiO) who was responsible for those irradiations runs. These runs were crucial for the correct development of SAMPA in time for the experiment update. An extensive description of the test procedures is available in the work Mahmood (2020).

The digital signal processor was already present in MPW1, but in a reduced version with just 3 channels instead of the 32 planned for the complete system. The processor included several digital filters that were responsible for the signal conditioning as BC1, DS and BC2.

This was a test design and included additional debugging ports to give access to the signal data-path. With this possibility, the internal signals were observed and validated.

Being the processor functionally evaluated, the need of radiation tolerance measurements increased due to the absence of similar evaluations on this process. This fact pushed to the execution of the first irradiation which occurred in April of 2015 at The Svedberg Laboratory (TSL) a national research facility located in Uppsala, Sweden.

The MPW1 test board undergone through radiation tests with two main objectives. The first was to validate the tolerance of the device against latch-ups. The second was to qualify the technology TSMC 130 nm with respect to SEU as both the group and the HEP community at CERN didn't have a large experience with this technological node and foundry, being CERN migrating from IBM to TSMC just in parallel with the first early runs of SAMPA.

The particle source used for this experiment was the Gustaf Werner Cyclotron which is illustrated in figure 43 among with several other auxiliary involved equipment.



Figure 43 – The Gustaf Werner Cyclotron with some of its main blocks numbered.

Source: The Svedberg Laboratory.

In the figure 43, the white-mark with number 1 indicate the Magnet yoke; this device is responsible to bend the particle flow in the accelerating spiral. The module 2 is an Internal Ion source. The radio frequency (RF) system is indicated by 3, and the machines at 4 are a part of the Vacuum system elements. The particles culminate at the beam transport output (marked as 5).

From the beam transport the particles can reach the proton facility which is located at the Blue hall experimental area, where the target elements can be mounted. In this case, the test board with the ASIC, the involved measurement equipment and the developed FPGA data acquisition system.

Figure 44 shows the test room environment. It is possible to see the carrier board in the beam line just after a dark gray box which contains a graphite collimator. The image also provides zoomed versions of the chip and the FPGA at right.

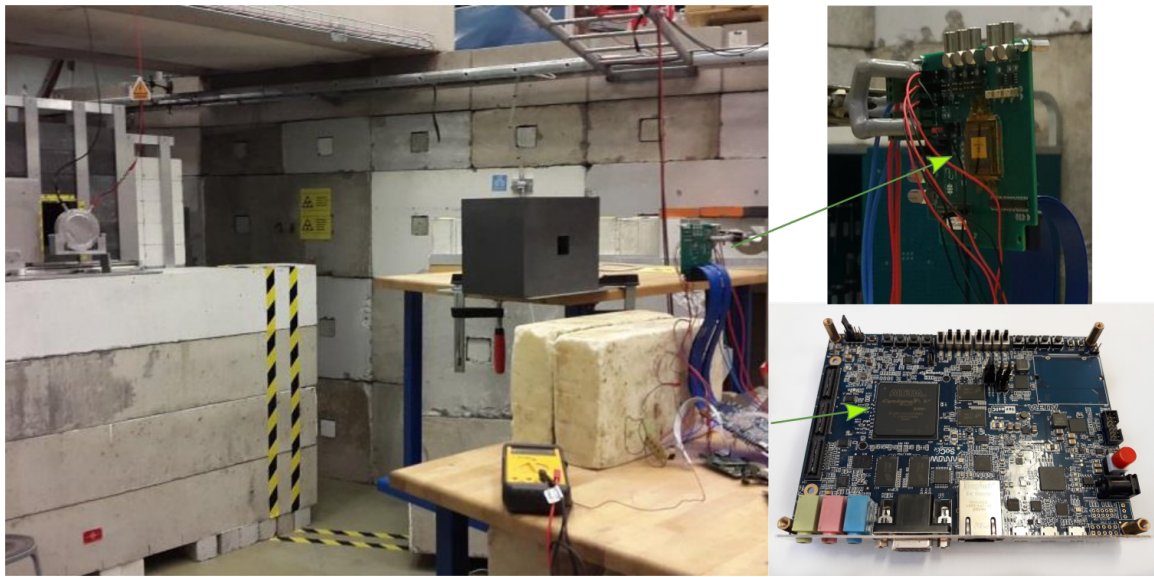


Figure 44 – Photo of the SAMPA MPW1 irradiation.

Source: The author and Sohail Musa Mahmood (MAHMOOD *et al.*, 2018).

It is also noticeable in figure 44 that a large blue high speed mezzanine card (HSMC) extension cable was used between the MPW1 test board and the FPGA. The FPGA was placed in a safer place, just after the two big radiation damper blocks in conjunct with other control boards. These boards are not radiation hardened and could interfere in the test results or even fully fail, interrupting the run and causing loss of time and money.

In this work, the cross-section will be an important metric being used along several studies to represent the sensitivity of some target event with respect to radiation, its value will be mainly calculated by the expression at equation 4.1:

$$\sigma = \frac{N_{events}}{F}, \quad (4.1)$$

where: σ represents the single event cross-section, the variable F is the accumulated fluence in the test and N_{events} is the total accounted observations of an event of interest. The event can be of several types, for example, errors (upsets) in flip-flops, transients in nets, latch-ups or many other events.

Aiming to discover the MPW1 characteristics, the prototype was irradiated with protons at average energy up to 160 MeV during six trials. These could reach a total fluence near $176 \cdot 10^9$ protons/cm² with a total dose in silicon of 12 krad, which was accumulated during all the tests, focusing both in SEE and TID analysis.

The main difference between the six runs was the flux and the run-time, where values between $6.52 \cdot 10^6$ protons/cm²s and $63.96 \cdot 10^6$ protons/cm²s were achieved for flux with run-time up to 2040 s.

All the runs were used to validate the tolerance to SEL, the methodology to detect a SEL was based on the monitoring the line voltage and current consumption in a stable scenario which constant clock. In case of abnormal changes in the consumption, a SEL can be the root cause and this event should be accounted and investigated.

For the measurements made along the six runs no signs of abnormal current or voltage change happened. With this information we concluded that no SEL was detected in any of the exposures, stating the tolerance of the base design scenario. As no SEL was detected during all the run-time, which is positive for the applicability of the design and technological process, it is at least possible to provide an up-limit to the SEL cross-section (MAHMOOD, 2020). As the total fluence was $176 \cdot 10^9$ protons/cm² per SAMPA MPW1 chip, so the SEL cross-section is limited by $5.8 \cdot 10^{-12}$ cm².

Knowing the upper bound for the cross-section, a lower limit for the mean time between failures (MTBF) can be stated. Using the standard flux values in ALICE for the device (MAHMOOD, 2020), the MTBF is expected to be greater than thousands of hours. As this value is quite high, it released the pressure over the SEL aspect as these limits are believed to be tolerable and then the project can continue as the device resisted to acceptable levels.

With the device approved in the SEL analysis, another very important aspect could be evaluated, the single event upset sensitivity. In preparation for this analysis, during the design of MPW1 chip 3, this author inserted a large shift register structure aiming to make the SEU evaluations viable and straightforward.

The shift register is made of 15.000 TSMC 130 nm flip flops (standard design kit), of small size and drive strength, connected in a long chain, without reset. These devices were fed by a strong clock tree and exclusive input/output (IO) PADs. The size of the shift register was the largest possible, being limited by the remaining free area in the MPW chip.

The test procedure to detect the SEUs were very direct and based on the insertion of an alternating pattern on the shift register input and clocking it; in this way the chip would be filled with a pattern 0xAA and then with 0x55 after the clock pulse. The tester should periodically empty and reload the shift register checking if the output pattern still

equaled to the original input one.

When a difference from low to high or high to low was found, the software should log it along with the time and position in a way that after the test, statistical information could be extracted from the acquired data.

From the six runs, four were used to obtain SEU data, each one with a different time and flux, creating a set of distinct fluences. With the accounting of the registered errors for each flux run, it was possible to check the general behavior of the device in this try and linearly extract the cross-section parameter after data analysis. In this SEU analysis, differently from the latch-up study, several errors were found and a total of 105 upsets were measured after data processing.

Knowing the amount of errors in each run and using the linear fit of the results, an average fitted cross-section of $(7.0 \pm 1.2) \cdot 10^{-14} \text{ cm}^2$ per DFF was obtained, for a confidence interval of 95% (MAHMOOD, 2020). This result was in accordance with the expectations and by the literature values between $4.6 \cdot 10^{-14} \text{ cm}^2$ and $7 \cdot 10^{-14} \text{ cm}^2$ were cited for this feature size (FACCIO; BONACINI, 2010; BONACINI, 2010).

As the dimensions of the ALICE detector are enormous and a massive amount of chips will be running, it is important to use the obtained cross-section to get an estimate of the MTBF for the TPC and MCH detectors. For this task it is supposed an estimated count of 55 thousand DFFs for the final complete 32 channels SAMPA design.

The TPC will have around half a million channels, which accounts for about 16380 SAMPAs and using the previous measured cross-section, it is possible to obtain that the MTBF is near 3.98 seconds. For the MCH, the case is even tighter as they will use around 34.000 SAMPAs implying that the MTBF can achieve a value as low as 1.92 seconds.

These results are very important and reveal that with respect to SEL, the technology and SAMPA are safe enough for the application but on the other hand the SEU MTBF is too low. This motivates and shows an important face of this work, justifying its existence as it aims exactly in the digital logic tolerance to errors caused by radiation and ways to improve it.

Due to these tests and predictions, next SAMPA versions received replication and protections to operate in the ALICE environment with a tolerable amount of errors, this using TMR and techniques already described in past sections.

The following sub-section will address the tests done with the first full prototype of the SAMPA including all channels and with functionality ready for the real application.

4.2 SAMPA V2

Along 2014 and 2015 a new version of the ASIC was developed and named as SAMPA version two (SAMPA V2). It was a full 32 channels mixed signal ASIC including a complete digital signal processor complying with the CERN specifications for the application in the TPC and MCH ALICE detectors (ALICE; APPELSHÄUSER; LIPPMANN, 2013; BARBOZA *et al.*, 2016).

The processor design was carried out prioritizing several guidelines and constraints agreed with CERN, where by first, the maximum chip dimension was limited due to physical board size. The processor also needed to have a big amount of SRAM memory (around 2.6 Mb), to buffer data bursts. To complete the scenario, it should be radiation tolerant and several redundancies must be added.

The obtained solution to cope with the targets and restrictions was based on the design of the filtering, communication and control with default standard cells and the SRAMs with IPs. Due to area limitation, the standard cell sections were only partially redundant, where the FSMs, filter operation logic and communication have been protected, while most of the chip data-path could not.

The SRAM IPs have been chosen trying to minimize the area where a single port IP was deployed for the BC1 pedestal memory and dual port IPs were needed for the pre-trigger, headers, neighbor and data memory. Most of the dual port memory area used was due to clock domain crossings and read/write data rate compatibilization. With these choices, the ASIC total area met the available margins and it was also in accordance to budget possibilities. Being the design taped-out as a MLM engineering run at TSMC in early 2016.

The chip footprint needed to be minimized and several cross-talk issues must have been taken into consideration for an optimum design; these facts implied in the packing with a custom made BGA³. This package was an important system improvement, but which impacted in extra manufacturing time.

In a way to anticipate the first complete system test results, CERN in conjunct with SAMPA and IN2P3⁴ proposed the development of a carrier board for chip on-board, which allowed the validation tests to begin in July 2016.

During the next months SAMPA V2 was tested and characterized. It operated adequately in room environment and that was an important proof of concept for the requested design.

³ Remarks for the excellent teamwork from SAMPA, CERN ALICE, IMEC, Institut National de Physique Nucléaire et de Physique des Particules (IN2P3) and ASE engineers.

⁴ Thanks to IN2P3, especially for Valerie Chambert and Khaing Tun-Lanoë due to the board design and production.

The ASIC was not fully compatible with the experiment needs, exhibiting small divergences in both analog and digital parts. The central difficulties were related to the power-on reset and internal bandgaps for voltage reference generation. The digital signal processor also had issues in the protocol compliance with the experiment requisitions.

The main problems were in the analog domain but cautiously, bypass and alternative solutions were inserted in the die and workarounds could be proposed to save the tape-out, both for digital and analog parts. For extended details please see (SANCHES; VELURE, 2018).

After the adjustments, the chip could be properly read out and its results were adequate, being accepted by the scientific community and CERN ALICE collaboration. For detailed results, please see our publication (ADOLFSSON *et al.*, 2017), which addressed the characterization of the full 32 channel SAMPA chip.

In March of 2017, the SAMPA V2 prototype was already tested for functionality in standard environment and radiation tests could be performed. The previous irradiation facilities at Upsalla were not available for this time and a new accelerator was selected to be used. The campaign was realized at KVI facility located at the University of Groningen in the Netherlands.

The KVI accelerator is a superconducting cyclotron know as AGOR, which is shown in the figure 45. The proton irradiation was performed on the AGOR Facility for Irradiations of Materials. The machine can provide an in-air beamline dedicated to irradiation of samples with high energy beams up to 190 MeV protons (solar spectrum), energy similar to the used in other tests made with SAMPA MPW1.

In the KVI irradiation, a different test setup was used, now basing on a carrier board with the die direct wire-bonded to it. The figure 46 shows the board (designed by IN2P3). It also presents a zoomed version of the wire bounded SAMPA V2 with its hundreds of pins, illustrating the complexity of the board and setup design for this experiment.

In KVI, the board mounting rack was also more functional than in previous irradiations, allowing XY axis movements. That eased the positioning and improved the beam to chip alignment, which was very important as SAMPA V2 die is much larger than the MPW1 chip previously irradiated.

The data acquisition system in the test room was composed of one Altera SOCKIT FPGA board and a single board computer. The acquisition devices were placed behind the device under test (DUT) mounting plate and out of the beamline. Other computers were also used to connect and log the data, but they were much better shielded and out of the irradiation environment.

SAMPA V2 prototype irradiation procedures were much more complex than the

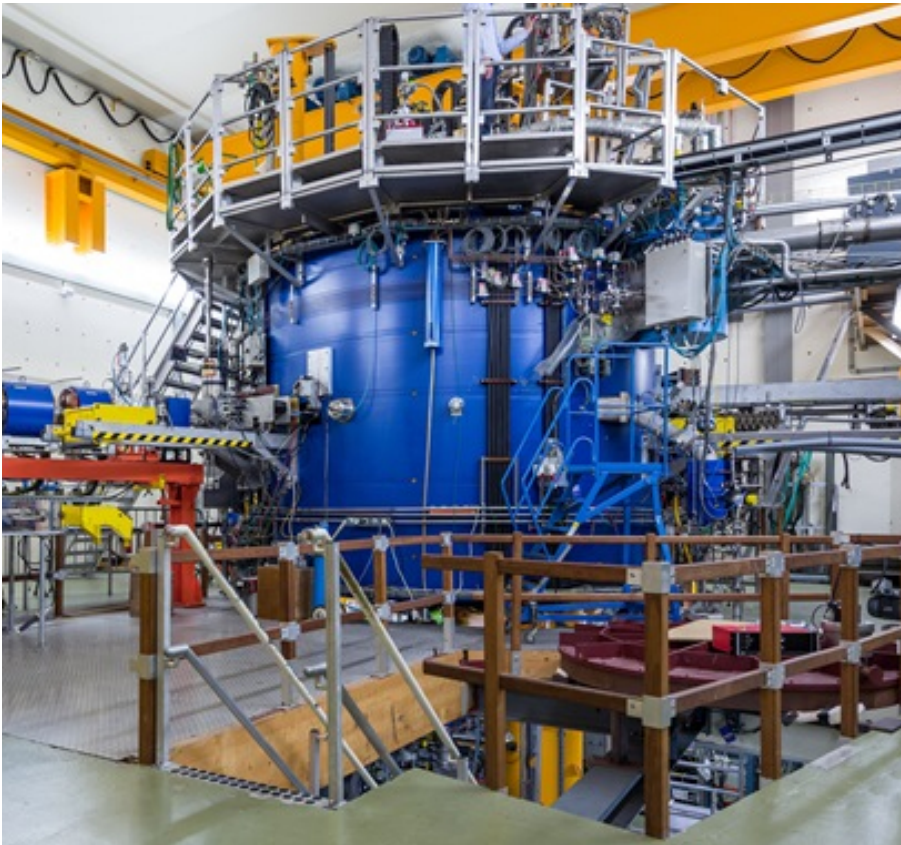


Figure 45 – The AGOR cyclotron.

Source: Peter Tahl. University of Groningen (the Netherlands).

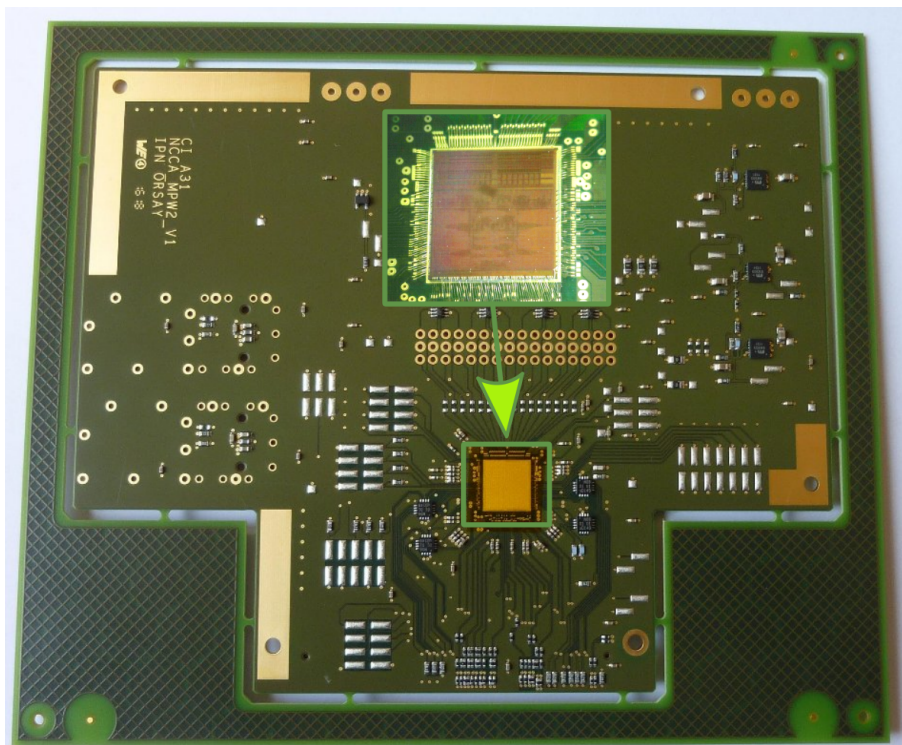


Figure 46 – Carrier board and a zoomed version of the exposed wire bounded SAMPA.

last case for MPW1. SAMPA V2 has an enormous increase in functionality and complexity, without mentioning the natural increase of size from a system with 3 channels growing to 32.

In this case, the main difference is that in SAMPA V2 there is no dedicated test infrastructure for irradiation, but a full system targeted for the final application. With this scenario in place, several system specific tests were proposed and the synthesized results will be very briefly addressed in the following paragraphs.

The tests done with SAMPA V2 were: scan chain, memory self-test, filters baseline estimation, registers monitoring, ring oscillator frequency, SLVS link status, packet integrity (HEADER against DATA) and internal chip error counters monitoring. Were these counters monitor data integrity, parity, redundancy and hamming code errors.

In the SAMPA V2 tests, the irradiation was conducted with 184 MeV protons (in sample), reaching a total fluence of $1.2 \cdot 10^{12}$ protons/cm² along 17 runs of different fluxes.

The first test procedure was based on the Scan Chain functionality of the ASIC (DE CARVALHO *et al.*, 2018); this was proposed as an important reuse of the DFT inserted mode originally implemented to check for the correct manufacture of the logic. One configuration of this scan chain culminates in the wiring of the chip flip flops in a similar fashion to the shift register made for MPW1, but now without the extra area consumption of that specific SEU testing block.

There are 121295 scan flip flops in SAMPA, distributed along five parallel scan chains of about 24 thousand flip flops each, providing a good structure to analyze the SEU cross-section in SAMPA V2.

The ASIC was tested using several fluxes, from $7 \cdot 10^6$ protons/cm²s up to $0.39 \cdot 10^9$ protons/cm²s and achieving a fluence of $200 \cdot 10^9$ protons/cm² for the high flux case.

Using the linear fit of the error data, it was possible to find the SEU cross-section for the SAMPA V2, where a mean value of $(5.65 \pm 0.80) \cdot 10^{-14}$ cm² per DFF was found for a 95% confidence interval.

In this experiment, it was possible to have different spatial parallel tests due to the 5 scan chains. With this information, it was tried to discover if there were any important spatial variation between the results over the chip area. For that, an analysis was made comparing the 5 scan chain cross-section results, where the standard deviation between the individual shift registers was the selected metric. These calculations found a standard deviation of $6.3 \cdot 10^{-15}$ cm², which is in the same order of magnitude than the uncertainty obtained for the cross-section that was $8.0 \cdot 10^{-15}$ cm². With this fact, it was concluded that the spatial variation of the cross-section was not important in the present case and the run was performed successfully.

The standard deviation of different chip samples tested was also calculated and resulted in $7.0 \cdot 10^{-15} \text{ cm}^2$; in this study the variation was also inside the error margin, which has led to the important conclusion that the cross-section is not connected to process variation, what is positive as the results can be more widely used.

It is also relevant to note that the results for the second version of SAMPA were compatible with the ones measured for SAMPA MPW1. By including the error margin, the obtained cross-sections match each other; with this result the basic SEU evaluation of SAMPA V2 was concluded.

Other tests were then performed and to be concise, the most relevant ones will be briefly mentioned in the following paragraphs, focusing after on some important results, artifacts and observations about the unexpected cases.

The next test addressed the internal ring oscillator; this block is composed of a loop with 102 inverters plus one NAND that is activated to generate a signal of about 100 MHz. The frequency can then be monitored by a addressable field in the global register unit and read by I2C (SANCHES; VELURE, 2018; BREGANT *et al.*, 2017).

In the oscillator test, the chip produced very stable results for the several evaluations made, showing that the dose up to 15 krad accumulated in silicon during all the irradiations did not expressively change the speed performance.

With the stable performance measured on digital side, signal degradation analysis due to TID was evaluated using the value of the front-end baseline. This value can be digitally read in a per channel base using debug functions implemented in the digital filters BC3 and BC2.

The filter estimated baseline can be read using the I2C interface, by accessing the channel register unit at the addresses *BC3BSL* and/or *BC2BSL* (BREGANT *et al.*, 2017), with the filter of interest enabled.

The results for the BC3 baseline were stable and consistent with the initial baseline values before the irradiation, even after the full irradiation period. This is important and states that both the logic and the front-end analog electronics did not shift or deviate from their standard behavior after the exposure of 15 krad of TID.

For the BC2 baseline at *BC2BSL*, the results were very similar to the ones measured for BC3 but unfortunately when the fluence reached the range of $1.5 \cdot 10^9$ particles/cm² to $5 \cdot 10^9$ particles/cm² some unexpected events occurred. These artifacts involved rapid changes in the read baseline value from some channels. For example, at random times the filtered values had gone from 88 (a normal baseline value) to 1880, and even there were cases of getting stuck in that high values.

This kind of peak was totally unreal for the analog block in question, as it always

returns to baseline after the charge pulse. Observing that BC3 filter did not have that behavior in the same time range, the BC2 filter was marked for analysis with respect to this artifact, probably linked to radiation vulnerability and SEUs. In order to not deviate the reader's attention from the global scenario, the results of this filter and newer prototypes are addressed in a future dedicated section.

Another relevant topic of interest was the SAMPA memory, the ASIC has 130 internal memory IPs that correspond to a big part of its area.

To ensure the correct manufacture of these set of blocks the author proposed an automatic built-in memory test to quickly validate this part of the ASIC without the need of any specific external tool or even Joint Test Action Group (JTAG) connection.

The test generates reads and writes with alternate low and high patterns to each bit of each memory in the SAMPA. As output, it provides an external signal that can be used as a trigger to stop the manufacture test if errors are found and a pulsed error indicator to inform each time one error is found, driving a high pulse during one clock cycle.

In this context, an important value still not characterized was the cross-section of the memory IP block. To achieve this objective the second output of the memory built-in self-test was captured and with the monitoring of the pulses, an estimation of the cross-section could be calculated.

This internal auto-test procedure is similar to the shift register one, but with one main difference: here is not possible to obtain the zero to one and one to zero individual cross-section, just the full SEU cross-section.

This memory IP test was monitored in several flux levels; achieving a fluence up to $16 \cdot 10^9$ particles/cm². During the tests, almost two thousand bit flips were encountered. With this considerable amount of events, an adequate estimation of the average cross-section could be made; by using that the number of bits per memory is known, a cross-section of $(4.9 \pm 0.5) \cdot 10^{-14}$ cm² per unitary bit cell was obtained.

Comparing the IP cross-section to the value achieved for a single standard cell flip-flop ($(5.65 \pm 0.80) \cdot 10^{-14}$ cm²) it is possible to see that the standard cell replacement by memory IPs was a good design choice, since even reducing considerably the area of the blocks, they still have a similar cross-section (actually marginally smaller than normal flip-flops).

SAMPA V2 also provides a direct read/write (R/W) access to one special block called pedestal memory. This can be programmed online by the control room using the I2C protocol in the real CERN ALICE experiment and is part of BC1 functionality (SANCHES; VELURE, 2018; BREGANT *et al.*, 2017; ADOLFSSON *et al.*, 2017). This pedestal memory R/W access can be reused in irradiation tests, providing a way to overcome the limitations

of the automatic self-test and with this obtain a better estimation of the individual memory behavior, including the zero to one and one to zero cross-section rates.

The difference in the I2C R/W testing is that the chip needs to be continuously read, address by address and channel by channel using I2C, which is a slow protocol. But this has not shown to be a big problem as the previous test (built-in memory self-test) already showed that the error rate is not very high. This fact allowed a reasonable amount of time for the data acquisition system to scan the memory.

In this way the R/W test was performed and a cross-section in the order of $(3.51 \pm 0.53) \cdot 10^{-14} \text{ cm}^2$ per pedestal memory bit was found for this specific test. The data provided per bit position statistics and the evaluation show that each of the 10 output bit was around 10% of occurrence. The statistics for low to high and high to low upsets were also calculated, where an even 50% division was found showing adequate symmetry for these single events. Up to this test, the memory behaved as expected and even showed a low cross-section, with about half of the cross-section of a standard flip-flop which is very positive.

The chip operated and resisted well during the packet and system readout tests, where a massive amount of packets (in the order of dozens of thousands) were read without problems during the irradiation.

Furthermore, the triplication worked properly in the registers monitored and this proved to be a good applied solution. The section 3.4.2 discuss about triplication and its characteristics.

The tests were performed without major issues, although during the irradiations with high proton flux from $1.6 \cdot 10^7$ protons/cm²s to $3.8 \cdot 10^8$ protons/cm²s, SAMPA V2 started to show some unexpected artifacts in its measurements. During these events, the chip suddenly started to present jumps in the current consumption, in a step-like aspect. The figure 47 shows one captured event along the time.

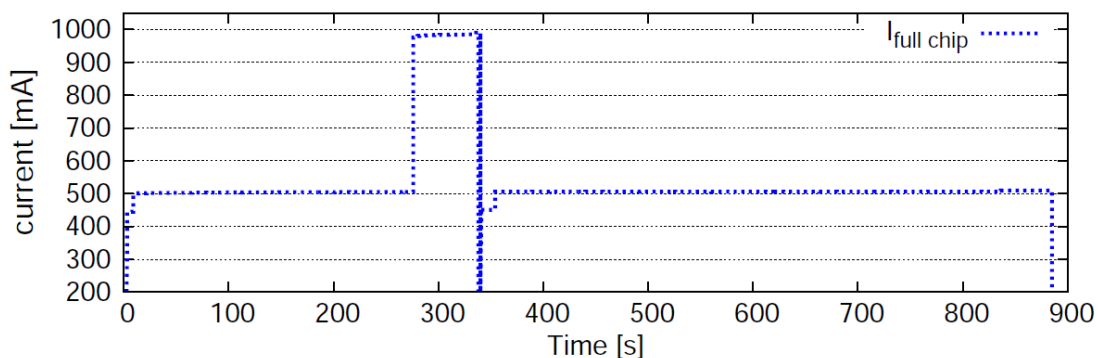


Figure 47 – SAMPA V2 full chip current along the time during the irradiation.

Source: Sohail Musa Mahmood.

In the figure 47 the ASIC was being irradiated with a flux of about $1.8 \cdot 10^7$ protons/cm²s

and after the start-up the consumption was stable at around half ampere for the full ASIC. During the test, just before 300 seconds of operation the consumption almost doubled keeping in that state continuously.

It is also possible to see in the figure that the consumption returned to the normal level about sixty seconds after the event; this was due to operator induced power cycle in the device.

After the restart, the device operated normally and without signs of errors, problems or main damages. With this, it was concluded that the event was nondestructive, and the chip could safely operate again after a power cycle, which is very important for the application in question.

One of the justifications found to explain why the chip resisted to this kind of event was the well-designed power distribution grid inside the ASIC, which was created to provide stable voltage to the full chip core with very limited IR drop.

As SAMPA has 32 channels, the design ended up with several memory blocks. They work in parallel and along with a considerable amount of standard cell based logic. These facts triggered the design of a power grid with resistance low enough to be stable during the intense write currents peaks generated by the memory blocks.

For the memory blocks in question, the write current peaks can be up to 72 times higher than the standard average current used during normal operation.

Figure 48 shows the SAMPA power distribution grid over the digital core of the ASIC. It is also shown the final positioning of the memory IPs in the ASIC where each of the 130 light-blue boxes is an independent SRAM memory IP. For the convenience of the reader, the dense top horizontal ultra tick metal distribution grid was omitted at metal 7 level. The lower smaller metal 1 routing and the individual memory power rings are also not shown.

Figure 48 focus on the vertical metal 6 distribution and each vertical orange line is a set of two rails, one VDD and one VSS (not visually separable due to their proximity in the zoomed-out view). The vertical stripe positioning was optimized targeting safe and good IR drop ranges while maintaining the congestion level acceptable for full system routing; the final solution included variable width stripes, depending on the horizontal positioning and routing usage of the tracks in the area. This optimization culminated in vertical stripes from 4 μm to 10 μm .

The power grid was validated using Cadence VOLTUS, ENCOUNTER, INCISIV and QRC along with Mentor Calibre and Modelsim. The design was approved as a good solution in both IR drop and electro-migration.

To illustrate the performance of the power grid, figure 49 shows the voltage drop

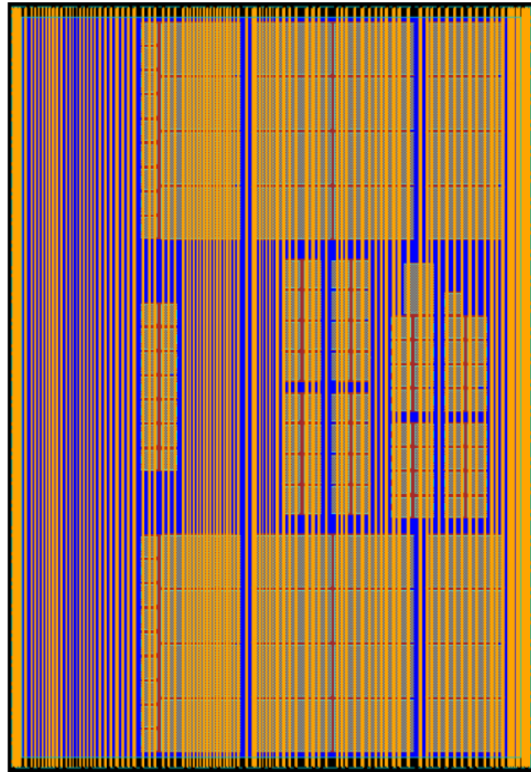


Figure 48 – SAMPA V2 digital core power grid.

during normal operation in relation to the position in the digital core while running at 320 MHz serial output clock and 10 MSPs conversion rate, which is one of the most power hungrier modes for this version.

In the figure 49, it is important to notice that the input voltage is set to 1.2 V and the full-color range was matched to just 1% of drop, so the green was mapped to 1.2 V and red to 1.188 V). The image shows that the power grid is with a good margin when feeding the blocks, as they can work in the worst case with 1.08 V or 10% less than nominal voltage and this system was designed and validated up to these limits. In this way, the grid allows some margin for overconsumption (as the case of the current steps in the problematic events triggered by radiation). This could explain how the chip survives and even keep working fine with these increments in current.

Going back to the fault itself, it is important to investigate the kind of failure and its source. There are several options for a fault like this, but two specific ones emerged as explanations for this artifact in specific, the single event functional interrupt and the single event latch-up (MAHMOOD, 2020).

Single event functional interrupts, in general, are connected to events that change the standard behavior of the device generating malfunctions that may interrupt routines or enter in unexpected states for a specified point in the run-time, causing system operation changes.

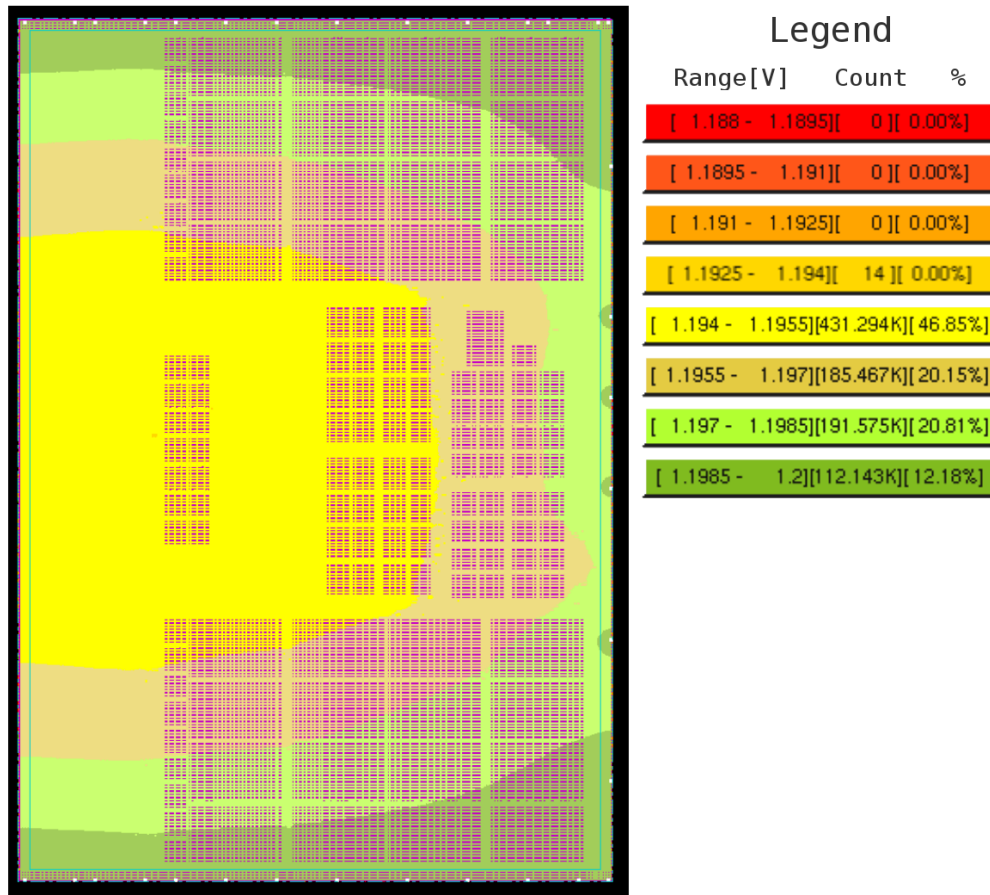


Figure 49 – SAMPA V2 IR drop map in digital core in 320 MHz mode.

In the SAMPA case, it would be possible that due to a single event upset, some state machine started to go in sequential operations in a repetitive and fast way; that is not predicted, strongly increasing the power supply, or even a set of events like this in parallel.

The turning point fact is that SAMPA has most of this control triplicated and with full reset activation (generated by a reset manager), being reset applied after the event. Even with this, the unexpected consumption level was not eliminated after the hard reset. These facts increased the possibility of the event be a single event latch-up and not a configuration or behavioral fault.

The work Artola, Hubert and Rousselin (2014) performs several analyses of latch-ups caused by single events, including one that shows the dynamic characteristics of latch-up in relation to the current versus time.

In Mahmood (2020) work, also the real SAMPA current behavior is compared to the guidelines in Artola, Hubert and Rousselin (2014) and the 4 phases in the transition from SAMPA normal operation to a single event latch-up match with the reference. This was a second important source to state with more conviction that latch-ups are really happening on SAMPA version two.

It is also important to investigate the origin of these events, allowing the focused and localized correction of the latch-up problem. In this direction, figure 50 illustrates the SAMPA current consumption individualized by each power domain. In the figure, I_{FE1} and I_{FE2} are the analog front-end power domains, I_{ADC} is the current usage of the ADC without including its reference, which is individualized in $I_{ADC-ref}$. The current I_{DR} corresponds to the digital I2C and differential SLVS drivers and finally, I_{DG} is the digital core power domain.

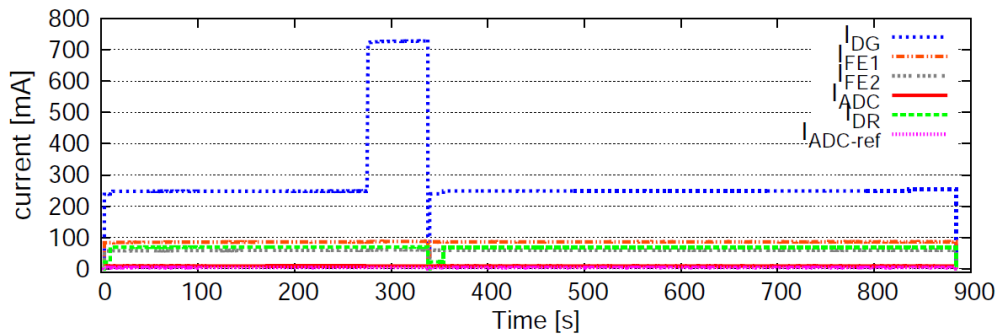


Figure 50 – SAMPA V2 chip current consumption individualized per power domain.

Source: Sohail Musa Mahmood.

From the figure 50, it is clearly possible to see that the current jump is from the digital core. Trying to achieve a better understanding of the artifact, other tests were done and figure 50 shows a case where latch-ups happened in a different and remarkable way.

In figure 51, it is possible to observe that the consumption is following a staircase form. This triggered the attention, since nothing similar happened in the evaluation of the first prototype. There are also clear signs of more than one latch-up happening in the same run, holding each time more current. This is very dangerous as summing each current step the consumption could reach several amperes, possibly damaging the chip by overheating or electro-migration in the power rails.

The repeating format of the latch-up event also indicates the possibility of the latch-up being triggered in a block that is used several times in the ASIC, which is another good hint in this investigation.

One interesting fact was that, after a full run analysis, the latch-up events were found both in the normal logic operation, in the scan chain tests and in memory readout, but it did not look to interfere with the basic logic functions or configuration of the chip. This was also a good indicator of the source of the latch-up, or better, an indicator that the standard cell logic is probably not the origin. It was unlikely that with the extra power consumption of a quarter of ampere, the standard cells around a latch-up would work properly due to power integrity issues and logic errors caused by the triggering of the thyristor itself.

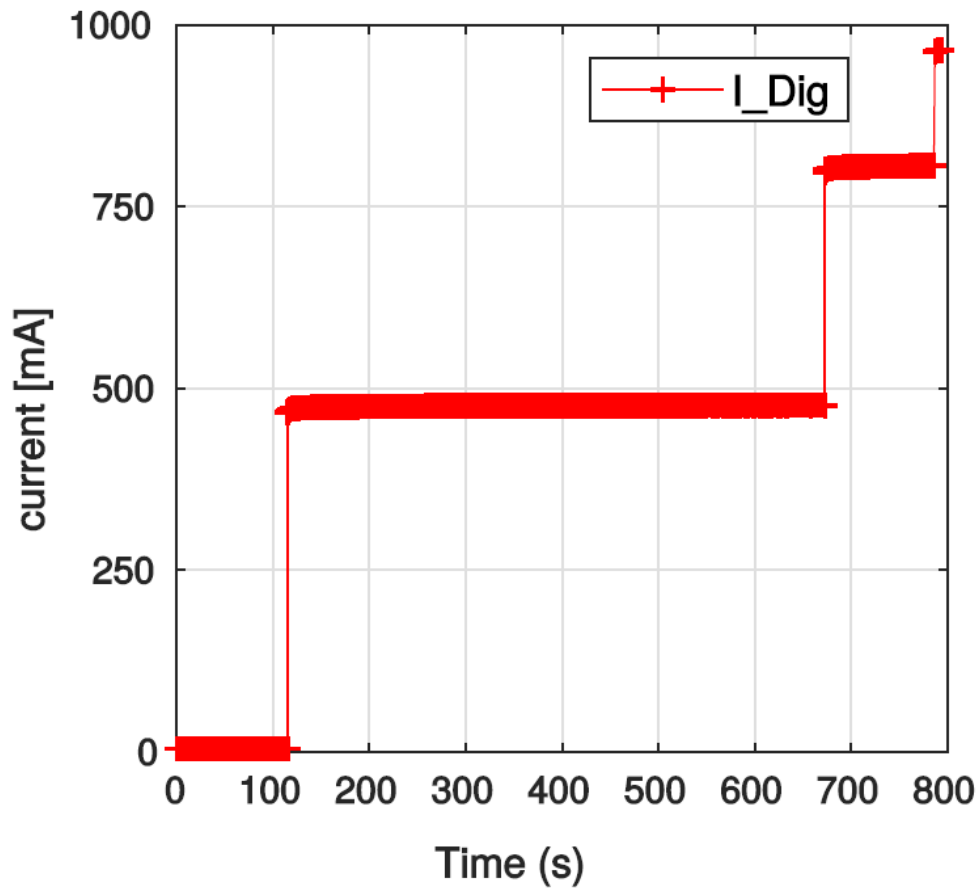


Figure 51 – SAMPA V2 chip current during a longer run without power cycling.

Source: Sohail Musa Mahmood.

After the above tests, a new irradiation was proposed and in May of 2017 heavy ion tests were made with the SAMPA V2 to check if the SEL phenomena would persist with this kind of stimulus. These tests were made in Louvain-la-Neuve, Belgium at the Université Catholique de Louvain (UCL) using the Heavy-ion Irradiation Facility (HIF). The tests were done with hardware and software elements provided by both SAMPA team at University of São Paulo (USP), University of Bergen (UiB), UiO and Boards from IN2P3 Orsay⁵.

The HIF has as its accelerator a cyclotron called CYCLONE that is capable of accelerating and delivering both heavy ions, protons and alpha particles.

In the SAMPA irradiation, the selected particle type was heavy ions. The ions involved were ^{84}Kr , ^{53}Cr , ^{40}Ar , ^{27}Al and ^{22}Ne , sorted here in descending order of energy from about 769 MeV to 238 MeV.

The maximum LET was around $32\text{ MeV}/(\text{mg}/\text{cm}^2)$ and happened for ^{84}Kr , with a range of $94\ \mu\text{m}$ in Si. Table 11 provides more detailed information about some of the

⁵ The SAMPA operator in the tests at UCL was Sohail Musa Mahmood from UiO.

available ions and their parameters.

An advantage of the UCL test infrastructure was that more efficient results were expected in the irradiation due to the usage of a vacuum chamber containing the irradiated setup. This avoids losing a part of the accelerated particles in the air. Additionally, with heavy ions irradiation, a higher rate of single event effects was expected and a better characterization could be made, mainly focusing with this on the latch-ups as they are not as frequent as the upsets in the past tests with protons and a better estimation of the cross-section is important.

The irradiation procedures were executed and being extremely concise about the results, latch-ups were found in this test and in several kinds of heavy ions used. The amount of accounted events had a range between dozens to several hundred depending on the ion, LET and fluence. That was a negative result for the ASIC, but useful to obtain the cross-section and behavior.

Table 11 – UCL HIF particle parameters

Ion	energy (in DUT) [MeV]	Range [μm in Si]	LET [$\text{MeV}/(\text{mg}/\text{cm}^2)$]
$^{13}\text{C}^{4+}$	131	269.3	1.3
$^{22}\text{Ne}^{7+}$	238	202.0	3.3
$^{27}\text{Al}^{8+}$	250	131.2	5.7
$^{40}\text{Ar}^{12+}$	379	120.5	10.0
$^{53}\text{Cr}^{16+}$	513	107.6	16.0
$^{58}\text{Ni}^{18+}$	582	100.5	20.4
$^{84}\text{Kr}^{25+}$	769	94.2	32.4

Figure 52 shows the results for the SAMPA V2 accounted latch-up cross-sections in function of the LET. The lower cross-section was found using the ion $^{22}\text{Ne}^{7+}$ with energy of 238 MeV and fluence of $3.28 \cdot 10^7$ ions/cm², where 23 latch-ups occurred, totalizing a cross-section of $6.9 \cdot 10^{-7}$ cm².

The most stressing case was $^{84}\text{Kr}^{25+}$ at an energy of 769 MeV with a fluence of $4.77 \cdot 10^4$ ions/cm², where a big amount of latch-ups happened. More specifically a total of 247 events were found, generating a cross-section of $5.1 \cdot 10^{-3}$ cm², the worst measured result for this set. Also in case of an intermediary energy ion like $^{53}\text{Cr}^{16+}$ at 513 MeV was obtained a middle cross-section of $3.3 \cdot 10^{-3}$ cm². The fitted saturation cross-section was $4.77 \cdot 10^{-3}$ cm² occurring after the $^{53}\text{Cr}^{16+}$ ion and the threshold LET was estimated to be around $3.3 \text{ MeV}/(\text{mg}/\text{cm}^2)$ (MAHMOOD, 2020).

In conclusion about heavy ion tests, it is possible to say that latch-ups were detected

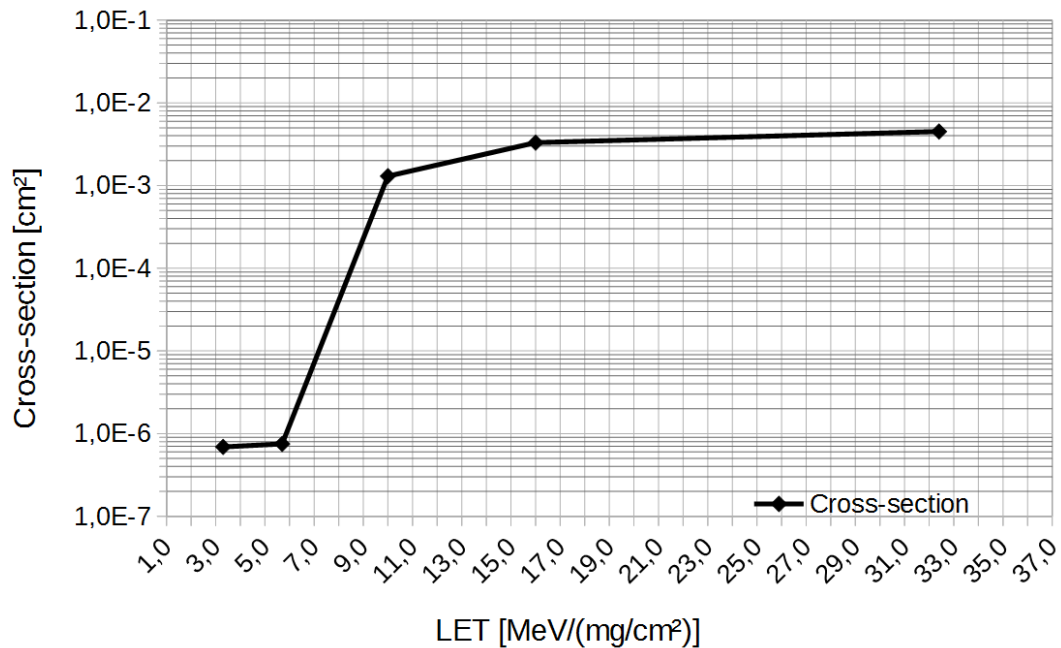


Figure 52 – SAMPA V2 latch-up cross-section for different LETs.

again and at considerable rates. This shows that changes must be done as the chip will operate in an environment with radiation that can trigger latch-ups and the reliability level need to be increased.

The investigation of the SEL root cause has correlated and contributed in several ways to the design of SAMPA V3 and SAMPA V4. To keep this section clean the SEL analysis and other contributions of this work were discussed in the section 3.4.4, named SEL Investigation and Avoidance techniques. With the methodology of section 3.4.4, the designs SAMPA V3 and SAMPA V4 were created. The next section will continue addressing the evaluation of SAMPA V3 and V4 under new irradiation campaigns.

4.3 SAMPA V3 and SAMPA V4

After the actions described in section 3.4.4, which culminated in the replacement of the suspect SEL sensitive blocks, SAMPA V3 and SAMPA V4 were fabricated. The process used was the same of SAMPA V2, the TSMC 130 nm with 7 metal layers. No changes were made in SAMPA pin-out and the substrate routing was evaluated to be adequate so the package design and its substrate were maintained.

Most of the dies were encapsulated in BGA to be soldered or used in sockets during the functional tests and characterizations, but around a dozen of dies were segregated to be wire bounded directly in test boards aiming to permit efficient irradiation procedures and earlier tests.

In this section, SAMPA V3 and V4 will be addressed as the same digital device

as they have identical core designs, so we expect similar results. Even knowing that, by safety, both chips were evaluated as there were changes in analog front-end blocks that could cause system issues. To cope with that, a new study was performed including several irradiations, where the first happened in November of 2017. The location was again UCL in Belgium and heavy ions were used as accelerated particles.

The tests were performed for all complete versions of the chip, the SAMPA V2, V3 and V4. Using 10 hours of heavy ion beam time two SAMPA V4, one V3 and one V2 were exposed.

Several test procedures were executed in this time, including the built-in memory test, the shift register scan chain test and the I2C read/write scan.

The first test aimed to check the behavior of the chip with all memory available active and in continuous writes and reads from all addresses and bits.

The second test stimulated most of the standard cell based registers and logic, but without going through the memory IPs access.

The I2C slow control read/write checks the 39 global registers together with the 32 x 31 channel registers and have also the advantage of direct access to all addresses of Pedestal Memory in an individual way. As this was a suspect block, this access could help to prove the hypothesis.

The idea with the three different kinds of tests was to obtain the single event upset cross-section of the flip flops and memory IPs while stimulating the chip in different beams, providing parallel information while observing the currents and possible latch-up events.

The difference in the V3 and V4 irradiation is that by the first time it is possible to have per address access to a dual port memory. This due to the fact that in SAMPA V3 and V4 the pedestal memory is implemented with a dual port memory and that is accessible by the I2C controller connected to the per channel register unit. With this access, it is possible to study the behavior of the bit flips and also verify how a chip populated with only one kind of memory IP would work with respect to sensitivity to single event latch-ups.

Initially, the single event upset tests were executed and from them it was possible to extract the upset cross-sections for the memory blocks, individually per type. The single port memory cross-section obtained was $3.5 \cdot 10^{-14} \text{cm}^2$, in the other hand for the dual port memory it is $4.9 \cdot 10^{-14} \text{cm}^2$.

The bit cell area for the dual port is bigger and it has more control signals resulting in a distinct cross-section. The single port had a cross-section 28.6% lower than the dual port version, so we expect more bit flips in the new dual port pedestal.

In fact, this is not a good point but the main target being addressed was the

fact that this single port memory blocks are being pointed as guilty to generate latch-up sensitive areas (please see section 3.4.4); in this scenario and with such a problem as latch-ups to solve, the modest increase in the errors in this memory may be tolerable. There is also the option to periodically refresh these memory values using the I2C access, reducing dramatically the importance of the additional bit flips due to this new cross-section.

With the upset cross-section evaluated, the focus was moved to the results from the latch-up accounting, the most relevant for this irradiation. In the present experiment, irradiations with several LET values were done, including 1.3, 5.7, 8.06, 16, 32.4 and 62.5 MeV/(mg/cm²).

Aiming to save time and for deeper analysis of the newer SAMPA versions, in this experiment the SAMPA V2 was irradiated just focusing on a single LET of 16 MeV/(mg/cm²), providing comparison data but not a complete LET curve. The results of this re-irradiation of SAMPA V2 agreed with the previous measurements taken in this accelerator months before, and isolating the results for LET of 16 MeV/(mg/cm²) the cross-section was $3.3 \cdot 10^{-3} \text{cm}^2$ in the previous run and $3.2 \cdot 10^{-3} \text{cm}^2$ in the new one, implying in a difference of just 3%. This indicates repeatability and validates the new scenario for the measurements with other chip versions.

In this campaign in addition to SAMPA V2, three runs have been executed for SAMPA V3 and 22 for SAMPA V4, in total 26 runs. From these, 3 had their temperature intentionally increased from around 40 °C up to 85 °C, in a way to investigate if it would impact the latch-up rate.

After these runs, the results were accounted and as a product of the changes in these new design versions, no latch-up events have been found in any of these dozens of exposures.

This is a very important result of this work and goes in two directions; at first, the chip is much more acceptable to work in the high energy physics experiments environment. Moreover, and even highly relevant to the present work is that, with the discussed strategies, the designers managed to locate the guilty block and replace it.

Furthermore, the operation was made without access to the real layout of the block (as it is a protected IP) and without investigation on the physical device. This shows that this problem could have been solved in the version two of the chip if this thesis has already been available, and so it may be used in further designs, before problems of this kind happen again, saving effort, man-power, time and money.

4.3.1 High resolution tests

After the heavy ion tests, a final exposition was done trying to better understand the latch-up events source physical positioning using high resolution equipment. These

tests were proposed to scan the suspected areas already pointed by the methods in this work and validated with the new fabrications of the ASIC.

To perform these new evaluations, the IN2P3 from Orsay-France helped providing a set of six modified printed circuit boards, 2 of each full SAMPA version. These boards had a modified backside, including a hole exposing the substrate behind the wire-bounded die (the chip back-face). For adequate results, it is crucial to have dies with a clear surface, without scratches. After careful selection over the samples, a set of ASICs to be exposed was ready.

The tests were done in January of 2018 at the Institute of Electronics and Systems Laboratory, Université Montpellier II, France. A laser facility was used, making possible the precise energy injection at specific spots in the ASIC substrate⁶.

A machine named PULSYS rad, from PULSCAN enterprise was the core of irradiation setup. This device is a complete solution for test and failure analysis of semiconductor devices using short laser pulses. Figure 53 shows the PULSYS box opened, where the lens and target space can be seen.

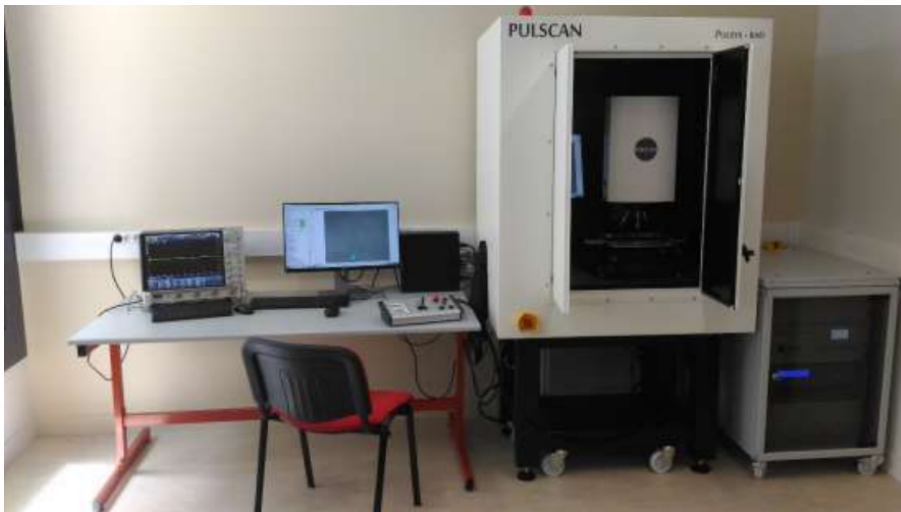


Figure 53 – The final campaign setup using the PULSYS-RAD system.

Source: Jonathas (2018).

The laser pico source used in this setup is capable of generating short pulses of around 30 ps, one standard duration for SEE laser testing (JONATHAS, 2018). The laser wavelength was 1064 nm, with injected energy selectable from 32 pJ up to a nano Joule. The system is also very precise and focused, being capable of generating light spots of 1.2 μm with 200 nm uncertainty, fulfilling the requirements to point in structures even inside the memory IPs targeted for scanning.

The system included a PULSYS infrared microscope, which is very useful to understand the position of the structures seen from the ASICs bottom side. Using this,

⁶ Additional thanks to the ALICE collaboration, IN2P3, Sohail Musa Mahmood and Ketil Røed.

the positioning of the blocks was validated and a base reference point was selected on the corner of the pre-samples memory on the first group of IPs, as shown in the figure 54 denoted as a yellow cross in the micro-photography.

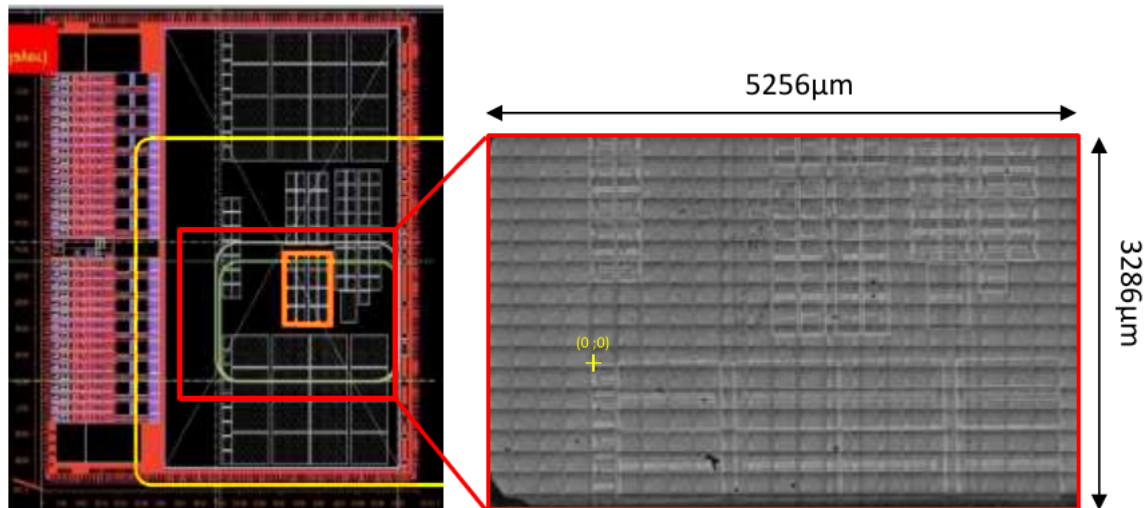


Figure 54 – The SAMPA V2 floor plan and its photography taken by an infrared microscope in the backside accessible area.

Source: The Author, Hugo Hernandez, Ronaldo Silva and Jonathas (2018).

Figure 54 shows three boxes, with the smaller orange box showing the grouping of 16 pedestal memory blocks (the main target of these tests). The middle box, in red, shows the visible area in the micro-photography and the bigger box in yellow shows the approximate size of the accessible area through the bottom hole cut in the backside of the printed circuit board. The image from the microscope clearly allows the identification of the memory blocks edges, exactly what is needed to stimulate them with the laser.

As the previous tests indicated evidences that the SAMPA V2 pedestal memory was a probable candidate for latch-ups, the initial laser pulse injections started in this memory. These aimed at discovering what is the threshold energy needed to enable a thyristor there.

After scanning the block, it was discovered that the IP periphery is not sensitive, but the internal area can be easily excited to create a latch-up. The minimum energy triggering latch-ups was in the range between 117 pJ and 124 pJ, for a nominal voltage of 1.25 V (JONATHAS, 2018).

The threshold energy variation with the reduction of the VDD was also tested using a previously detected sensitive location. The sensitivity to single event latch-ups increased to 172 pJ near the voltage of 1.16V in VDD (JONATHAS, 2018), operational voltage just below the lower voltage corner of this technology. This results represent a real increase of 47% and is very important as the technique can be added to the already discussed strategies to improve the radiation tolerance, even without any major changes

to the circuit itself, just being necessary to design the ASIC to work in the lower voltage corner.

Another relevant fact was that the state of the memory seems to be related to its tolerance to latch-ups, being the word patterns 10b1111111111 and 10b0101010101 more vulnerable than the 10b0000000000. This reveals that a good idea is to have a zero filling routine when the memory is not being used, which is not done automatically in SAMPA, but could be easily done externally using I2C commands or even included as an upgrade in future versions.

The selected laser system has high spatial precision and due to that, it was possible to evaluate the memory surface in steps as small as a micrometer and even in a grid of 500 nm.

To obtain the latch-up spacial behavior in an automated way, a trigger signal was included in the measurement setup. This signal flags to an oscilloscope in the laser system when a possible latch-up current event occurred.

Crossing the data between the laser scan and the triggers from the chip latch-up events allowed the creation of a bitmap image showing the sensitive regions. The plot of this scan is presented in the figure 55.

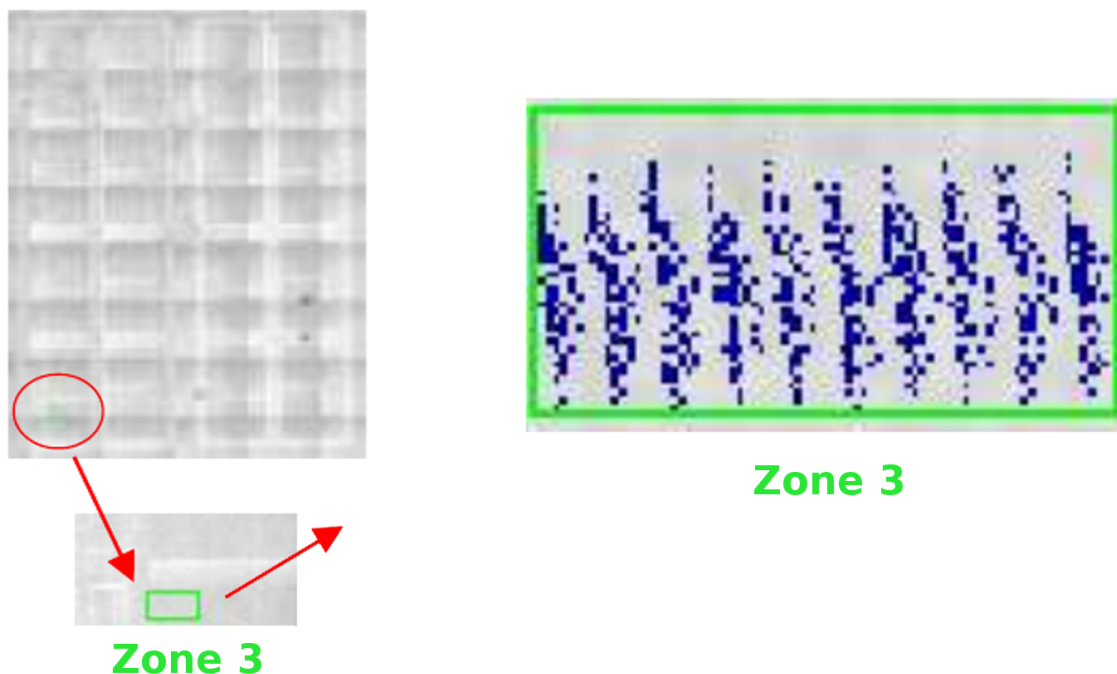


Figure 55 – The pedestal memory scan bitmap.

Source: The author and Jonathas (2018).

Figure 55 shows at its top left the micro-photography of the pedestal memory array, including 32 single port IPs. Also, a zoomed version is available at the bottom including the mark of the region of interest for the scan labeled as Zone 3 (in the green

box). The activation energy needed for this scan was just 131 pJ for each pulse, showing very constant sensitivity, and just over the minimum energy discovered in previous tests.

In the zoomed version of Zone 3 region provided at right of figure 55, an overlay of a serie of squares (in blue) are plotted, these dots correspond to the locations where the laser injection system detected latch-up events. It is also possible to see that there are vertical groups indicating a spatial periodic pattern. This may be correlated to the data region of the memory, which is usually based on a modular construction approach.

Evaluating the pattern revealed in the scan, ten columns are present and considering that the region measures about $40\ \mu\text{m} \times 21\ \mu\text{m}$ the average spacing of the columns found is in the order of $4\ \mu\text{m}$. This is an important result, providing an insight of the physical architecture causing the latch-ups. The distance and pattern can be cross-correlated to the spacing obtained for both compared IPs with the techniques of section 3.4.4, where the dual port minimum substrate polarization distance was smaller than the $4\ \mu\text{m}$ obtained with this laser scan, helping to explain why the dual port is less sensitive to the single event latch-ups.

Finally, focusing on a comparison between the SAMPA versions, the full area of the dual port memory used in SAMPA V3/V4 was scanned. The measured results were very positive and have not shown any latch-ups. Where even increasing the pulse energy, ranging from 48 pJ and going up to 1035 pJ, did not trigger latch-up events (JONATHAS, 2018).

The energy injected in this last tests was almost nine times the value needed to generate latch-ups on the previous memory, showing the applicability and the clear improvement when choosing this solution for the problems found in SAMPA V2 in relation to latch-ups, where with this successful results, this investigation was closed.

As a final comparison, table 12 provides a compact reference for the main characteristics, tests and results of SAMPA MPW1, V2, V3 and V4. SAMPA V4 was the final design approved by CERN, being composed of more than 120 thousand data flip-flops of which more than 83% are related to protected logic.

4.4 The MPW5 test chip irradiation

SAMPA V4 design was approved to be used in CERN ALICE (ALICE TPC COLLABORATION *et al.*, 2021), but targeting in new applications an extension of the project was proposed and named SAMPA V5. This new ASIC was targeted to be used in the sPHENIX detector at the BNL and consists in a 32 channel SAMPA with modified analog front-end and improved ADC. This project also included a testing MPW run which was named SAMPA MPW5.

Table 12 – Comparison between the irradiated SAMPA versions

	SAMPA MPW1	SAMPA V2	SAMPA V3	SAMPA V4
Channels	3	32	32	32
Memory	DFF based	SRAM IP	SRAM IP	SRAM IP
Memory IO	Single/Dual Port	Single/Dual Port	Dual Port	Dual Port
Max frequency	160 MHz	320 MHz	320 MHz	320 MHz
Configuration	DFF based	TMR DFF	TMR DFF	TMR DFF
Slow control	Serial	TMR I2C	TMR I2C	TMR I2C
Filters	BC1, DS, BC2 and ZSU	BC1, DS, BC2, BC3 and ZSU	BC1, DS, BC2, BC3 and ZSU	BC1, DS, BC2, BC3 and ZSU
DFT	none	JTAG and 5 scan chains	JTAG and 5 scan chains	JTAG and 5 scan chains
Shift register size	15000	121295	122980	122980
Irradiations	protons	protons/heavy ions	heavy ions	heavy ions
SEU cross-section	$7 \cdot 10^{-14} \text{ cm}^2$ per DFF	$3.51 \cdot 10^{-14} \text{ cm}^2$ per SRAM bit	$4.9 \cdot 10^{-14} \text{ cm}^2$ per SRAM bit	$4.9 \cdot 10^{-14} \text{ cm}^2$ per SRAM bit
SEL cross-section	$<5.8 \cdot 10^{-12} \text{ cm}^2$	$3.3 \cdot 10^{-3} \text{ cm}^2$	$<6.9 \cdot 10^{-8} \text{ cm}^2$	$<6.9 \cdot 10^{-8} \text{ cm}^2$
Pulsed laser test	not done	sensitive IP found	not done	insensitive

This MPW included several prototype chips and one of them implemented the test of the front-end connected to ADC and a small digital output section. Using the spare area left in this chip, several digital test blocks and new designs related to the present work have been fabricated, where the most relevant were optimizations of the BC2 filter and alternatives to the ADC digital structures.

The next section will address the main characteristics of the ADC control part and the results of several measurements made over this design in irradiation sessions executed in the Pelletron particle accelerator at IFUSP.

4.4.1 SAR ADC tests and analysis

Each of the 32 analog front-ends in SAMPA culminates in an analog to digital converter (HERNÁNDEZ *et al.*, 2020; HERNÁNDEZ, 2015). These converters are based on the successive approximation architecture and built as mixed signal blocks controlled by an internal digital subsystem.

This digital block is responsible to coordinate the capacitive DAC and calculate the output digitized value using the responses from a comparator. The block in question was identified as the SAR Register (*sar_reg*) and shown in the schematic of the figure 12.

The present section is intended to show the SAMPA ADC characteristics and weaknesses, also confirming the block response during a real irradiation. New alternatives to the digital block are also discussed, implemented, fabricated and tested.

The *sar_reg* block will be the focus here as it contains most of the ADC digital

circuitry. The design in question is based on a state machine controlled by the comparator providing as output the digitized data word and two complementary vectors that control the capacitive DAC inputs.

The first remarkable characteristic found when analyzing SAMPA ADC state machine was that its reset is asynchronous and controlled by the sampling clock, resetting the machine at each new conversion.

This fact was associated to have two major impacts, the first is that a SET in the lines feeding this resets can easily reset the full block as it has no filtering or synchronization to the main SAR clock. This can possibly cause metastability, wrong conversions and conversions with different sampling periods than the desired, where this can be considered as distortion.

The SET can also act just partially in the block (due to the asynchronous nature of the reset), corrupting the conversion and producing wrong digitized data, which is bad for the experiment and is a kind of data loss.

Both cited cases can also have additional drawbacks on the receiver side (on the DSP block), as these extra conversions in unexpected times could cause timing violations and meta-stability in the first register layer or further.

The asynchronous reset has several problems, but on the other hand, can be used to promptly clear the full block in case of a SEU or SET returning its state to an operational point. In the case of SAMPA, this is made continuously and in the frequency of the sampling clock, which may limit the duration of a fault to just one sampling period.

The ADC also has a synchronous section based on standard flip flops. This part is responsible to keep the current state and also to store the final digitized value. The final output was registered to relax the timing constraints of the inputs in the next block.

The ADC digital section is in fact not protected, being vulnerable to single event upsets which can lead at least to two main problems. The first is the corruption of the output data after a successful conversion. It can happen while the achieved result stored in the last register is waiting to be acquired by the digital signal processor. This corruption usually appears as bit-flips in the ADC value, destroying the sample data.

The second vulnerability appears when the SEU happens in the registers of the SAR state machine. This can lead to undesirable behavior and bad control of the analog blocks activated by this state machine, as the sampling and capacitive DAC switches. After an event like this, at the end of the cycle, an unexpected result may be achieved and experiment data will be lost. This circuit has an additional aggravating factor, it runs much faster than the output register, being more active in a factor of ten in relation to the sampling clock.

Due to this set of weaknesses, an irradiation was planned aiming the evaluation of the real behavior of this block when exposed to interactions with a controlled particle flow.

Figure 56 shows the test board used in the irradiation tests of this ASIC. No digital components were included in this board except for the test chip itself. Voltage regulators are present but they already were validated to tolerate the exposed dose in these tests.

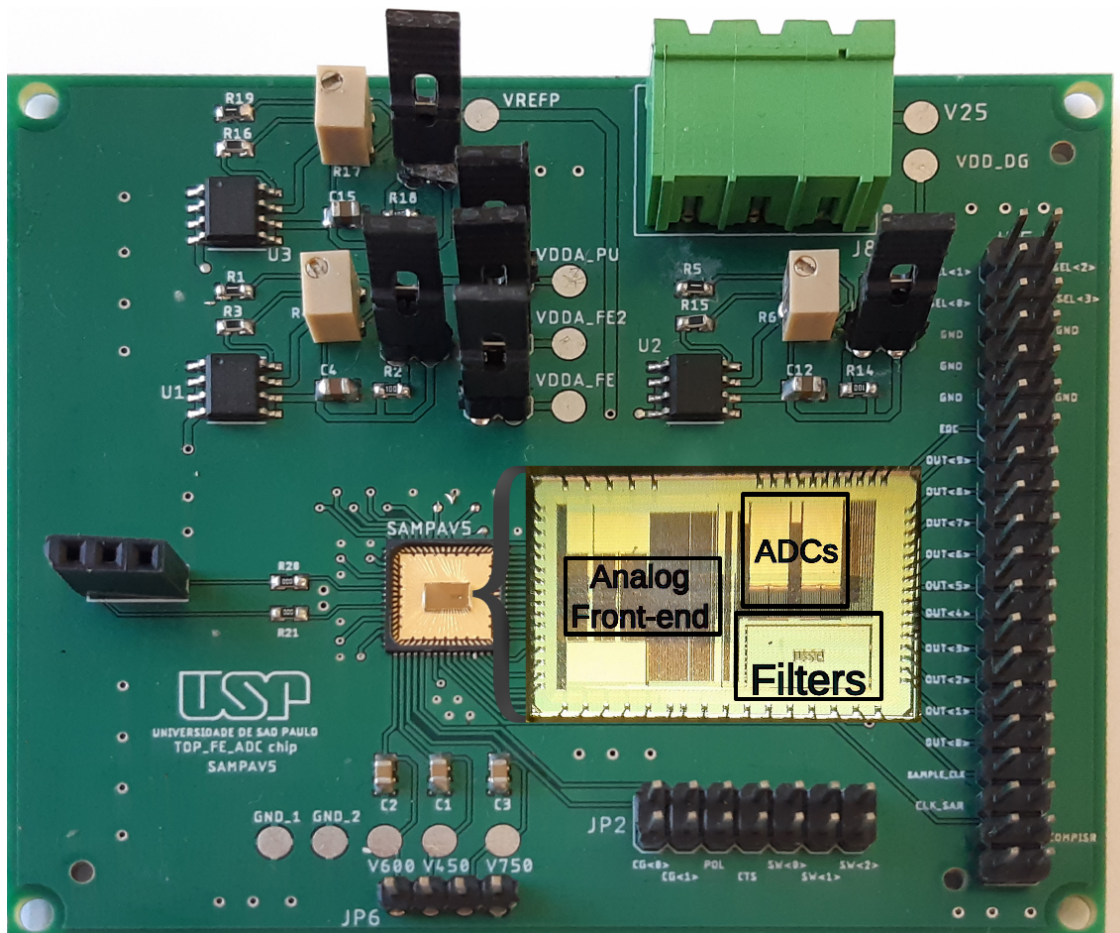


Figure 56 – Test board with the opened package and a zoomed version of the die.

The chip was housed in an open window quad-flat no-leads (QFN) 64 package to permit the irradiation testing of the die with more exposure and precision. Fig. 56 also provides a micro-photography of the die at the side of the packaged version. The total test chip area was $3346 \mu\text{m} \times 2120 \mu\text{m} = 7.1 \text{ mm}^2$.

The micro-photography provides rectangular marks showing the three main structures in this ASIC. The front-ends, the ADCs and the Filters digital block. The front-end is totally analog and will not be part of this work, the ADC section contains a pair of standard SAMPA V5 10 bit ADCs, without protection and the filters section is a multi-purpose digital block containing digital filters, test structures, shift registers and several implementations of the ADC SAR circuit.

The chip includes a set of selection input bits $sel[0:3]$ to permit the testing data

acquisition system to choose which part of the chip to test or even just access the bare ADCs direct output.

The test setup was based on the board shown in Fig. 56 connected to a SocKit Cyclone V System-on-Chip FPGA board. A data acquisition software was developed in C and run over a Linux operating system in a dual-core ARM hard processor system (HPS). The software automatically performs functional tests over the blocks in the ASIC, monitoring and accounting for any detected anomaly.

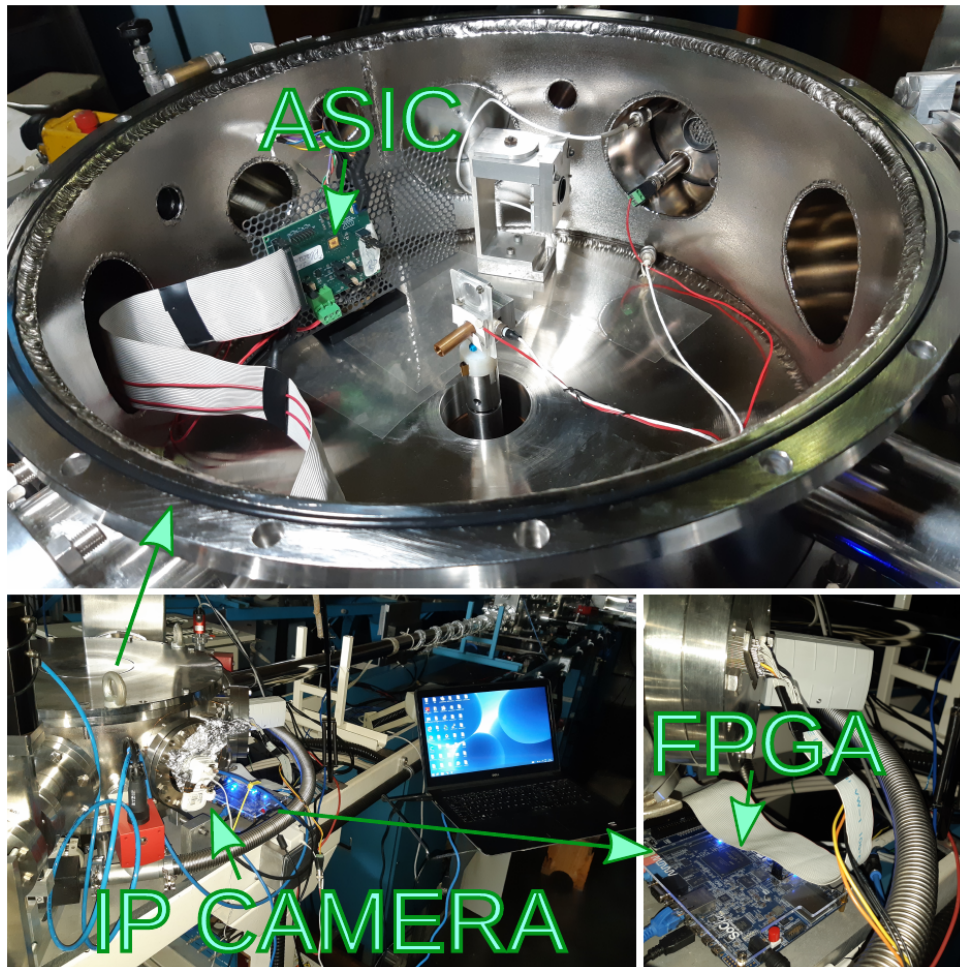


Figure 57 – Pelletron accelerator ASIC irradiation setup.

Figure 57 illustrates the actual irradiation setup used during the tests in the Pelletron particle accelerator. The bottom left picture shows a general view of the environment, where it is possible to see the test chamber being monitored by a notebook and an IP camera. This was needed to permit remote access during the tests, avoiding human exposition during the irradiation. At the bottom right is provided a zoom over the FPGA. This board was placed outside of the irradiation chamber, minimizing the chances of the data acquisition system running in it fails due to single events.

The top image in figure 57 provides a clear expanded view of the opened vacuum chamber where the particles hit the DUT. The test board of figure 56 can also be identified,

where the ASIC is highlighted.

As mentioned early, this section starts analyzing the ADC and its irradiation results, but the same package, die, board and test setup will be used for all remaining tests and for compactness will not be further addressed.

Table 13 shows some of the available ions in the IFUSP Pelletron facility, including their energy and LET. Additionally, a radioactive calibration source providing an alpha particle flow of 5 MeV energy and 0.65 MeV/(mg/cm²) LET was also used. The cited particles were selected for this section and keep as a reference for all the irradiations targeting the board shown in figure 56.

Table 13 – Selected beams characteristics

Particle	Energy [MeV]	Range [μm]	LET [$MeV/(mg/cm^2)$]
¹⁶ O	44	28	6.4
²⁸ Si	57	18	13.6
³⁵ Cl	58	14	17

Being the test environment briefly described, it is possible to focus on the ADC irradiation and its results. The ADC test was performed running conversions and checking the behavior of the output pins, searching for anomalies.

Some of the possible events that can be detected include output data SEUs, fake pulses on the end of conversion pin and undesirable conversion requests.

Aiming to protect the quality of the acquired data, one extra feature was included in the output bus. In this chip, a parity bit is sent in conjunct with each sample of result data. This strategy permits that a SET in the output PADs be separated from a problem in the internal block being tested, reducing the error sources of the experiment.

The ADC irradiation was then performed in four distinct runs in the chamber. Table 14 shows the details of each one, where the run name will be used as a general identifier of each test in this thesis and always in the format composed by the character t followed by an identification number. The test with the alpha particle source was discarded due to its extreme low event count and statistical quality. The alpha particle run was mainly used as an environment and data acquisition test in free periods where the accelerator could not be used or was scheduled for other users.

From the data on table 14 is clear that the block in question had a considerable amount of errors in a small period of time, showing its sensitivity to the exposed environment. The Events column corresponds to the sum of any detected error that happened in the device. It is important to note that no PAD errors were detected by the parity bit,

Table 14 – ADC irradiation runs

Run Name	Particle	Duration [s]	Flux [$10^3/cm^2s$]	Fluence [$10^6/cm^2$]	Events
t4	^{16}O	260	105.3	27.5	691
t8	^{16}O	450	819.0	368.2	5932
t13	^{28}Si	483	12.6	5.8	11222

indicating that the block was probably fully responsible for the errors.

Focusing on metrics for comparison with future variations of this block, the test data was processed and the cross-sections were estimated. The obtained values for ^{16}O and ^{28}Si were respectively $(1.67 \pm 0.04) \cdot 10^{-5} \text{ cm}^2$ and $(1.93 \pm 0.04) \cdot 10^{-3} \text{ cm}^2$.

These cross-sections numbers indicate that the block was more vulnerable to the ^{28}Si ion and when checking the data manually it had severe losses and malfunctions showing its fragility. Most of the failures were followed by good conversions, showing that the block was not hardly damaged by the previous event, re-enforcing that a SEU or SET was the error source, not a burnout event, latch-up or worse.

The failure levels found in the ADC are not negligible and can impact significantly on the converted experimental measurements. In order to understand and improve the *sar_reg* control block of the ADC, several alternative versions of this circuit were built to demonstrate in a real irradiation, the individual characteristics of different design strategies.

The analysis was divided into two main topics, one regarding the coding of the state machine and the other in relation to the redundancy architecture used for protection. Additionally, the role of the asynchronous reset was evaluated, where for the new alternatives synchronous resets were used. This change was motivated by the strong suspicion regarding observed errors and other events of the asynchronous implementation, raised during the tests reported in the table 14.

Table 15 provides a list of the designed blocks according to the architectures and redundancy options selected, where all of them were manufactured in the 130 nm process. The initial lines of the table present comparatively the ADC of SAMPA (already tested) as ADC0 and ADC1 (both functionally equivalent) and a version with parity in the outputs to check for SET in the PADs. The following blocks were incrementally identified from *sar_reg03* to *sar_reg08* focusing on the alternatives with synchronous reset where for the binary and one-hot coding, 3 different blocks were implemented. This intending to comparatively explore the protection alternatives with triplication by register and by module.

The encoding alternatives were based on the use of binary values for each SAR conversion step (in the first option) and one hot encoding (LIU, 2017) (for the second implementation alternative), where each SAR step was direct encoded as one active bit (as the one hot name suggests).

Table 15 – List of the ADC implementations and their main characteristics

Block ID	Name	Encoding	Protection	Reset
ADC0	SAMPA V5 ADC	one hot	none	asynchronous
ADC1	SAMPA V5 ADC	one hot	none	asynchronous
ADC0P	SAMPA V5 ADC + Parity	one hot	none	asynchronous
sar_reg_03	sar_reg5_notmr_hot	one hot	none	synchronous
sar_reg_04	sar_reg5_tmr_hot	one hot	TMR	synchronous
sar_reg_05	sar_reg5_mod_hot	one hot	Modular TMR	synchronous
sar_reg_06	sar_reg5_notmr_bin	binary	none	synchronous
sar_reg_07	sar_reg5_tmr_bin	binary	TMR	synchronous
sar_reg_08	sar_reg5_mod_bin	binary	Modular TMR	synchronous

Several irradiations were performed over the described blocks using the ions ^{16}O , ^{28}Si and also alpha particles. Due to low event count, the alpha particle test and $t3$ were discarded. The run $t3$ was a quick ^{16}O run for 300 seconds with a flux of $104.7 \cdot 10^3/\text{cm}^2\text{s}$.

The runs named $t7$ and $t14$ had several events and were used in a way to compare the results of the alternative blocks listed in table 15 with the tests of SAMPA ADC.

To obtain a fair comparison between the blocks, one extra consideration was taken into account, the test should have similar fluxes making the effects happening in parallel comparable in the distinct evaluations. Using this approach, the table 16 was compiled, unifying the results of SAMPA ADC with the results of the alternative *sar_reg* blocks, easing the evaluation and grouping it by the ions and similar fluxes. In this table, the fluxes are denoted in thousands of particles per second per square centimeter and the fluence in million particles per square centimeter.

Table 16 shows a rich amount of cross-section data for the distinct implementations and situations, where the device was exposed to low, medium and high fluxes achieving a large range of fluences.

To start the analysis, it is possible to clearly see that there is a huge difference in the global cross-section values between the SAMPA ADC and the other implementations, and this happens for all particles and fluxes. This fact is even more discrepant when

Table 16 – Comparison between the different SAR implementations results

Block ID	Ion Name	Run Name	Flux [$10^3/(\text{cm}^2\text{s})$]	Fluence [$10^6/\text{cm}^2$]	Event Count	Cross-section [cm^2]
SAMPA ADC	^{16}O	t4	105.3	27.5	691	$(2.51 \pm 0.11) \cdot 10^{-5}$
sar_reg_03	^{16}O	t5	167.9	35.7	1	$< 1.56 \cdot 10^{-7}$
sar_reg_04	^{16}O	t5	167.9	35.7	0	$< 8.39 \cdot 10^{-8}$
sar_reg_05	^{16}O	t5	167.9	35.7	0	$< 8.39 \cdot 10^{-8}$
sar_reg_06	^{16}O	t5	167.9	35.7	13	$(3.65 \pm 1.01) \cdot 10^{-7}$
sar_reg_07	^{16}O	t5	167.9	35.7	0	$< 8.39 \cdot 10^{-8}$
sar_reg_08	^{16}O	t5	167.9	35.7	0	$< 8.39 \cdot 10^{-8}$
SAMPA ADC	^{16}O	t8	819.0	368.2	5932	$(1.61 \pm 0.03) \cdot 10^{-5}$
sar_reg_03	^{16}O	t7	918.5	291.9	140	$(4.79 \pm 0.41) \cdot 10^{-7}$
sar_reg_04	^{16}O	t7	918.5	291.9	0	$< 1.03 \cdot 10^{-8}$
sar_reg_05	^{16}O	t7	918.5	291.9	0	$< 1.03 \cdot 10^{-8}$
sar_reg_06	^{16}O	t7	918.5	291.9	102	$(3.49 \pm 0.35) \cdot 10^{-7}$
sar_reg_07	^{16}O	t7	918.5	291.9	0	$< 1.03 \cdot 10^{-8}$
sar_reg_08	^{16}O	t7	918.5	291.9	0	$< 1.03 \cdot 10^{-8}$
SAMPA ADC	^{28}Si	t13	12.1	5.8	11222	$(1.93 \pm 0.04) \cdot 10^{-3}$
sar_reg_03	^{28}Si	t14	11.0	7.1	0	$< 4.22 \cdot 10^{-7}$
sar_reg_04	^{28}Si	t14	11.0	7.1	0	$< 4.22 \cdot 10^{-7}$
sar_reg_05	^{28}Si	t14	11.0	7.1	0	$< 4.22 \cdot 10^{-7}$
sar_reg_06	^{28}Si	t14	11.0	7.1	42	$(5.92 \pm 0.92) \cdot 10^{-6}$
sar_reg_07	^{28}Si	t14	11.0	7.1	0	$< 4.22 \cdot 10^{-7}$
sar_reg_08	^{28}Si	t14	11.0	7.1	0	$< 4.22 \cdot 10^{-7}$

looking to the big amount of error events recorded in these devices, and in this way, it should be understood as that can have relevance for the real application of the device.

Searching for a closer comparison, the most similar implementation to the SAMPA ADC can be found in table 15 as *sar_reg_03*. This alternative is basically designed with the same architecture and encoding scheme, but implemented with the synchronous reset.

Going back to table 16 and comparing the SAMPA version with the *sar_reg_03*, a considerable bigger cross-section and error rate is found in the SAMPA case, where the major difference is the asynchronous reset. This can also be checked for several other run

cases including t4 versus t5, t8 versus t7 and t13 versus t14.

With these facts, a relevant hypothesis can be stated, this design should have the amount of asynchronous nets minimized, as they have shown to increase the sensitivity of the block to the interactions.

Further observations can also be made in the provided results of table 16, where focusing on higher flow situations (like the t7 run of ^{16}O), there were significant differences in the cross-sections between *sar_reg_03* and *sar_reg_06*.

These versions have as main difference the change of the coding used in the states thus, it can be said that a slightly worse performance happened when using the one-hot coding in the state machines as it is observed comparing the results.

This fact can have several reasons, both functional due to different behaviors derived from changing a bit and its propagation in each of the implementations, as well as issues related to the physical area exposed in case the one-hot coding, that is bigger, given the greater number of flip-flops involved. It is also relevant to note that t5 and t14 runs were not used for these comparisons, given the low flow and the consequent reduced number of events.

It is also observable that, under these conditions, no considerable difference was found in the change of redundancy to the bigger modular strategy and both redundancy alternatives have been successful, even with particularly high flows of the order of $0.9 \cdot 10^6/\text{cm}^2\text{s}$.

Finally, it is possible to state that there are positive results concerning the evaluation of the inserted protections since, for all cases with some level of redundancy, no errors were registered. And this scenario was repeated for all the bundles and all the flows illustrating a great improvement in relation to the older versions in this aspect.

The prototype ASIC shown in figure 56 also contained other blocks which are used in the SAMPA digital signal processor, the next subsection continues with the analysis and results of the FIR baseline correction filter irradiation.

4.4.2 FIR baseline correction filter

Several readout front-ends, including the SAMPA ASIC itself, have digital filters in their signal processing chain (GARCIA, 2012; BOSCH *et al.*, 2003; HERNÁNDEZ *et al.*, 2020). A relevant filter used in TPCs is based on an FIR section with thresholds, being known as BC2 in SAMPA, as described in section 3.2.

During the irradiations of the full SAMPA V2 prototypes unexpected behaviors have been detected in the estimated baseline of BC2 filters, culminating in output data loss and the need for external actions to resume the operation (MAHMOOD, 2020).

Due to these facts, BC2 filter was elected to be an analysis case for the artificial intelligence algorithm of chapter 3.4, trying to understand the possible vulnerabilities and countermeasures to improve it (SANCHES; NOIJE, 2021).

The optimizer was set to run with the filter as its target and focusing on 3 main minimization targets: area, power and malfunction rate. To perform that, the fitness function was implemented as a weighted combination of 60% of the area and 40% of the power (SANCHES; NOIJE, 2021).

The radiation tolerance was included in this metric as a factor that bad rate solutions which do not perform well in single event injection tests. These are made in simulations after the gate level generation in the optimization loop shown in figure 42.

To cope with that, each solution was checked using testbenches of several kinds. These included simple standard runs, single upsets injections and various modes of multiple events failures. At the end, the error output results were delivered to the fitness function, possibly reducing the solution scores and balancing the fitness evaluation, now including the single events.

It is important to note that the fitness function was made negative as the fitness of the individuals more adapted should grow. To ease the visualization and understanding, the values of power and area were normalized by the pre-optimized design results.

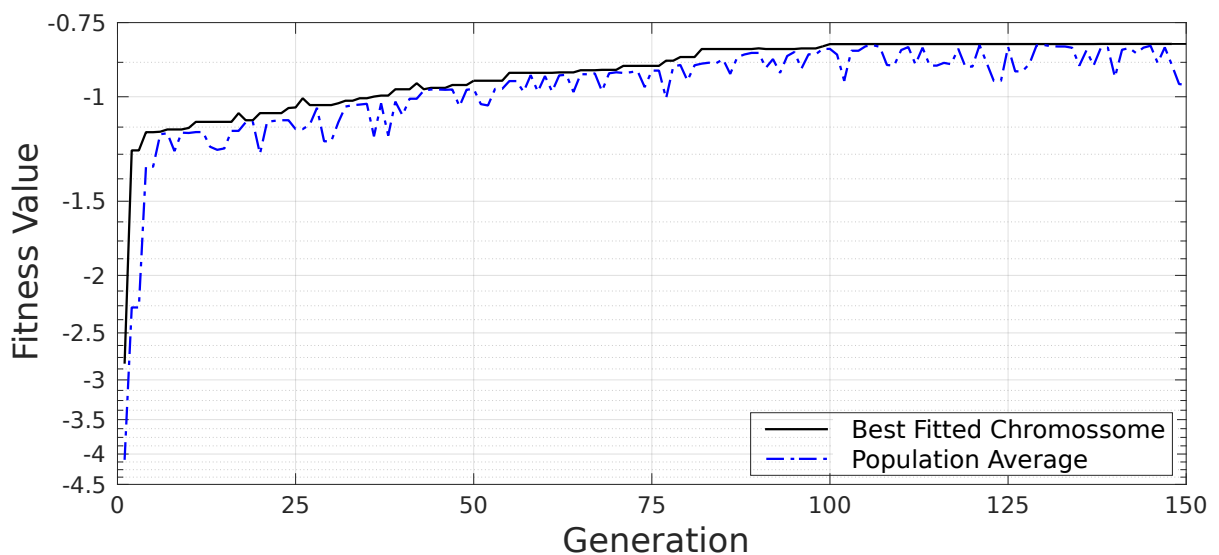


Figure 58 – Evolution of the population fitness along the generations in the optimizer.

The algorithm was run over BC2 with a population size of 200 and a maximum iteration number of 150, taking about a day to complete; where logging the output metrics per generation permitted the creation of a monitoring graph. Figure 58 presents the evaluated fitness evolution of the best chromosome in the population along with the generations during the optimization loop.

The curve in figure 58 shows that the fitness was growing and it had been considerably improved during the execution. The graph, in addition, shows that the average fitness of the population is progressing in direction to the best value, but the search path causes fluctuations due to the inherent nature of the evolutionary algorithms.

A possible maximum value was found after iteration 138, where the best chromosome ceased to improve at the value of 0.8147 (negative). The algorithm continued to run up to generation 150 achieving its stop condition, but no further changes have been registered.

This best solution was converted to System Verilog, being synthesized and its gate level evaluated. The simulations have passed, indicating a valid working filter with functionality compatible with the original design, but now including several internal redundant devices.

With a valid resulting code available, it is important to investigate the design changes proposed by the optimization algorithm and understand their causes and effects. The designs were then compared and the main MACROs inserted were noted.

In a brief description, the obtained solution majority directs the designer to use triplication in most of the MAF pipeline registers (Z_i), but with some exceptions. Parts of the static configuration bits could be set to be block encoded with hamming (implementing single error correction per variable). The flag pipeline presented in figure 23 also received this kind of redundancy.

Knowing that, a focused analysis of the single event injection simulations could be made. Thus, pairing the proposed design with the original reference behavior could clarify the path to track the reasons that guided the optimizer to insert protection. The method is also relevant to search for the origins of the problems measured in (MAHMOOD, 2020) due to single events effects in this filter.

The discovered root cause was that there is a trade-off between area and power versus hardening when implementing the reduction of MAF using (eq. 3.7). In standard operation, the design is fine and more than halves the power and area in BC2. But in an aggressive environment, it exposes the chip to unrecoverable faults caused by both SEUs and SETs. These errors are justified by the inherent fragility imposed by the unprotected data delay pipeline shown as $Z8$ to $Z0$ in Fig. 24 (SANCHES; NOIJE, 2021; SANCHES; NOIJE, 2020).

This work provides a solution for these sensitive points with an alternative BC2 block which includes a MAF filter that uses the TMR MACRO in its flip-flops, tolerating one upset per bit per clock cycle. The main idea is to triplicate the data delay pipeline registers $Z8$ to $Z0$ and the *previous baseline* register, where each register of this set will be replaced by a trio followed by a majority voter.

These added devices will contribute with extra power and area but in this solution,

each set of three registers will have a much lower final upset cross-section needing at least double errors per original register to corrupt the data pipeline.

To validate this work, three BC2 filters have been designed and prototyped. The first design is a reference unprotected filter identified as NOTMR (id: BCII_c12_NOTMR). The second was the BC2 used in SAMPA, which included triplication in the control sections and protection with watchdog counters to auto-reset the filter in case of problems. The third design is an extension of the SAMPA version where the MAF filter was protected using TMR.

The test setup used was exactly the same as the one shown in figures 57 and 56 being the changes predominantly on the software side, which runs in the embedded Linux at the FPGA board, aiming the control and detection of anomalies in the filter outputs.

In this campaign, five irradiation runs were executed over BC2, being three using ^{16}O , one ^{28}Si and one ^{35}Cl . The last three runs were selected to be further evaluated due to the higher fluence and greater quantity of detected errors, reducing the measurement uncertainty.

Table 17 provides the test data for the selected runs, including the resultant calculated cross-sections. In the table, fluxes are shown in thousands of particles per second per cm^2 and fluences in million particles per cm^2 .

Table 17 – BC2 irradiation results

Block Name	Ion Name	Run Name	Flux [$10^3/(cm^2s)$]	Fluence [$10^6/cm^2$]	Cross-section [cm^2]
BCII_c12_NOTMR	^{16}O	t9	819	231.0	$(1.69 \pm 0.27) \cdot 10^{-7}$
BCII_c13_SAMPA	^{16}O	t9	819	231.0	$(7.79 \pm 1.84) \cdot 10^{-8}$
BCII_c14_TMR	^{16}O	t9	819	231.0	$(2.60 \pm 1.06) \cdot 10^{-8}$
BCII_c12_NOTMR	^{28}Si	t12	13.8	6.4	$(3.46 \pm 0.74) \cdot 10^{-6}$
BCII_c13_SAMPA	^{28}Si	t12	13.8	6.4	$(1.73 \pm 0.52) \cdot 10^{-6}$
BCII_c14_TMR	^{28}Si	t12	13.8	6.4	$(9.43 \pm 3.85) \cdot 10^{-7}$
BCII_c12_NOTMR	^{35}Cl	t16	2.5	1.1	$(4.76 \pm 2.14) \cdot 10^{-6}$
BCII_c13_SAMPA	^{35}Cl	t16	2.5	1.1	$(9.52 \pm 3.03) \cdot 10^{-6}$
BCII_c14_TMR	^{35}Cl	t16	2.5	1.1	$(5.71 \pm 2.34) \cdot 10^{-6}$

In table 17 it is possible to notice that the cross-sections are ascending with the LET, which is expected, and it is also notable that the uncertainties are increasing, this due to the higher difficulty to keep with elevated error event rates as the LET increases.

This happened mainly because of the lower fluxes achieved in Pelletron for heavier ions and also due to schedule time limitations. The results for ^{35}Cl had considerable uncertainty and is difficult to separate the cross-sections there, being just the initial points clear to be used in the subsequent analysis as they have higher event count.

Comparing the errors and cross-sections between the different fabricated designs shows that the unprotected version (BC2_NOTMR) is more sensitive than the SAMPA V4 version and the version with TMR protected data-path.

The SAMPA V4 version also shows advantages in relation to the unprotected filter, this can be justified as it has triplication in its control parts but still had detected faults in the past and in this test also.

The present work proposed the additional protection of the filter data-path, which was tested, and as shown in the measurements, increased the tolerance to the particle flow, achieving a reduced cross-section. These measurements help to state that this part of the block was possibly guilty for some of the observed faults in the past, both by this work and Mahmood (2020).

The results also show the importance of the radiation effects evaluation in the design phase, showing again that with automated analysis before SAMPA submission several weak points may have been detected and fixed. Artificial intelligence techniques as the ones discussed here may have a relevant role in big projects, helping the designers to achieve balanced optimized results with reduced manual effort.

4.4.3 Applicability and comparisons

It is important to evaluate practical metrics and provide comparisons involving the trade-offs to confirm the applicability and improvements made in the previously addressed designs.

The circuits in question have been tested and their cross-section obtained for different scenarios. With these values, it is possible to estimate the mean time between failures, which is a helpful number when developing an experiment. It is also relevant to note that for this analysis the word failure will be understood as an error or simple malfunction (as in cross-section evaluation experiments). A failure should not be understood as a complete device fault or permanent damage.

Starting by the *sar_reg* block and assuming the reference environment as CERN ALICE TPC, an estimation of the flux is needed. Thus an average particle flux of $3.4 \cdot 10^3 / \text{cm}^2\text{s}$ was chosen from Antonioli, Kluge and Riegler (2013) to be used in the calculations.

With the flux, it is possible to obtain the error rates from the cross-sections in

table 16. For these evaluations, the data were based on the ^{16}O beam, due to its reduced error margin and greater statistical content.

Table 18 provides the obtained mean time between failures together with the number of cells (total standard cell instance count), instance area [μm^2] (sum of individual cell areas), total block area [μm^2] (the real implementation area including routing and physical cells) and density (the percentage of the full design with useful standard cells). The detailed block architectures and names were defined in table 15.

Table 18 – SAR register comparison

Block ID (Name)	Cell Count	Cell Area [μm^2]	Final Area [μm^2]	Design Density	MTBF [s]
ADC0 (SAMPA ADC)	94	1845	7432.56	24.82%	< 20
sar_reg_03 (notmr_hot)	116	1673	7345.28	22.78%	< 566
sar_reg_04 (tmr_hot)	272	4375	7345.28	59.56%	> 28000
sar_reg_05 (mod_hot)	416	5935	7345.28	80.80%	> 28000
sar_reg_06 (notmr_bin)	114	1561	7345.28	21.25%	< 766
sar_reg_07 (tmr_bin)	249	3691	7345.28	50.25%	> 28000
sar_reg_08 (mod_bin)	413	5581	7345.28	75.98%	> 28000

Initially, it is possible to observe that all versions in table 18 had similar final areas, this fact is explained due to the fact that the design in (HERNÁNDEZ *et al.*, 2020) was implemented with reduced density and with this information, one design restriction was added to the protected designs, aiming to replace the original control block with a better one but without using any extra area.

The data in table 18 confirm that all the developed designs achieved a final area slightly smaller than the first (reference) implementation. This makes the blocks interchangeable, as the pin-out was made compatible.

Now focusing on the mean time between failures, the first entry (HERNÁNDEZ *et al.*, 2020; ADOLFSSON *et al.*, 2017) resulted in a very low MTBF value (smaller than a minute), which can indicate very frequent failures in the converted data, a fact that justifies the existence of this section.

Comparing the first line with the synchronous strategies notmr_hot and notmr_bin, which shows a considerable improvement of about thirty times in the mean times. An extra time margin also appears when using a binary coded scheme for the state machine. This implementation additionally obtained the combined advantage of having an instance area almost 7% smaller than the one hot alternative and almost 15% smaller than the

reference asynchronous reset one hot design of the first line.

The remaining implementations include redundancy and compare different strategies concerning coding and architecture. Focusing on the MTBF results, all four TMR versions obtained a noticeable improvement in relation to the reference implementation of the first line, being the per module and per register redundancy options effective.

The protected implementations achieved MTBFs thousands of times greater than the unprotected version which is a big advantage. But it worth saying that, up to the energy and fluence used in these tests, no conclusive measured difference was observed between the modular and per register TMR alternatives.

As the MTBF was considerably better for all the protected versions, the *Cell Area* was analyzed in a way to classify the implementations. The total area was not used as the blocks were similar in this parameter due to design restrictions targeting the replacement of the original block.

The data also show that protection using redundancy involving the full module implied in an area increase of around 30% on average for this case, as the per module approach includes substantially more logic than in the per register version.

The state machine coding had also an impact in the cell area, where for the one hot encoding an average extra area of 10% was used to accommodate the added flip-flops and combinatory conversion logic.

Finally, as the block is targeted to an application where it is continuously refreshed, and the alternative redundancy versions have not shown expressive improvements, it is possible to conclude that the most relevant and economic alternative was the SAR ADC version with TMR in binary coded states (`sar_reg7_tmr_bin`), implying in improved protection with a cell area reduction around 38% in relation to the modular one-hot design with similar MTBF.

Moving the focus to the BC2 digital filter, it is also relevant to obtain the mean time between failures and compare the different irradiated versions. Initiating by the unprotected version of the block, it was obtained that the errors may happen with an average interval of 25 minutes at TPC environment ($3.4 \cdot 10^3$ particles/cm²s).

In the case of the BC2 implemented in SAMPA, with partial protection, the failures would have around 51 minutes between then on average. Finally, the BC2 with data-path TMR protection has an average time between the errors of 2 hours and 14 minutes.

The growing MTBF intervals show that the protected versions may have operational advantages in the system and is notable that the SAMPA version is better than the unprotected one. Also it is very important to highlight that the TMR version with protected data-path was successful, obtaining an improvement in the average filter error-free run

time of more than 430%, a relevant advantage.

A comparison between the three proposed versions and the works in the state of the art is provided in table 19, showing the trade-offs between area, power and the functional performance that the hardened device achieved. The power values provided are for the frequency of 20 MHz, where standard usage modes vary between 5 MHz to 20 MHz (HERNÁNDEZ *et al.*, 2020).

Table 19 – Comparison between several BC2 filter implementations

Filter	Bosch <i>et al.</i> (2003)	Garcia (2012)	This work		
			NOTMR	SAMPA	TMR
Instances	1470	924	931	1038	2580
Process [nm]	250	130	130	130	130
Area [μm^2]	84079	15665	15969	17539	39939
Power [μW]	1352.2	265.1	283.1	316.7	690.0
Power / MHz	68	13	14	15	34
Lockout free			YES	YES	YES
SEU protected	YES			CONTROL	YES
Restores upset			YES	YES	YES

The two first columns show works from the literature targeting similar filters for TPCs. The first column provides the replica results of Bosch *et al.* (2003) which may perform adequately in radiation in respect to SEU, but can be stuck out of its calculation range by specific signals that make the double threshold scheme (GARCIA, 2012) to fail, locking the baseline tracking fundamental functionality (SANCHES; NOIJE, 2020).

The work Garcia (2012) uses less power and area but in the same way as the first work, can be locked out of the range and also had problems with unrecoverable baseline jumps due to SEUs (SANCHES; NOIJE, 2020).

With a small increase of area, the SAMPA V4 watchdog monitored BC2 filter of column 4 could solve the problem of the filter getting stuck outside its calculation range (SANCHES; NOIJE, 2020). This filter is not fully triplicated, so it still has the exposed data pipeline vulnerabilities addressed in Sanches and Noije (2020), but the capacity of re-evaluating the operating point is enough to recover from upsets in the baseline. In this way, errors may happen but the filter restores itself back to an operational state, differently than the cited works in literature (GARCIA, 2012; BOSCH *et al.*, 2003).

The last filter shown in table 19 is fully protected, using TMR also on its data-path registers. This version was irradiated and showed improved behavior in relation to the undesired baseline erroneous events when compared to previous filters.

It is important to note that all novel proposed versions resulted in advantages over the first work, being the last much more resistant to single events in cost of extra

area and power. Additionally, the SAMPA filter with watchdog counter and FIR re-estimation (SANCHES; NOIJE, 2020) perform better than (GARCIA, 2012; BOSCH *et al.*, 2003).

Finally, a deeper analysis shows that is possible to fit the watchdog monitored filter in the same full chip area for a complete readout front-end ASIC as SAMPA. The state of the art (HERNÁNDEZ *et al.*, 2020) shows that a complete channel has an average area of 2.65 mm^2 where this filter changes it in just 0.07%, providing an acceptable solution with a viable strategy and using negligible extra area.

5 Conclusion

In this thesis, the development of a novel continuous readout 32 channel ASIC for gaseous detector systems in high energy particle physics was presented focusing on its largest block, the application specific digital signal processor.

The signal conditioning architecture was modified and a new lockout free non-linear filter named BC3 was implemented and included in complement to the existing filters resulting in an improved system capable of operating in the GEM based ALICE TPC. The BC3 filter was optimized and presents an average area reduction of 55% in comparison to a filter of similar application.

A novel artificial intelligence based optimizer was proposed focusing on the improvement of design metrics while increasing the tolerance to radiation using redundancy. The problem conversion was addressed and also the optimization loop was described using genetic algorithms along with state of art EDA tools. The algorithm included dynamic probability selection allowing the parameters to change depending on the search path and solution performance. The optimizer was validated with parts of the SAMPA design, where the BC2 filter is a notable block.

The BC2 filter was improved to avoid undesirable lockout behaviors and it was also corrected concerning vulnerabilities triggered by single events. The block received protection in detected critical parts and a watchdog timer with three distinct recovery alternatives. The protections could increase the MTBF of the filter by more than 430% and even in the event of a failure, there is still the auto-estimation watchdog mechanism. The inserted watchdog redirects the filter to a valid tracking state, reducing the need of external actions or monitoring and minimizing the data loss in case of a malfunction.

An iterative procedure for single event latch-up avoidance was proposed targeting the analysis of designs with IPs and black-boxes due to their inherent verification difficulties. The SAMPA was used as a test case and the evaluations resulted in the identification of a possible vulnerability and a guilty block, a single port SRAM IP.

The Pedestal single port SRAM of BC1 filter was changed to a different implementation to increase the system radiation tolerance to latch-ups and the filter also received a watchdog in its IIR section. This memory replacement was very effective and resulted in a reduction of the SEL cross-section in more than 99.99% at a cost of an area increase of 2.43%.

Additionally, a novel communication protocol for the readout ASIC was proposed, including packet based transmission through SLVS differential links. This targeted the

operation in a link exposed to single events being the packet headers SECDED protected and the data payload parity checked. The protocol can keep the receiver on track of the data and without uncorrected headers if the error count is below one at every 50 bits (2%), while the added redundancy corresponds only to 0.07% of the bandwidth in case of full data link usage.

In this work, several prototypes were fabricated aiming for concept, performance and radiation tests. The first taped-out MPW was composed of three chips. These carried the main composing blocks of the system along with a miniature version of the readout ASIC. The reduced system was composed of 3 analog channels, 3 ADCs, 3 channels of the digital processing section and structures to allow measurements in irradiation tests.

These chips were fabricated, mounted and measured showing satisfactory results. This engaged the development of a first complete chip version, the SAMPV V2. This prototype represented the first 32 channels chip of its kind in the state of art and included all the requirements for the newest 2021 upgrade at CERN ALICE.

SAMPV V2 was produced and tested in both chip on board and BGA assembled versions. The system showed a good performance and the results were as expected in its functional tests.

Irradiation runs were performed in both MPW1 and SAMPV V2 using protons and heavy ions. SAMPV MPW1 was used to obtain the flip-flop single event upset cross-section which was $(7.0 \pm 1.2) 10^{-14} \text{ cm}^2$ one acceptable value for the experiment. The MPW1 tests occurred without major issues being detected. On the other hand, SAMPV V2 irradiation tests had shown current increase artifacts which further have been attributed to single event latch-ups. The SEL cross-section was obtained for several heavy ions and was as high as $5.1 \cdot 10^{-3} \text{ cm}^2$ for ^{84}Kr (the ion with highest LET used). Requests for specification changes in the digital core and front-end in conjunct with the unacceptable SEL cross-section triggered the development of two new chip versions, the SAMPV V3 and SAMPV V4.

With the feedback of the proposed single event latch-up avoidance procedure, the problem was isolated, culminating in the replacement of the suspect single port SRAM IPs by dual port SRAM IPs, which was implemented in SAMPV V3 and V4.

The SAMPV V4 version was tested and its results were accepted by CERN in the final product readiness review done over this project by a committee elected by ALICE, authorizing its mass fabrication and usage.

Irradiation tests made over the final SAMPV V3 and V4 had not shown latch-ups, confirming the design correction and also the adequate tolerance for the detector environment. As no SEL happened, a boundary worst case cross-section was estimated as $1.7 \cdot 10^{-7} \text{ cm}^2$ an improvement of four orders of magnitude.

High resolution pulsed laser tests lately had shown that the fixes blind derived

by the actions described here for latch-up avoidance were correct and the solution was effective and performed properly, concluding the contribution to CERN ALICE.

Even with the conclusion of SAMPA V4, a last chip prototype was taped-out including proofs of concept for the proposed automated design optimizer. This was SAMPA MPW5 and carried seven versions of the SAR ADC digital block and new implementations of the BC2 filter.

The chip was irradiated in the Pelletron accelerator at IFUSP and monitored using a custom SoC based data acquisition system. The SAR block measurements had shown that it is possible to increase the device MTBF by changes in its internal state machine encoding and also by adding redundancy.

Two triplication methods have also been tested, where both had improved the device MTBF achieving more than a thousand times of increase. The per register TMR and the full modular approach had similar performance without measurable difference up to the ^{16}O fluence of $368 \cdot 10^6$ particles/cm², being both methods very successful. On the other hand, the per register TMR area consumption was 33.8% smaller.

An analysis was also made over the reset strategy, where asynchronous and synchronous solutions were compared; the test results showed that the asynchronous design was considerably more sensitive to the single events, being the synchronous strategy the preferred solution for this case as it increased the MTBF by more than 31 times.

Finally, three new digital baseline correction FIR filters have been proposed as solutions for the lockout problems and to the detected baseline jumps induced by single event upsets. Comparisons with existent works have shown that these problems can be solved at a very low cost and the filter can be fit in a state of art front-end ASIC with an impact as small as 0.07% in the area.

These filters were fabricated in 130 nm technology being packaged and tested. An irradiation campaign of about one week was performed in the Pelletron particle accelerator facility where all proposed versions showed advantages in relation to the reference filter, more than doubling its MTBF.

These tests validated the filters and also had shown the importance of automated strategies in the design loop, allowing the increase of radiation tolerance while searching for adequate trade-offs using artificial intelligence techniques.

5.1 Next steps

The present work achieved a processor that is compatible with the current needs of the target detectors but for future applications, some improvements of the digital section are suggested.

There is a growing need for higher ADC sample rates, in this way, the signal processing capacities could be increased from 20 MSps to faster rates near 100 MSps. Considering this input rate would imply in several changes in terms of compression and output bandwidth.

The support of higher serialization frequency values would be important together with an increased number of SLVS links, dedicated serializers and even phase-locked loops.

New serial stream encoding would be desirable for the output links, including 8b10b encoding, Reed–Solomon or other alternatives.

Even with improved output bandwidth, a stronger compression rate in the chip may be needed including lossy and loss-less algorithms with more dedicated resources than SAMPAs. Algorithms using external information from neighborhood pads could be beneficial, but for this, an inter-chip network needs to be implemented.

SAMPAs was already a big evolution with respect to channel density per chip, but there is still the objective to go further achieving a chip with 64 channels or even 80 channels, reducing the number of chips in the current TPC board from 5 SAMPAs to just two. This will imply in a very large chip with the current 130 nm technology, so a more modern process should be selected going to 65 nm or below.

With a 65 nm process, a higher memory density will be achievable and the internal data memory buffers could be extended surpassing 8K words per channel, which could be used for better input burst handling and improved compression.

With respect to the optimizer, new target circuits could be addressed including sections with tighter and high-demanding constraints like high-speed blocks as the serializers and blocks with internal IPs, as the neighbor input block or the ring buffers. Other algorithms for non-linear problems could also be explored and an extensive artificial intelligence research field could be derived from this base problem and proposal.

The proposed SEL avoidance technique could also be tested and validated in other IPs, design kits and technological processes providing important support for other projects.

Finally, if other tape-outs are available, several of the cited actions could be implemented, fabricated and even irradiated in test beams, enriching the knowledge on the topic with real measurements and proofs of concept.

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APPENDIX A – SAMPA V4 Datasheet

SAMPA V4 Data Sheet

Revision 11/11/2020

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A.1. Overview

A.1.1. Documentation Overview

This document is part of a set of documents that describes the SAMPA_V4 IC, a new prototype ASIC for the front-end readout specially designed for the Time Protection Chamber (TPC). The SAMPA_V4 is a modified version of SAMPA_V3, with an increased input rate of front-end and improved pile-up performance for TPC.

Technical SAMPA_V4 IC information is distributed over two documents: (I) SAMPA_V4 Data Sheet and (II) specific block guides for each block, that will be referred along this document. Each is a self-contained document, but thorough understanding of the IC and its applications requires studying all documents.

All released SAMPA_V4 documents are posted on the TWIKI website (<https://twiki.cern.ch/twiki/bin/viewauth/ALICE/SAMPA>) and are available for download. The SAMPA ASIC Document List could be found at:

<https://docs.google.com/spreadsheets/d/16SnfEWtvyZYONnxmMhVzUo-St-ZtPRVV3Z6mfy13dRU/edit?usp=sharing>

A.1.2. Device Description

The SAMPA_V4 prototype is a front-end ASIC implemented in a commercial 130nm CMOS process from TSMC, with 1.2V nominal voltage supply. It integrates 32 channels per chip that concurrently digitize and process the input signals. SAMPA_V4 contains negative and positive polarity front-end, which transform the charge signal into a differential semi-Gaussian voltage signal, that is digitized by a 10-bit 10 M Samples/s full differential ADC. After the ADC a digital signal processor eliminates signal perturbations, distortion of the pulse shape, offset and signal variation due to temperature variations. The data read-out takes place continuously at a speed of up to 1.28 Gbps by eleven 320 Mb/s e-links.

The functional block diagram for the SAMPA_V4 IC is shown in Figure 1.

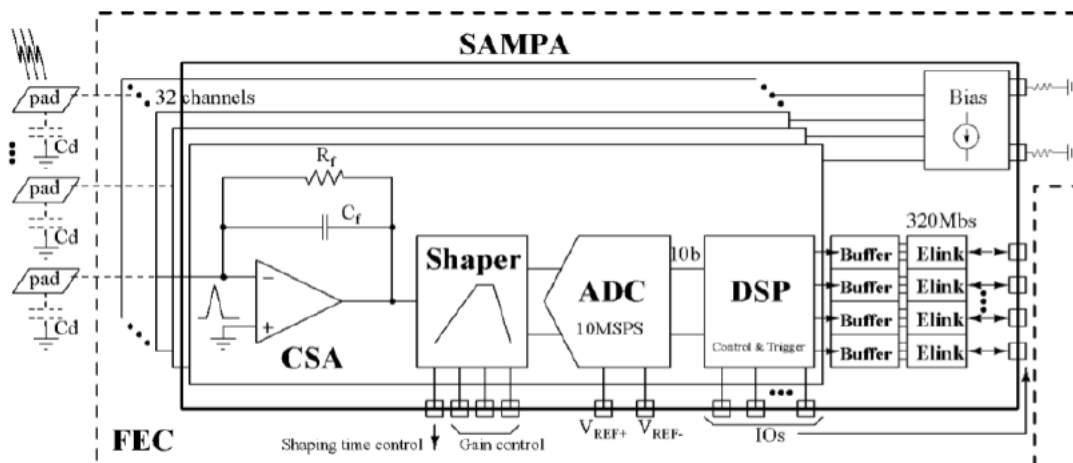


Figure 1: Block diagram for the SAMPA chip.

A.1.2.1. Analog front-end

The front-end block is composed of negative and positive polarity Charge Sensitive Amplifier (CSA) with a capacitive feedback C_f and a resistive feedback R_f connected in parallel, a Pole-Zero Cancellation (PZC) network, a high pass filter, two bridged-T second order low pass filters, a non-inverting stage, as shown in Figure 2.

The first shaper is a scaled-down version of the CSA and generates the two first poles and one zero. A copy of the first shaper connected in unity gain configuration is implemented in order to provide a differential mode input to the next stage.

The second stage of the shaper is a fully differential second order bridged-T filter and it includes a Common-Mode Feed-Back network (CMFB). The non-inverting stage adapts the DC voltage level of the shaper output to use the full dynamic range of the ADC. It consists of a parallel connection of two equally designed Miller compensated amplifier.

The SAMPA front-end V4 circuit is a modified version of SAMPA_V3, with an increased input rate of front-end and improved pile-up performance for TPC. In order to improve the input charge rate the feedback resistance (RF) of the CSA was reduced by reducing the size ratio of the current mirror transistors (K). When K is reduced the number of the VGS voltage of the feedback transistor is increased and as a consequence the drain-to-source resistance of the feedback resistance is reduced.

With this modification, SAMPA_V4 supports more equivalent input charge and does not saturates in the pile-up scenarios specified by the TPC.

The performance comparison between SAMPA_V3 and SAMPA_V4 is summarized in the Performance Section. More detail on the analog front end can be find in the following documents: [Block Guide Readout Front-end](#) and [SAMPA V4 CSA Pile-up Improvement](#).

The analog front-end can be configured to operate at two shaping time settings controlled by the CTS pin, three sensitivity settings controlled by the CG[1:0] pins and positive/negative input charge polarity controlled by the POL pin. Table 1 summarizes the possible configurations.

Table 1: Analog Front-end Configurations

Polarity	POL	Gain	Shaping time	CTS	CG0	CG1
Positive	low	30mV/fC	160 ns	low	high	high
Negative	high	20mV/fC	160ns	low	low	high
		4mV/fC	300 ns	high	low	low

(a) Pulse polarity configuration

(b) Gain and shaping time configuration

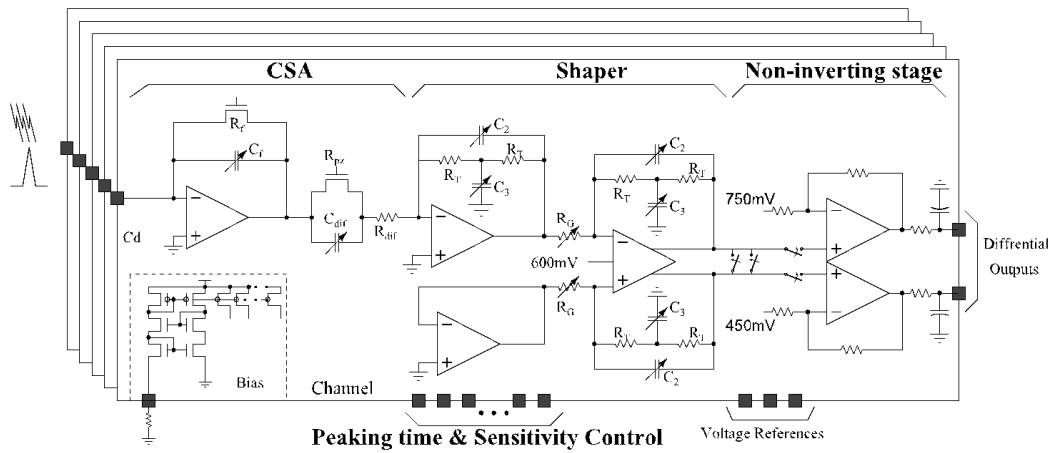


Figure 2: Block diagram of the analog front-end.

A.1.2.2. Analog to digital converter

ADC used in SAMPA V4 is the same than used in SAMPA V3. The ADC is based on a split capacitor fully differential successive approximation (SAR) topology. The SAR topology allows for low power with reasonable sample rates and resolution. The ADC has a resolution of 10-bit and a sample rate up to 20 MSamples/s. The block diagram of the ADC is shown in Figure 3. The main parts of the circuit are: capacitive array, switches, comparator and the SAR control logic. The capacitor array is used to perform sample & hold and the digital to analog converter functions. Figure 4 shows the time diagram for the ADC².

The ADC circuit was slightly modified when compared to SAMPA_V2 (unitary capacitor array from 26fF to 45fF) and the path between Analog Front-End output and ADC input was improved. With this modification, the ADC has an expected nominal ENOB of 9.0bits, as shown in Figure 5.

Considering a 50 ohms ADC input resistance (wave generator output impedance), simulated and measured spectrums are practically identical for 90% range.

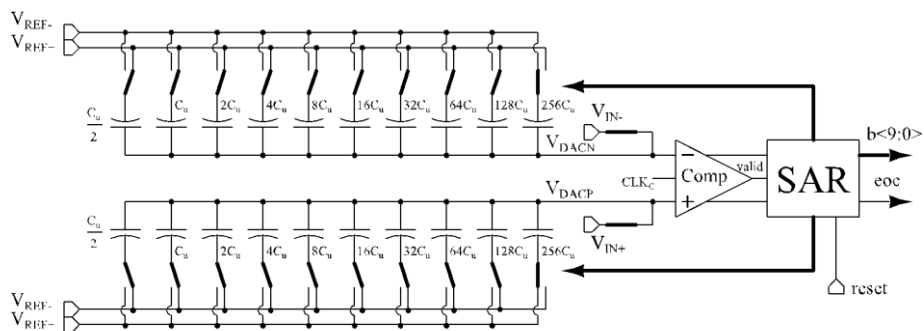


Figure 3: Block diagram of the ADC.

² [ADC Block Guide](#)

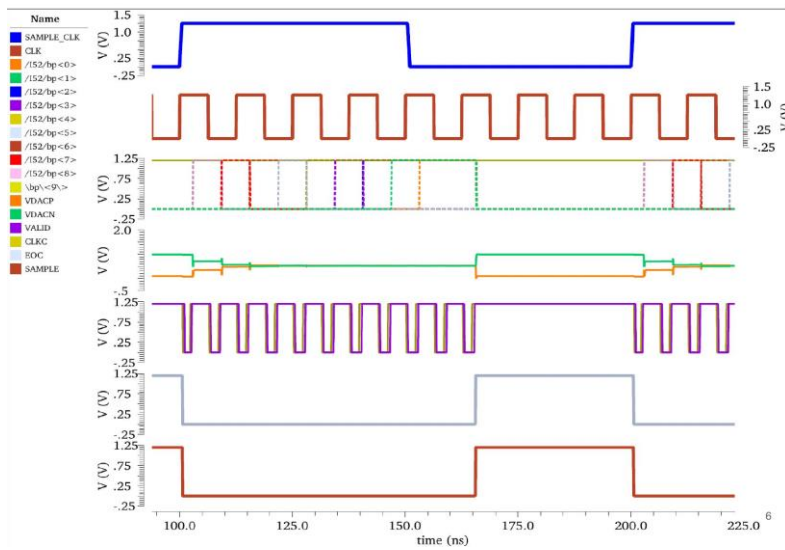


Figure 4. ADC Time diagram.

Table 2: ADC V3 Corners dynamic simulation results.

SAMPA V3 ADC	ENOB [bits]	SINAD [dB]	SFDR [dB]
NOM	9.25	56.8	-59.0
SLOW	9.34	57.3	-60.0
FAST	9.09	55.9	-57.7
FSFS	9.23	56.6	-58.8
FSSF	9.09	55.9	-57.6
SFFS	9.33	57.3	-59.8
SFSF	9.22	56.7	-58.8

<https://docs.google.com/spreadsheets/d/10cpaeWiAVzwEMBH6OfhxNREImmlAWuLrPyY5ByAUxck/edit?usp=sharing>

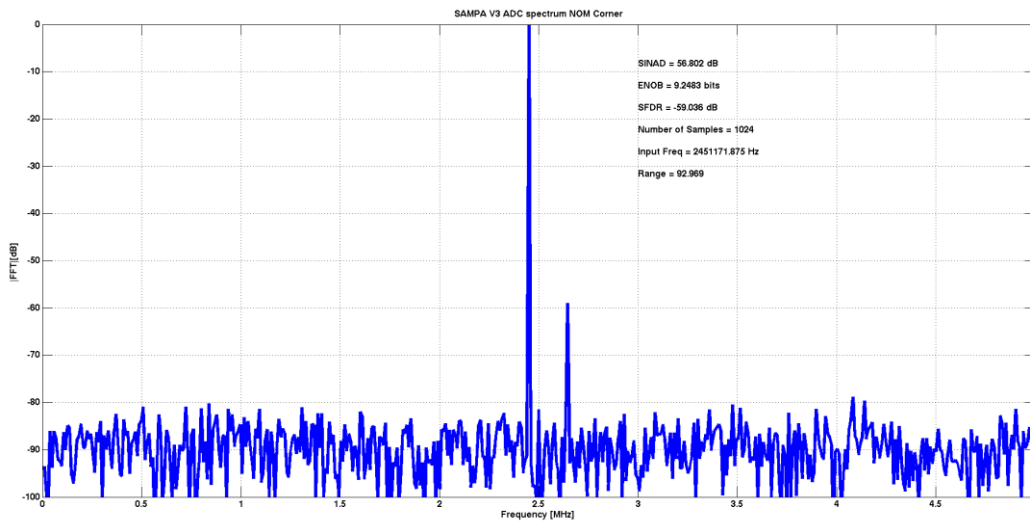


Figure 5. ADC simulation full extracted @ 10MSPS, 1024 samples, Input frequency of 2,451,171.875 Hz, 90% Input range, typical corner at 40 degrees Celsius - ENOB 9.25 bits.

The ADC shows a low code spreading and no missing codes, as can be seen in Figure 6. Figure 7 shows the DNL obtained from the ADC full extracted view simulation, considering all parasitics and dumping resistor. DNL is below 0.2 LSB, which is a result of no missing codes events and low spread between even and odd codes quantity. The INL, showed no Figure 8, is below 1 LSB and remains a third order distortion.

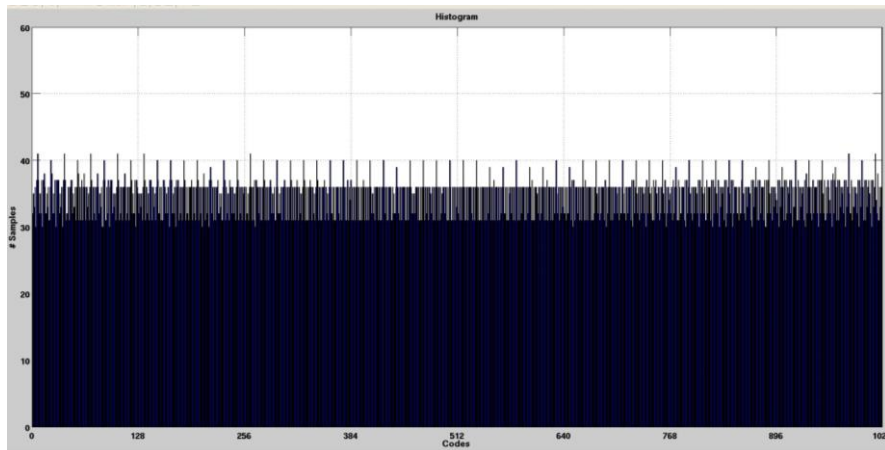


Figure 6. ADC full extracted simulation histogram, considering parasitic routing and dumping resistors.

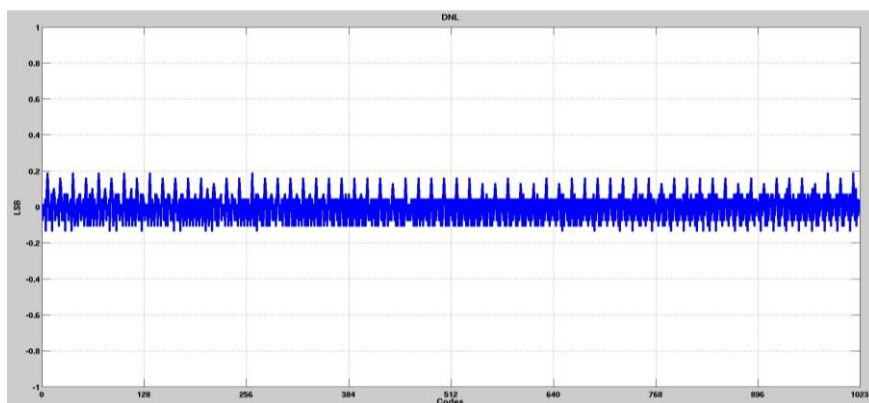


Figure 7. ADC full extracted simulation DNL, considering parasitic routing and dumping resistors. DNL < 0.2 LSB.

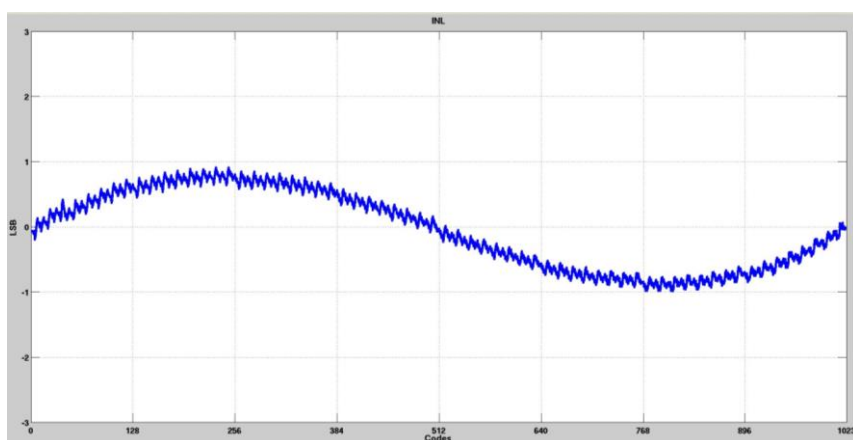


Figure 8. ADC full extracted simulation INL, considering parasitic routing and dumping resistors. INL < 1 LSB.

A.1.2.3. Digital Signal Processing

The Digital Signal Processing (DSP) part is composed by digital filters, a data format unit, a ring buffer, a trigger manager block, a configuration register bank, a control state machine, and eleven 320 Mb/s e-links³.

The data read-out takes place continuously at a speed of up to 1.28 Gbps by eleven 320 Mb/s serializations links (e-links). The data read-out can be performed in continuous mode or in triggered mode. In continuous mode the read-out of a programmable number of samples is performed trigger-less if the input signal exceeds the programmable threshold value. For the TPC application the DSP capabilities are not used but DAS mode is assumed. For the MCH the design event rate is 100 kHz and 1 % occupancy with probability of 90 % and 9 % with probability of 10 %. Software triggers are accepted in continuous mode for calibration and synchronization purposes.

In triggered mode, the data read-out of programmable number of samples is performed only upon reception of an external trigger with a maximum latency $< 9.6\mu\text{s}$. Triggers arriving during an active readout will be accepted. In that case the active readout will be extended by the new arriving trigger for the programmable number of samples and status information is sent to acknowledge the read-out extension. Optionally a programmable number of pre/post samples before/after the input signal crossed the threshold in continuous mode or the external trigger mode arrived can be read-out.

Digital signal conditioning

The objective of the Digital Signal Condition (DSC) is to increase the efficiency of the data compression algorithms (e. g. zero suppression). The DSC implements, in several subsequent stages (pipeline), different algorithms to condition and shape the signal. The DSC is comprised of four main building blocks

Baseline Correction I (BCI)

It is the first stage of the data processor. Its main task is to remove the low frequency perturbations and systematic effects. This filter has different modes of operation depending on the application.

Digital Shaper (DS)

It can be use for two different applications; tail cancellation or peaking time correction. A fourth order IIR filter is implemented. The choice of the filter parameters configure the system for one of the applications:

- Tail cancellation: an accurate cancellation of the signal tail is required in order to perform the zero suppression efficiently. Since the filter coefficients for each channel are fully programmable and reconfigurable, the circuit is able to cancel a wide range of signal tail shapes.
- Peaking time correction: modification of the peaking time according to the application

³ [Block Guide for the digital part.](#)

Baseline Correction II (BCII)

This unit applies a baseline correction based on a moving average filter. This scheme removes non-systematic perturbations of the baseline that are superimposed to the signal. At the output of this block, the signal baseline is constant with an accuracy of 1 Least Significant Bit (LSB).

Baseline Correction III (BCIII)

This unit applies a baseline correction through a slope based filter. It is provided as an alternative to the BCII filter as the BCII filter can potentially get stuck outside its thresholds in cases of very large perturbations.

The digital word length can be changed only in steps of 1 bit, the addition of 1 bit to the data-path reduces the size of quantification error analysis by factor of 2. Table 3 shows the calculated signal to noise ratio of the system. Following a commitment between accuracy system and hardware complexity, it is added two extra bits (LBS) in the data path.

In Sampa_V4 all memories used are Dual Port Memory (SAMPA_V2 used Single Port Memory). Dual Port Memories allow to read and write different cells simultaneously and seem to be more robust regarded to Single-Event-Latchup. For instance, the pre-trigger samples delay module uses a 10 x 192 bit dual port memory to provide a programmable delay chain for the samples to compensate for any delay in the trigger signal.

Table 3: Signal to noise ratio of the filter

Resolution	NR
ADC (10 bits)	66.22 dB
ADC (10 bits) + Shaper (10bits)	53.99 dB
ADC (10 bits) + Shaper (11bits)	59.30 dB
ADC (10 bits) + Shaper (12bits)	63.25 dB
ADC (10 bits) + Shaper (13bits)	65.27dB

A.1.3. Configurable Reference Voltage Source

The Configurable Reference Voltage Source provides 3 output voltage tap values: 750mV, 600mV and 450 mV, which works with 3% variation on a temperature range between -20°C and 70°C and a power supply range 1.05V and 1.35V.

The circuit topology is based the one proposed by Banba and others [Huang et al.,2006], as shown in the Figure 9 below. Additional resistors are used in the M3 current branch to provide two additional voltages. To allow for trimming, the resistor connected to ground is adjustable with 3 NMOS transistors.

The main reference voltages are named according to its nominal expected values respectively 450 mV, 600 mV, 750 mV, for the signals V450, V600 and V750. The Monte Carlo simulation results are described in table 4.

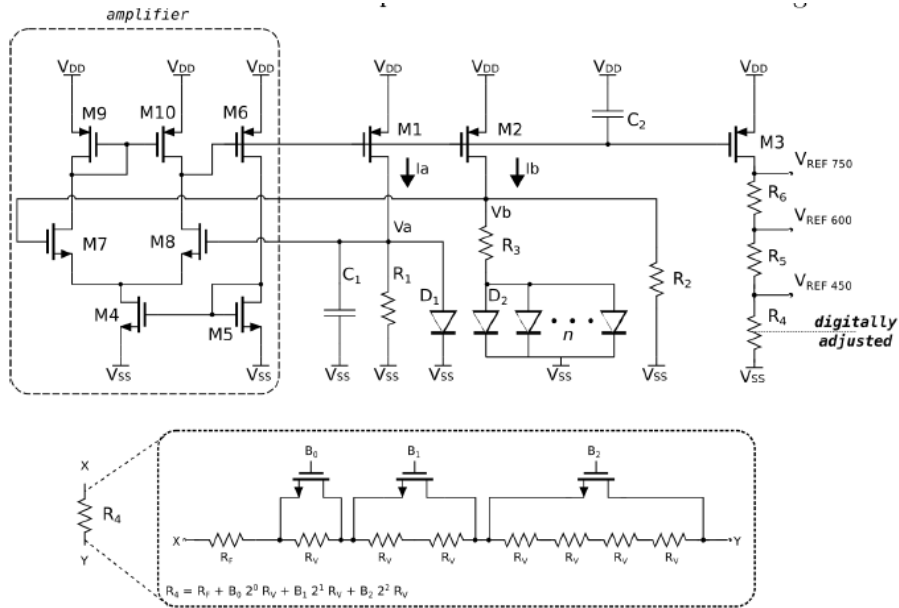


Figure 9. Voltage Reference schematic.

Table 4: Monte Carlo Simulation Result.

Characteristics	Min	Max	Mean	Sigma	Unit
Line Regulation	245.8u	465.5u	346u	35.35u	V/V
PSSR	180.8	183.3	182.1	390.3m	dB
TC	7.364	21.86	13.37	2.721	ppm
Vref_750mV	741.1m	764.2m	752.2m	3.923m	V
Vref_600mV	592.9m	611.6m	601.8m	3.142m	V
Vref_450mV	449m	458.9m	451.5m	2.363m	V

The reference voltage source is configured using three I2C configurable bits available in the global register unit. The expected levels for each possible configuration are shown in the table 5. It is important to note that these values are subject to process variations, as described in the [Bandgap Reference Source Design](#).

Table 5: Simulated results for the Bandgap output voltage, for 1.25V of VDD and 40°C temperature.

Setting	Bit 2	Bit 1	Bit 0	v600 [mV]	v750 [mV]	v450 [mV]
0	0	0	0	698.4	847.7	549.1
1	0	0	1	674.0	823.4	524.6
2	0	1	0	649.1	798.6	499.6
3	0	1	1	624.5	774.1	474.9
4	1	0	0	599.3	749.0	449.6
5	1	0	1	574.5	724.3	424.7
6	1	1	0	549.5	699.3	399.6
7	1	1	1	524.7	674.6	374.7

A.1.4. Performance Specification

In the tables 6, 7 and 8 below, it is summarized the post layout simulations for the 3 gain configurations of the SAMPA_V4: 4P300 (4mV/fC gain, 300ns peaking time and positive input polarity), 20N160 (20mV/fC gain, 160ns peaking time and negative input polarity) and 30N160 (30 mV/fC gain, 160ns peaking time and negative input polarity).

The simulation was performed for the extracted view considering an input charge of 50fC ($Q_{in}=50fC$), a Detector capacitance of 18.5pF ($C_d =18.5pF$) and a corner variation from 0 to 80 degrees Celsius.

Table 6: Post layout simulations for SAMPA V4 circuit, considering 4mV/fC configuration and the worst case for process and temperature variation.

	4P300 (SAMPA V4)		
	Min	Typ (40C)	Max
IREF<1:32> (bias 01)	192.9uA (SLOW_0C)	262.6 uA	362uA (FAST_80C)
VBC (bias 01)	662mV (FSSF_80C)	777.6mV	898.6mV (SFFS_0C)
Sensitivity	3.29mV/fC (SFFS_0C)	3.81mV/fC	4.28mV/fC (FSSF_80C)
Peaking Time	222.6ns (FAST_80C)	305.1ns	405.8ns (SLOW_0C)
IREFS<1:32> (bias 02)	34.19uA (SLOW_0C)	58.41uA	109.5uA (SFFS_80C)
ENC * @ Cd=40pF	959 e- (FAST_0C)	1053 e-	1144 e- (SLOW_80C)

*Those ENC values only consider Analog Front-End noise and not ADC quantization noise.

Table 7: Post layout simulations for SAMPA_V4 circuit, considering 20mV/fC configuration and the worst case for process and temperature variation.

	20N160 (SAMPA V4)		
	Min	Typ (40C)	Max
IREF<1:32> (bias 01)	192.9uA (SLOW_0)	262.6uA	362uA (FAST_80C)
VBC (bias 01)	662mV (FSSF_80C)	777.6mV	898.6mV (SFFS_0C)
Sensitivity	16.35mV/fC (SFFS_80C)	19.01mV/fC	21.17mV/fC FSSF_80C)
Peaking Time	118.4ns (FAST_80C)	165.3ns	223.6ns (SLOW_0C)
IREFS<1:32> (bias 02)	34.19uA (SLOW_0C)	58.41uA	109.5uA (SFFS_80C)
ENC * @ Cd=25pF	513 e- (SFFS_0C)	572 e-	626 e- (FSSF_80C)

*Those ENC values only consider Analog Front-End noise and not ADC quantization noise.

SAMPA_V4 has an increased input rate and an improved pileup performance, when compared to SAMPA_V2, as shown in table 9. The Pile Up simulations were performed by applying at input of the Charge Amplifier (CSA) a series of charges (voltage step over a 1pF injection capacitor) simulating a stream of charge injections using slow corner to find the saturation point.

As conclusion of those simulations, for 5fC continuous charge stream with a 90fC peak after 256 pulses, 400ns of pulse spacing caused agglutination of semi-gaussian pulses but no saturation was observed in SAMPA_V4. Considering a 10fC continuous charge stream with a 90fC peak after 256 pulses, no saturation was observed but the results show a small gain variation due to baseline variations, especially after the 90fC charge peak.

For 100 charge injections with 50fC peak it was observed saturation in 2 stages: (a) strong saturation in 45nA and 50nA which implies a continuous degradation of sensitivity and (b) weak saturation in 40nA with small sensitivity degradation at the beginning until a steady state is reached, after that the sensitivity is stable.

Table 8: Post layout simulations for SAMPA V4 circuit, considering 30mV/fC configuration and the worst case for process and temperature variation.

	30N160 (SAMPA V4)		
	Min	Typ (40C)	Max
IREF<1:32> (bias 01)	192.9uA (SLOW_0C)	262.6uA	362uA (FAST_80C)
VBC (bias 01)	662mV (FSSF_80C)	777.6mV	898.6mV (SFFS_0C)
Sensitivity	24.43mV/fC (SFFS_80C)	28.46mV/fC	31.57mV/fC (FSSF_40C)
Peaking Time	119.1ns (FAST_80C)	166ns	226.2ns (SLOW_0C)
IREFS<1:32> (bias 02)	34.19uA (SLOW_0C)	58.41uA	109.5uA (SFFS_80C)
ENC * @ Cd=25pF	501 e- (SFFS_0C)	560 e-	620 e- (FSSF_80C)

*Those ENC values only consider Analog Front-End noise and not ADC quantization noise.

The simulations were performed for typical extraction at Nominal Corner and 40 degrees Celsius and the complete Pile Up results are documented in [Pile Up Summary Report](#).

Table 9: Comparison of SAMPA_V3 and SAMPA_V4 performance, considering typical corner (40°C) and 50fC input charge.

20N160			
	Typ V3	Typ V4	Change
Sensitivity	18.4mV/fC	19.01mV/fC	+3.3%
Peaking Time	162ns	165.3ns	+2.03%
ENC @ Cd=25pF	548e-	572e-	+4.4%
30N160			

	Typ V3	Typ V4	Change
Sensitivity	27.1mV/fC	28.46mV/fC	+5,01%
Peaking Time	165ns	166ns	+0.6%
ENC @Cd=25pF	536e-	560e-	+4.5%
4P300			
	Typ V3	Typ V4	Change
Sensitivity	3.78mV/fC	3.81mV/fC	+0,79%
Peaking Time	302ns	305.1ns	+1,02%
ENC @Cd=40pF	1023e-	1053e-	+3%

As shown in the table 10 below, ADC simulation shows an ENOB of 9.0 considering a typical corner at 40 degrees Celsius.

Table 10: ADC Performance Summary.

Parameters	V3 Simulation		
	Spec	WC	Condition
ENOB [bits]	> 9.2	9.06	FSSSF, 40°C
SNDR [dB]	< 57.76	55.7	FSSSF, 40°C
SFDR [dB]	> 60	57.9	FSSSF, 40°C
INL [LSB]	< 0.7	-0.86	FSF,40°C
DNL [LSB]	< 0.7	-0.18	FSF,40°C

A.2. Pad Definitions

A.2.1. Die physical dimensions

SAMPA_V4 is a 9.534 mm x 8.944 mm ASIC with 32 input channels implemented in a commercial 130 nm CMOS process. The full layout is displayed in Figure 10. Its main physical characteristics are described below.

Die size:	9534 μ m x 8944 μ m
Dice uncertainty	40 μ m per side
Die thickness:	300 μ m
Input bonding pads:	One column
Pad size:	50 μ m x 66 μ m
Pad pitch:	100 μ m

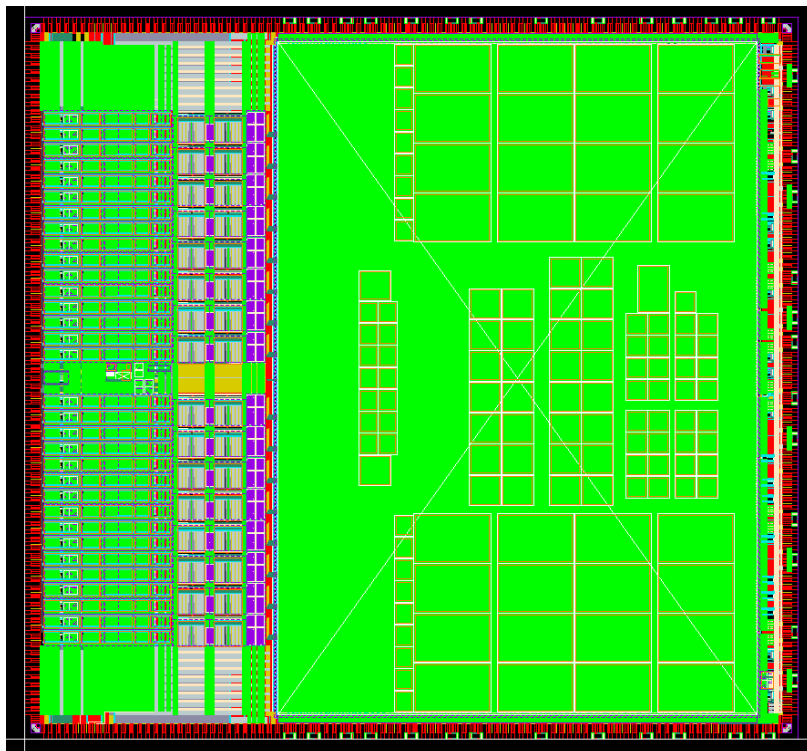


Figure 10: SAMPA V4 full layout.

The full chip is composed by several analog and digital blocks. Their position in the full chip is shown in Figure 11 and the size of each block is shown in Table 11.

The input pads are located in the left side. The output pads are in the left side. The top and bottom pads corresponds to the bias and power pads. The chip input, output and power pads are shown in Figure 12.

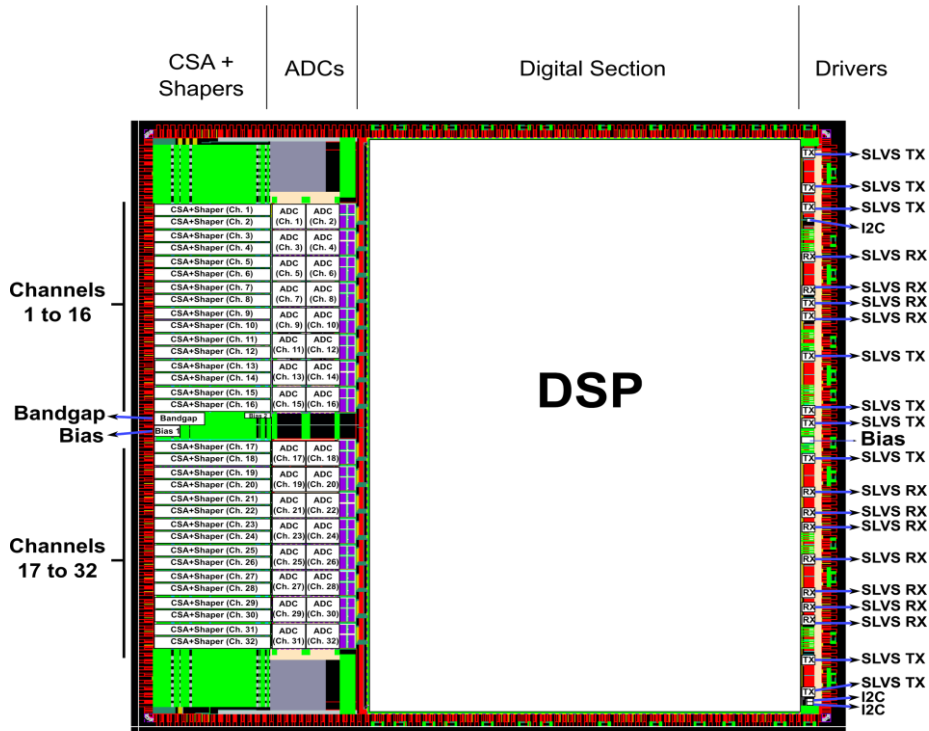


Figure 11: Full-chip with highlighted blocks

Table 11: Area of the full chip and of each block

Full Area:	9534 μm x 8944 μm
FE Channel area:	1559 μm x 193 μm
ADC area:	451 μm x 323 μm
DSP area:	5897 μm x 8536 μm
SLVS Tx area:	154 μm x 112 μm
SLVS Rx area:	142 μm x 82 μm
I2C area:	72 μm x 41 μm
Bandgap area:	305 μm x 222 μm
Bias01 area:	294 μm x 168 μm
Bias02 area:	270 μm x 71 μm
BiasTx area:	270 μm x 71 μm
POR area:	159 μm x 229 μm

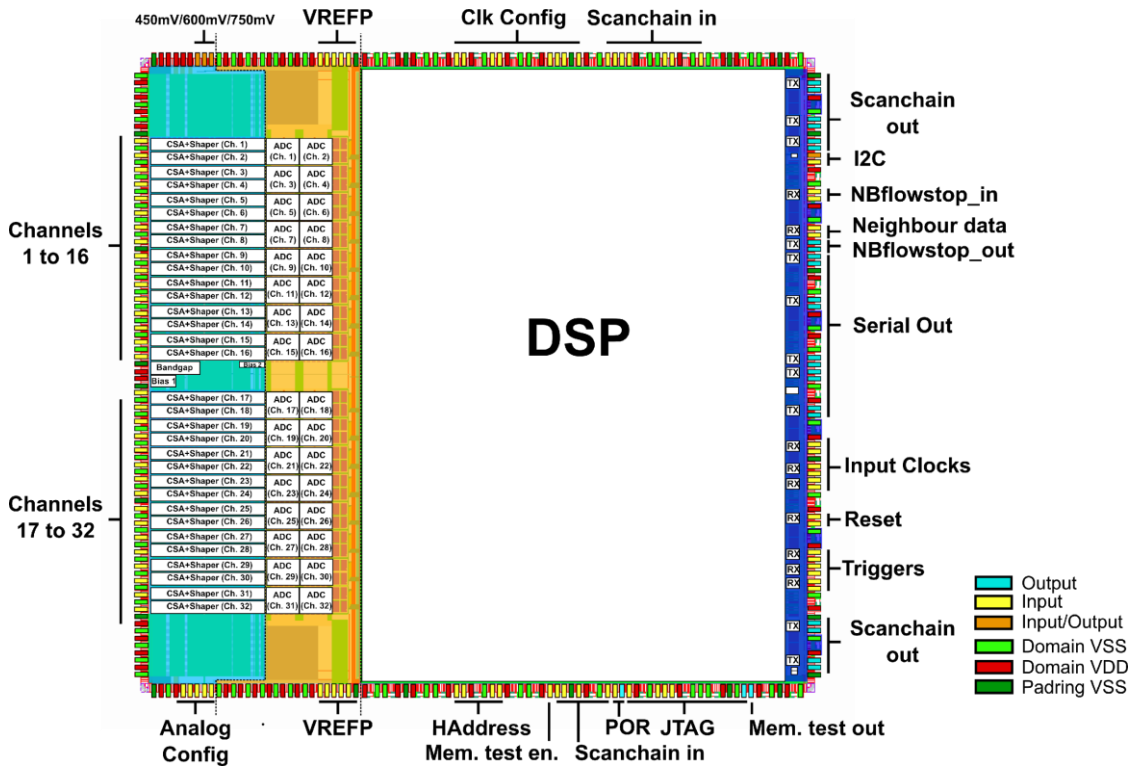


Figure 12: Inputs and outputs of the SAMPA V4 chip.

A.2.2. Pad assignments

The SAMPA_V2 IC has 350 pads that are shown in Figure 13.

Pin assignments are defined in Table 12, Table 13, Table 14, Table 15 in this chapter.

When used as a die, the center slug must be soldered directly to the PCB analog ground plane.

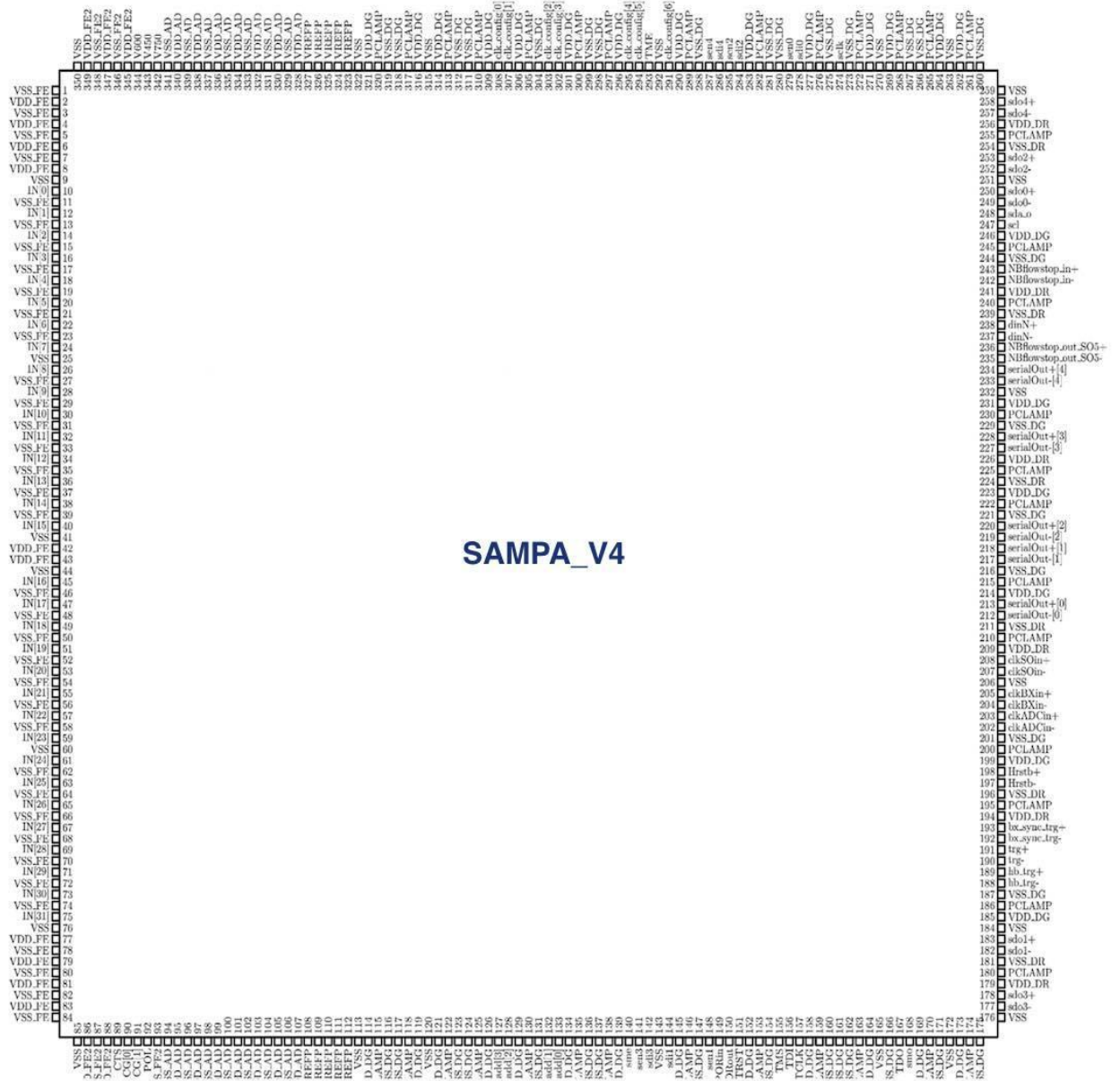


Figure 13: SAMPA V4 pad names.

A.2.3. Pad Description

Type definitions:

AI = Analog Input

AO = Analog output

DI = Digital input

DNC = Do not connect

DO = Digital output

P = Power or ground

Table 12: Pad description part1.

Pad #	Pad Name	IO type	Pad Description	Pad #	Pad Name	IO type	Pad Description
1	VSS_FE	P	Analog ground FS and CSA	43	VDD_FE	P	Analog core voltage FS and CSA
2	VDD_FE	P	Analog core voltage FS and CSA	44	VSS	P	PADRING ground
3	VSS_FE	P	Analog ground FS and CSA	45	IN[16]	AI	Analog channel 16
4	VDD_FE	P	Analog core voltage FS and CSA	46	VSS_FE	P	Analog ground FS and CSA
5	VSS_FE	P	Analog ground FS and CSA	47	IN[17]	AI	Analog channel 17
6	VDD_FE	P	Analog core voltage FS and CSA	48	VSS_FE	P	Analog ground FS and CSA
7	VSS_FE	P	Analog ground FS and CSA	49	IN[18]	AI	Analog channel 18
8	VDD_FE	P	Analog core voltage FS and CSA	50	VSS_FE	P	Analog ground FS and CSA
9	VSS	P	PADRING ground	51	IN[19]	AI	Analog channel 19
10	IN[0]	AI	Analog channel 0	52	VSS_FE	P	Analog ground FS and CSA
11	VSS_FE	P	Analog ground FS and CSA	53	IN[20]	AI	Analog channel 20
12	IN[1]	AI	Analog channel 1	54	VSS_FE	P	Analog ground FS and CSA
13	VSS_FE	P	Analog ground FS and CSA	55	IN[21]	AI	Analog channel 21
14	IN[2]	AI	Analog channel 2	56	VSS_FE	P	Analog ground FS and CSA
15	VSS_FE	P	Analog ground FS and CSA	57	IN[22]	AI	Analog channel 22
16	IN[3]	AI	Analog channel 3	58	VSS_FE	P	Analog ground FS and CSA
17	VSS_FE	P	Analog ground FS and CSA	59	IN[23]	AI	Analog channel 23
18	IN[4]	AI	Analog channel 4	60	VSS	P	PADRING ground
19	VSS_FE	P	Analog ground FS and CSA	61	IN[24]	AI	Analog channel 24
20	IN[5]	AI	Analog channel 5	62	VSS_FE	P	Analog ground FS and CSA
21	VSS_FE	P	Analog ground FS and CSA	63	IN[25]	AI	Analog channel 25
22	IN[6]	AI	Analog channel 6	64	VSS_FE	P	Analog ground FS and CSA
23	VSS_FE	P	Analog ground FS and CSA	65	IN[26]	AI	Analog channel 26
24	IN[7]	AI	Analog channel 7	66	VSS_FE	P	Analog ground FS and CSA
25	VSS	P	PADRING ground	67	IN[27]	AI	Analog channel 27
26	IN[8]	AI	Analog channel 8	68	VSS_FE	P	Analog ground FS and CSA
27	VSS_FE	P	Analog ground FS and CSA	69	IN[28]	AI	Analog channel 28
28	IN[9]	AI	Analog channel 9	70	VSS_FE	P	Analog ground FS and CSA
29	VSS_FE	P	Analog ground FS and CSA	71	IN[29]	AI	Analog channel 29
30	IN[10]	AI	Analog channel 10	72	VSS_FE	P	Analog ground FS and CSA
31	VSS_FE	P	Analog ground FS and CSA	73	IN[30]	AI	Analog channel 30
32	IN[11]	AI	Analog channel 11	74	VSS_FE	P	Analog ground FS and CSA
33	VSS_FE	P	Analog ground FS and CSA	75	IN[31]	AI	Analog channel 31
34	IN[12]	AI	Analog channel 12	76	VSS	P	PADRING ground
35	VSS_FE	P	Analog ground FS and CSA	77	VDD_FE	P	Analog core voltage FS and CSA
36	IN[13]	AI	Analog channel 13	78	VSS_FE	P	Analog ground FS and CSA
37	VSS_FE	P	Analog ground FS and CSA	79	VDD_FE	P	Analog core voltage FS and CSA
38	IN[14]	AI	Analog channel 14	80	VSS_FE	P	Analog ground FS and CSA
39	VSS_FE	P	Analog ground FS and CSA	81	VDD_FE	P	Analog core voltage FS and CSA
40	IN[15]	AI	Analog channel 15	82	VSS_FE	P	Analog ground FS and CSA
41	VSS	P	PADRING ground	83	VDD_FE	P	Analog core voltage FS and CSA
42	VDD_FE	P	Analog core voltage FS and CSA	84	VSS_FE	P	Analog ground FS and CSA

Table 13: Pad description part 2.

Pad #	Pad Name	IO type	Pad Description	Pad #	Pad Name	IO type	Pad Description
85	VSS	P	PADRING ground	131	VSS_DG	P	Digital ground
86	VDD_FE2	P	Analog core voltage SS and output buffer	132	hadd[1]	DI	Chip address (Static)
87	VSS_FE2	P	Analog ground SS and output buffer	133	hadd[0]	DI	Chip address (Static)
88	VDD_FE2	P	Analog core voltage SS and output buffer	134	VDD_DG	P	Digital core voltage
89	CTS	AI	Shaping configuration (Static)	135	PCLAMP	DNC	POWER CUT RESERVED SPACE
90	CG0	AI	Gain configuration (Static)	136	VSS_DG	P	Digital ground
91	CG1	AI	Gain configuration (Static)	137	VSS_DG	P	Digital ground
92	POL	AI	Polarity configuration (Static)	138	PCLAMP	DNC	POWER CUT RESERVED SPACE
93	VSS_FE2	P	Analog ground SS and output buffer	139	VDD_DG	P	Digital core voltage
94	VSS_AD	P	ADC supply ground	140	sme	DI	MEM Test En (CMOS)
95	VDD_AD	P	ADC supply voltage	141	sen3	DI	Scanchain test Scan Enable (CMOS)
96	VSS_AD	P	ADC supply ground	142	sd13	DI	Scanchain test Scan In (CMOS)
97	VDD_AD	P	ADC supply voltage	143	VSS	P	PADRING ground
98	VSS_AD	P	ADC supply ground	144	sd11	DI	Scanchain test Scan In (CMOS)
99	VDD_AD	P	ADC supply voltage	145	VDD_DG	P	Digital core voltage
100	VSS_AD	P	ADC supply ground	146	PCLAMP	DNC	POWER CUT RESERVED SPACE
101	VDD_AD	P	ADC supply voltage	147	VSS_DG	P	Digital ground
102	VSS_AD	P	ADC supply ground	148	sen1	DI	Scanchain test Scan Enable (CMOS)
103	VDD_AD	P	ADC supply voltage	149	PORin	DI	Power on reset input (CMOS)
104	VSS_AD	P	ADC supply ground	150	PORout	DO	Power on reset output (CMOS)
105	VDD_AD	P	ADC supply voltage	151	TRST	DI	JTAG (CMOS)
106	VSS_AD	P	ADC supply ground	152	VDD_DG	P	Digital core voltage
107	VDD_AD	P	ADC supply voltage	153	PCLAMP	DNC	POWER CUT RESERVED SPACE
108	VREFP	P	Voltage reference p	154	VSS_DG	P	Digital ground
109	VREFP	P	Voltage reference p	155	TMS	DI	JTAG (CMOS)
110	VREFP	P	Voltage reference p	156	TDI	DI	JTAG (CMOS)
111	VREFP	P	Voltage reference p	157	TCLK	DI	JTAG (CMOS)
112	VREFP	P	Voltage reference p	158	VDD_DG	P	Digital core voltage
113	VSS	P	PADRING ground	159	PCLAMP	DNC	POWER CUT RESERVED SPACE
114	VDD_DG	P	Digital core voltage	160	VSS_DG	P	Digital ground
115	PCLAMP	DNC	POWER CUT RESERVED SPACE	161	VSS_DG	P	Digital ground
116	VSS_DG	P	Digital ground	162	VSS_DG	P	Digital ground
117	VSS_DG	P	Digital ground	163	PCLAMP	DNC	POWER CUT RESERVED SPACE
118	PCLAMP	DNC	POWER CUT RESERVED SPACE	164	VDD_DG	P	Digital core voltage
119	VDD_DG	P	Digital core voltage	165	VSS	P	PADRING ground
120	VSS	P	PADRING ground	166	VSS_DG	P	Digital ground
121	VDD_DG	P	Digital core voltage	167	TDO	DO	JTAG (CMOS)
122	PCLAMP	DNC	POWER CUT RESERVED SPACE	169	VDD_DG	P	Digital core voltage
123	VSS_DG	P	Digital ground	170	PCLAMP	DNC	POWER CUT RESERVED SPACE
124	VSS_DG	P	Digital ground	171	VSS_DG	P	Digital ground
125	PCLAMP	DNC	POWER CUT RESERVED SPACE	172	VSS	P	PADRING ground
126	VDD_DG	P	Digital core voltage	173	VDD_DG	P	Digital core voltage
127	hadd[3]	DI	Chip address (Static)	174	PCLAMP	DNC	POWER CUT RESERVED SPACE
128	hadd[2]	DI	Chip address (Static)	175	VSS_DG	P	Digital ground
129	VDD_DG	P	Digital core voltage				
130	PCLAMP	DNC	POWER CUT RESERVED SPACE				

Table 14: Pad description part 3

Pad #	Pad Name	IO type	Pad Description	Pad #	Pad Name	IO type	Pad Description
176	VSS	P	PADRING ground	218	serialOut+[1]	DO	Serial data link 1 p (SLVS)
177	sdo3-	DO	Scanchain test Scan Out (SLVS)	219	serialOut-[2]	DO	Serial data link 2 n (SLVS)
178	sdo3+	DO	Scanchain test Scan Out (SLVS)	220	serialOut+[2]	DO	Serial data link 2 p (SLVS)
179	VDD_DR	P	Digital SLVS drivers voltage	221	VSS_DG	P	Digital ground
180	PCLAMP	DNC	POWER CUT RESERVED SPACE	222	PCLAMP	DNC	POWER CUT RESERVED SPACE
181	VSS_DR	P	Digital SLVS drivers ground	223	VDD_DG	P	Digital core voltage
182	sdo1-	DO	Scanchain test Scan Out (SLVS)	224	VSS_DR	P	Digital SLVS drivers ground
183	sdo1+	DO	Scanchain test Scan Out (SLVS)	225	PCLAMP	DNC	POWER CUT RESERVED SPACE
184	VSS	P	PADRING ground	226	VDD_DR	P	Digital SLVS drivers voltage
185	VDD_DG	P	Digital core voltage	227	serialOut-[3]	DO	Serial data link 3 n (SLVS)
186	PCLAMP	DNC	POWER CUT RESERVED SPACE	228	serialOut+[3]	DO	Serial data link 3 p (SLVS)
187	VSS_DG	P	Digital ground	229	VSS_DG	P	Digital ground
188	hb_trg-	DI	Heartbeat trigger n (SLVS)	230	PCLAMP	DNC	POWER CUT RESERVED SPACE
189	hb_trg+	DI	Heartbeat trigger p (SLVS)	231	VDD_DG	P	Digital core voltage
190	trg-	DI	Event trigger n (SLVS)	232	VSS	P	PADRING ground
191	trg+	DI	Event trigger p (SLVS)	233	serialOut-[4]	DO	Serial data link 4 n (SLVS)
192	bx_sync_trg-	DI	Bunchcrossing counter sync n (SLVS)	234	serialOut+[4]	DO	Serial data link 4 p (SLVS)
193	bx_sync_trg+	DI	Bunchcrossing counter sync p (SLVS)	235	Nbflowstop_out_SO5-	DO	Stop neighbour data out or serial data link 5 n (SLVS)
194	VDD_DR	P	Digital SLVS drivers voltage	236	Nbflowstop_out_SO5+	DO	Stop neighbour data out or serial data link 5 p (SLVS)
195	PCLAMP	DNC	POWER CUT RESERVED SPACE	237	dinN-	DI	Neighbour chip data n (SLVS)
196	VSS_DR	P	Digital SLVS drivers ground	238	dinN+	DI	Neighbour chip data p (SLVS)
197	Hrstb-	DI	Reset n (SLVS)	239	VSS_DR	P	Digital SLVS drivers ground
198	Hrstb+	DI	Reset p (SLVS)	240	PCLAMP	DNC	POWER CUT RESERVED SPACE
199	VDD_DG	P	Digital core voltage	241	VDD_DR	P	Digital SLVS drivers voltage
200	PCLAMP	DNC	POWER CUT RESERVED SPACE	242	Nbflowstop_in-	DI	Stop neighbour data in n (SLVS)
201	VSS_DG	P	Digital ground	243	Nbflowstop_in+	DI	Stop neighbour data in p (SLVS)
202	clkADCin-	DI	ADC clock n (SLVS)	244	VSS_DG	P	Digital ground
203	clkADCin+	DI	ADC clock p (SLVS)	245	PCLAMP	DNC	POWER CUT RESERVED SPACE
204	clkBXin-	DI	Bunchcrossing clock n (SLVS)	246	VDD_DG	P	Digital core voltage
205	clkBXin+	DI	Bunchcrossing clock p (SLVS)	247	scl	I2C	I2C clock
206	VSS	DI	PADRING ground	248	sda_o	I2C	I2C data
207	clkSOin-	DI	Serial out clock n (SLVS)	249	sdo0-	DO	Scanchain test Scan Out (SLVS)
208	clkSOin+	DI	Serial out clock p (SLVS)	250	sdo0+	DO	Scanchain test Scan Out (SLVS)
209	VDD_DR	P	Digital SLVS drivers voltage	251	VSS	P	PADRING ground
210	PCLAMP	DNC	POWER CUT RESERVED SPACE	252	sdo2-	DO	Scanchain test Scan Out (SLVS)
211	VSS_DR	P	Digital SLVS drivers ground	253	sdo2+	DO	Scanchain test Scan Out (SLVS)
212	serialOut-[0]	DO	Serial data link 0 n (SLVS)	254	VSS_DR	P	Digital SLVS drivers ground
213	serialOut+[0]	DO	Serial data link 0 p (SLVS)	255	PCLAMP	DNC	POWER CUT RESERVED SPACE
214	VDD_DG	P	Digital core voltage	256	VDD_DR	P	Digital SLVS drivers voltage
215	PCLAMP	DNC	POWER CUT RESERVED SPACE	257	sdo4-	DO	Scanchain test Scan Out (SLVS)
216	VSS_DG	P	Digital ground	258	sdo4+	DO	Scanchain test Scan Out (SLVS)
217	serialOut-[1]	DO	Serial data link 1 n (SLVS)	259	VSS	P	PADRING ground

Table 15: Pad description part 4.

Pad #	Pad Name	IO type	Pad Description	Pad #	Pad Name	IO type	Pad Description
260	VSS_DG	P	Digital ground	306	VDD_DG	P	Digital core voltage
261	PCLAMP	DNC	POWER CUT RESERVED SPACE	307	clk_config[1]	DI	Clock configuration (Static)
262	VDD_DG	P	Digital core voltage	308	clk_config[0]	DI	Clock configuration (Static)
263	VSS	P	PADRING ground	309	VDD_DG	P	Digital core voltage
264	VDD_DG	P	Digital core voltage	310	PCLAMP	DNC	POWER CUT RESERVED SPACE
265	PCLAMP	DNC	POWER CUT RESERVED SPACE	311	VSS_DG	P	Digital ground
266	VSS_DG	P	Digital ground	312	VSS_DG	P	Digital ground
267	VSS_DG	P	Digital ground	313	PCLAMP	DNC	POWER CUT RESERVED SPACE
268	PCLAMP	DNC	POWER CUT RESERVED SPACE	314	VDD_DG	P	Digital core voltage
269	VDD_DG	P	Digital core voltage	315	VSS	P	PADRING ground
270	VSS	P	PADRING ground	316	VDD_DG	P	Digital core voltage
271	VDD_DG	P	Digital core voltage	317	PCLAMP	DNC	POWER CUT RESERVED SPACE
272	PCLAMP	DNC	POWER CUT RESERVED SPACE	318	VSS_DG	P	Digital ground
273	VSS_DG	P	Digital ground	319	VSS_DG	P	Digital ground
274	sclk	DI	Scanchain test clock (CMOS)	320	PCLAMP	DNC	POWER CUT RESERVED SPACE
275	VSS_DG	P	Digital ground	321	VDD_DG	P	Digital core voltage
276	PCLAMP	DNC	POWER CUT RESERVED SPACE	322	VSS	P	PADRING ground
277	VDD_DG	P	Digital core voltage	323	VREFP	P	Voltage reference p
278	sdi0	DI	Scanchain test Scan In (CMOS)	324	VREFP	P	Voltage reference p
279	sen0	DI	Scanchain test Scan Enable (CMOS)	325	VREFP	P	Voltage reference p
280	VSS_DG	P	Digital ground	326	VREFP	P	Voltage reference p
281	VSS_DG	P	Digital ground	327	VREFP	P	Voltage reference p
282	PCLAMP	DNC	POWER CUT RESERVED SPACE	328	VDD_AD	P	ADC supply voltage
283	VDD_DG	P	Digital core voltage	329	VSS_AD	P	ADC supply ground
284	sdi2	DI	Scanchain test Scan In (CMOS)	330	VDD_AD	P	ADC supply voltage
285	sen2	DI	Scanchain test Scan Enable (CMOS)	331	VSS_AD	P	ADC supply ground
286	sdi4	DI	Scanchain test Scan In (CMOS)	332	VDD_AD	P	ADC supply voltage
287	sen4	DI	Scanchain test Scan Enable (CMOS)	333	VSS_AD	P	ADC supply ground
288	VSS_DG	P	Digital ground	334	VDD_AD	P	ADC supply voltage
289	PCLAMP	DNC	POWER CUT RESERVED SPACE	335	VSS_AD	P	ADC supply ground
290	VDD_DG	P	Digital core voltage	336	VDD_AD	P	ADC supply voltage
291	clk_config[6]	DI	Clock configuration (Internal DSP Clock Gating) (Static)	337	VSS_AD	P	ADC supply ground
292	VSS	P	PADRING ground	338	VDD_AD	P	ADC supply voltage
293	TME	DI	Scanchain test ? TEST MODE EN (CMOS)	339	VSS_AD	P	ADC supply ground
294	clk_config[5]	DI	Clock configuration (Static)	340	VDD_AD	P	ADC supply voltage
295	clk_config[4]	DI	Clock configuration (Static)	341	VSS_AD	P	ADC supply ground
296	VDD_DG	P	Digital core voltage	342	V750	P	Bandgap voltage reference (750mV)
297	PCLAMP	DNC	POWER CUT RESERVED SPACE	343	V450	P	Bandgap voltage reference (450mV)
298	VSS_DG	P	Digital ground	344	V600	P	Bandgap voltage reference (600mV)
299	VSS_DG	P	Digital ground	345	VDD_FE2	P	Analog core voltage SS and output buffer
300	PCLAMP	DNC	POWER CUT RESERVED SPACE	346	VSS_FE2	P	Analog ground SS and output buffer
301	VDD_DG	P	Digital core voltage	347	VDD_FE2	P	Analog core voltage SS and output buffer
302	clk_config[3]	DI	Clock configuration (Static)	348	VSS_FE2	P	Analog ground SS and output buffer
303	clk_config[2]	DI	Clock configuration (Static)	349	VDD_FE2	P	Analog core voltage SS and output buffer
304	VSS_DG	P	Digital ground	350	VSS	P	PADRING ground
305	PCLAMP	DNC	POWER CUT RESERVED SPACE				

A.2.4. Pad Coordinates

Table 16: Pad coordinates part 1.

Pad #	Pad Name	X-coordinate	Y-coordinate	Pad #	Pad Name	X-coordinate	Y-coordinate
1	VSS_FE	35	8621.8	43	VDD_FE	35	4421.8
2	VDD_FE	35	8521.8	44	VSS	35	4321.8
3	VSS_FE	35	8421.8	45	IN[16]	35	4221.8
4	VDD_FE	35	8321.8	46	VSS_FE	35	4121.8
5	VSS_FE	35	8221.8	47	IN[17]	35	4021.8
6	VDD_FE	35	8121.8	48	VSS_FE	35	3921.8
7	VSS_FE	35	8021.8	49	IN[18]	35	3821.8
8	VDD_FE	35	7921.8	50	VSS_FE	35	3721.8
9	VSS	35	7821.8	51	IN[19]	35	3621.8
10	IN[0]	35	7721.8	52	VSS_FE	35	3521.8
11	VSS_FE	35	7621.8	53	IN[20]	35	3421.8
12	IN[1]	35	7521.8	54	VSS_FE	35	3321.8
13	VSS_FE	35	7421.8	55	IN[21]	35	3221.8
14	IN[2]	35	7321.8	56	VSS_FE	35	3121.8
15	VSS_FE	35	7221.8	57	IN[22]	35	3021.8
16	IN[3]	35	7121.8	58	VSS_FE	35	2921.8
17	VSS_FE	35	7021.8	59	IN[23]	35	2821.8
18	IN[4]	35	6921.8	60	VSS	35	2721.8
19	VSS_FE	35	6821.8	61	IN[24]	35	2621.8
20	IN[5]	35	6721.8	62	VSS_FE	35	2521.8
21	VSS_FE	35	6621.8	63	IN[25]	35	2421.8
22	IN[6]	35	6521.8	64	VSS_FE	35	2321.8
23	VSS_FE	35	6421.8	65	IN[26]	35	2221.8
24	IN[7]	35	6321.8	66	VSS_FE	35	2121.8
25	VSS	35	6221.8	67	IN[27]	35	2021.8
26	IN[8]	35	6121.8	68	VSS_FE	35	1921.8
27	VSS_FE	35	6021.8	69	IN[28]	35	1821.8
28	IN[9]	35	5921.8	70	VSS_FE	35	1721.8
29	VSS_FE	35	5821.8	71	IN[29]	35	1621.8
30	IN[10]	35	5721.8	72	VSS_FE	35	1521.8
31	VSS_FE	35	5621.8	73	IN[30]	35	1421.8
32	IN[11]	35	5521.8	74	VSS_FE	35	1321.8
33	VSS_FE	35	5421.8	75	IN[31]	35	1221.8
34	IN[12]	35	5321.8	76	VSS	35	1121.8
35	VSS_FE	35	5221.8	77	VDD_FE	35	1021.8
36	IN[13]	35	5121.8	78	VSS_FE	35	921.8
37	VSS_FE	35	5021.8	79	VDD_FE	35	821.8
38	IN[14]	35	4921.8	80	VSS_FE	35	721.8
39	VSS_FE	35	4821.8	81	VDD_FE	35	621.8
40	IN[15]	35	4721.8	82	VSS_FE	35	521.8
41	VSS	35	4621.8	83	VDD_FE	35	421.8
42	VDD_FE	35	4521.8	84	VSS_FE	35	321.8

Table 17: Pad coordinates part 2.

Pad #	Pad Name	X-coordinate	Y-coordinate	Pad #	Pad Name	X-coordinate	Y-coordinate
85	VSS	266.8	35	131	VSS_DG	4866.8	35
86	VDD_FE2	366.8	35	132	hadd[1]	4966.8	35
87	VSS_FE2	466.8	35	133	hadd[0]	5066.8	35
88	VDD_FE2	566.8	35	134	VDD_DG	5166.8	35
89	CTS	666.8	35	135	PCLAMP	5266.8	35
90	CG\$<0>\$	766.8	35	136	VSS_DG	5366.8	35
91	CG\$<1>\$	866.8	35	137	VSS_DG	5466.8	35
92	POL	966.8	35	138	PCLAMP	5566.8	35
93	VSS_FE2	1066.8	35	139	VDD_DG	5666.8	35
94	VSS_AD	1166.8	35	140	sme	5766.8	35
95	VDD_AD	1266.8	35	141	sen3	5866.8	35
96	VSS_AD	1366.8	35	142	sdi3	5966.8	35
97	VDD_AD	1466.8	35	143	VSS	6066.8	35
98	VSS_AD	1566.8	35	144	sdi1	6166.8	35
99	VDD_AD	1666.8	35	145	VDD_DG	6266.8	35
100	VSS_AD	1766.8	35	146	PCLAMP	6366.8	35
101	VDD_AD	1866.8	35	147	VSS_DG	6466.8	35
102	VSS_AD	1966.8	35	148	sen1	6566.8	35
103	VDD_AD	2066.8	35	149	PORin	6666.8	35
104	VSS_AD	2166.8	35	150	PORout	6766.8	35
105	VDD_AD	2266.8	35	151	TRST	6866.8	35
106	VSS_AD	2366.8	35	152	VDD_DG	6966.8	35
107	VDD_AD	2466.8	35	153	PCLAMP	7066.8	35
108	VREFP	2566.8	35	154	VSS_DG	7166.8	35
109	VREFP	2666.8	35	155	TMS	7266.8	35
110	VREFP	2766.8	35	156	TDI	7366.8	35
111	VREFP	2866.8	35	157	TCLK	7466.8	35
112	VREFP	2966.8	35	158	VDD_DG	7566.8	35
113	VSS	3066.8	35	159	PCLAMP	7666.8	35
114	VDD_DG	3166.8	35	160	VSS_DG	7766.8	35
115	PCLAMP	3266.8	35	161	VSS_DG	7866.8	35
116	VSS_DG	3366.8	35	162	VSS_DG	7966.8	35
117	VSS_DG	3466.8	35	163	PCLAMP	8066.8	35
118	PCLAMP	3566.8	35	164	VDD_DG	8166.8	35
119	VDD_DG	3666.8	35	165	VSS	8266.8	35
120	VSS	3766.8	35	166	VSS_DG	8366.8	35
121	VDD_DG	3866.8	35	167	TDO	8466.8	35
122	PCLAMP	3966.8	35	168	smo	8566.8	35
123	VSS_DG	4066.8	35	169	VDD_DG	8666.8	35
124	VSS_DG	4166.8	35	170	PCLAMP	8766.8	35
125	PCLAMP	4266.8	35	171	VSS_DG	8866.8	35
126	VDD_DG	4366.8	35	172	VSS	8966.8	35
127	hadd[3]	4466.8	35	173	VDD_DG	9066.8	35
128	hadd[2]	4566.8	35	174	PCLAMP	9166.8	35
129	VDD_DG	4666.8	35	175	VSS_DG	9266.8	35
130	PCLAMP	4766.8	35				

Table 18: Pad coordinates part 3.

Pad #	Pad Name	X-coordinate	Y-coordinate	Pad #	Pad Name	X-coordinate	Y-coordinate
176	VSS	9498.6	321.8	218	serialOut+[1]	9498.6	100
177	sdo3-	9498.6	421.8	219	serialOut-[2]	9498.6	200
178	sdo3+	9498.6	521.8	220	serialOut+[2]	9498.6	300
179	VDD_DR	9498.6	621.8	221	VSS_DG	9498.6	400
180	PCLAMP	9498.6	721.8	222	PCLAMP	9498.6	500
181	VSS_DR	9498.6	821.8	223	VDD_DG	9498.6	600
182	sdo1-	9498.6	921.8	224	VSS_DR	9498.6	700
183	sdo1+	9498.6	1021.8	225	PCLAMP	9498.6	800
184	VSS	9498.6	1121.8	226	VDD_DR	9498.6	900
185	VDD_DG	9498.6	1221.8	227	serialOut-[3]	9498.6	1000
186	PCLAMP	9498.6	1321.8	228	serialOut+[3]	9498.6	1100
187	VSS_DG	9498.6	1421.8	229	VSS_DG	9498.6	1200
188	hb_trg-	9498.6	1521.8	230	PCLAMP	9498.6	1300
189	hb_trg+	9498.6	1621.8	231	VDD_DG	9498.6	1400
190	trg-	9498.6	1721.8	232	VSS	9498.6	1500
191	trg+	9498.6	1821.8	233	serialOut-[4]	9498.6	1600
192	bx_sync_trg-	9498.6	1921.8	234	serialOut+[4]	9498.6	1700
193	bx_sync_trg+	9498.6	2021.8	235	Nbflowstop_out_SO5-	9498.6	1800
194	VDD_DR	9498.6	2121.8	236	Nbflowstop_out_SO5+	9498.6	1900
195	PCLAMP	9498.6	2221.8	237	dinN-	9498.6	2000
196	VSS_DR	9498.6	2321.8	238	dinN+	9498.6	2100
197	Hrstb-	9498.6	2421.8	239	VSS_DR	9498.6	2200
198	Hrstb+	9498.6	2521.8	240	PCLAMP	9498.6	2300
199	VDD_DG	9498.6	2621.8	241	VDD_DR	9498.6	2400
200	PCLAMP	9498.6	2721.8	242	Nbflowstop_in-	9498.6	2500
201	VSS_DG	9498.6	2821.8	243	Nbflowstop_in+	9498.6	2600
202	clkADCin-	9498.6	2921.8	244	VSS_DG	9498.6	2700
203	clkADCin+	9498.6	3021.8	245	PCLAMP	9498.6	2800
204	clkBXin-	9498.6	3121.8	246	VDD_DG	9498.6	2900
205	clkBXin+	9498.6	3221.8	247	scl	9498.6	3000
206	VSS	9498.6	3321.8	248	sda_o	9498.6	3100
207	clkSOin-	9498.6	3421.8	249	sdo0-	9498.6	3200
208	clkSOin+	9498.6	3521.8	250	sdo0+	9498.6	3300
209	VDD_DR	9498.6	3621.8	251	VSS	9498.6	3400
210	PCLAMP	9498.6	3721.8	252	sdo2-	9498.6	3500
211	VSS_DR	9498.6	3821.8	253	sdo2+	9498.6	3600
212	serialOut-[0]	9498.6	3921.8	254	VSS_DR	9498.6	3700
213	serialOut+[0]	9498.6	4021.8	255	PCLAMP	9498.6	3800
214	VDD_DG	9498.6	4121.8	256	VDD_DR	9498.6	3900
215	PCLAMP	9498.6	4221.8	257	sdo4-	9498.6	4000
216	VSS_DG	9498.6	4321.8	258	sdo4+	9498.6	4100
217	serialOut-[1]	9498.6	4421.8	259	VSS	9498.6	4200

Table 19: Pad coordinates part 4.

Pad #	Pad Name	X-coordinate	Y-coordinate	Pad #	Pad Name	X-coordinate	Y-coordinate
260	VSS_DG	9266.8	8908.6	306	VDD_DG	4666.8	8908.6
261	PCLAMP	9166.8	8908.6	307	clk_config[1]	4566.8	8908.6
262	VDD_DG	9066.8	8908.6	308	clk_config[0]	4466.8	8908.6
263	VSS	8966.8	8908.6	309	VDD_DG	4366.8	8908.6
264	VDD_DG	8866.8	8908.6	310	PCLAMP	4266.8	8908.6
265	PCLAMP	8766.8	8908.6	311	VSS_DG	4166.8	8908.6
266	VSS_DG	8666.8	8908.6	312	VSS_DG	4066.8	8908.6
267	VSS_DG	8566.8	8908.6	313	PCLAMP	3966.8	8908.6
268	PCLAMP	8466.8	8908.6	314	VDD_DG	3866.8	8908.6
269	VDD_DG	8366.8	8908.6	315	VSS	3766.8	8908.6
270	VSS	8266.8	8908.6	316	VDD_DG	3666.8	8908.6
271	VDD_DG	8166.8	8908.6	317	PCLAMP	3566.8	8908.6
272	PCLAMP	8066.8	8908.6	318	VSS_DG	3466.8	8908.6
273	VSS_DG	7966.8	8908.6	319	VSS_DG	3366.8	8908.6
274	sclk	7866.8	8908.6	320	PCLAMP	3266.8	8908.6
275	VSS_DG	7766.8	8908.6	321	VDD_DG	3166.8	8908.6
276	PCLAMP	7666.8	8908.6	322	VSS	3066.8	8908.6
277	VDD_DG	7566.8	8908.6	323	VREFP	2966.8	8908.6
278	sdi0	7466.8	8908.6	324	VREFP	2866.8	8908.6
279	sen0	7366.8	8908.6	325	VREFP	2766.8	8908.6
280	VSS_DG	7266.8	8908.6	326	VREFP	2666.8	8908.6
281	VSS_DG	7166.8	8908.6	327	VREFP	2566.8	8908.6
282	PCLAMP	7066.8	8908.6	328	VDD_AD	2466.8	8908.6
283	VDD_DG	6966.8	8908.6	329	VSS_AD	2366.8	8908.6
284	sdi2	6866.8	8908.6	330	VDD_AD	2266.8	8908.6
285	sen2	6766.8	8908.6	331	VSS_AD	2166.8	8908.6
286	sdi4	6666.8	8908.6	332	VDD_AD	2066.8	8908.6
287	sen4	6566.8	8908.6	333	VSS_AD	1966.8	8908.6
288	VSS_DG	6466.8	8908.6	334	VDD_AD	1866.8	8908.6
289	PCLAMP	6366.8	8908.6	335	VSS_AD	1766.8	8908.6
290	VDD_DG	6266.8	8908.6	336	VDD_AD	1666.8	8908.6
291	clk_config[6]	6166.8	8908.6	337	VSS_AD	1566.8	8908.6
292	VSS	6066.8	8908.6	338	VDD_AD	1466.8	8908.6
293	TME	5966.8	8908.6	339	VSS_AD	1366.8	8908.6
294	clk_config[5]	5866.8	8908.6	340	VDD_AD	1266.8	8908.6
295	clk_config[4]	5766.8	8908.6	341	VSS_AD	1166.8	8908.6
296	VDD_DG	5666.8	8908.6	342	V750	1066.8	8908.6
297	PCLAMP	5566.8	8908.6	343	V450	966.8	8908.6
298	VSS_DG	5466.8	8908.6	344	V600	866.8	8908.6
299	VSS_DG	5366.8	8908.6	345	VDD_FE2	766.8	8908.6
300	PCLAMP	5266.8	8908.6	346	VSS_FE2	666.8	8908.6
301	VDD_DG	5166.8	8908.6	347	VDD_FE2	566.8	8908.6
302	clk_config[3]	5066.8	8908.6	348	VSS_FE2	466.8	8908.6
303	clk_config[2]	4966.8	8908.6	349	VDD_FE2	366.8	8908.6
304	VSS_DG	4866.8	8908.6	350	VSS	266.8	8908.6
305	PCLAMP	4766.8	8908.6				

A.3. Electrical Specifications

A.3.1. Power Domains

The SAMPA ASIC has five power-domains, as follows:

FE Analogue front-end: First Shaper and Charge Sensitive Amplifier

FE2 Analogue Front-end: Second Shaper and Output Buffer

AD ADC

DG Core digital logic

DR SLVS IO drivers

Each power domain has its corresponding VDD and VSS net. Additionally, there is a separate IO padding ground for the IO pad ESD diodes named just VSS. Figure 14 shows how the domains are separated through the padding and which blocks are connected to each domain. Table 20 describes power nets, names, nominal voltages and observations for each domain

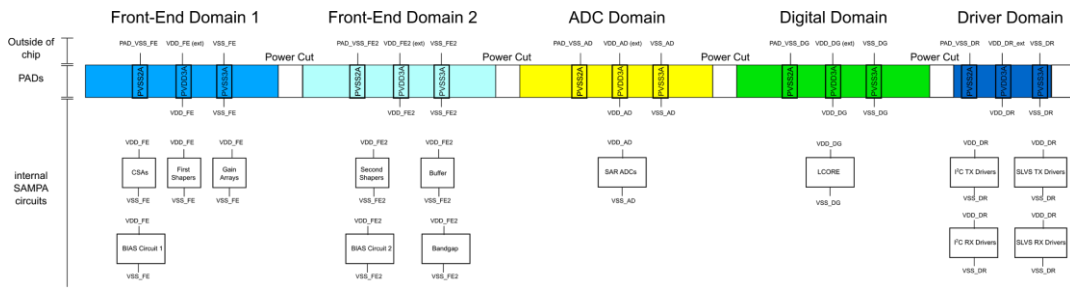


Figure 14: Power domains.

Table 20: Power nets per domain.

Power Net	Name	Nominal Voltage	Observation
Frontend Domain 1			
Ground	VSS_FE	0 V	
Supply Voltage	VSS_FE	1.25 V	
PADRING ground	VSS	0 V	common to all domains
Frontend Domain 2			
Ground	VSS_FE2	0 V	
Supply Voltage	VSS_FE2	1.25 V	
PADRING ground	VSS	0 V	common to all domains
ADC Domain			
Ground	VSS_AD	0 V	
Supply Voltage	VSS_AD	1.25 V	
PADRING ground	VSS	0 V	common to all domains

A.3.2. DSP Domain

Table 21: DSP Power nets.

Ground	VSS_DC	0 V	
Supply Voltage	VSS_DC	1.25 V	
PADRING ground	VSS	0 V	common to all domains
Driver Domain			
Ground	VSS_DR	0 V	
Supply Voltage	VSS_DR	1.25 V	
PADRING ground	VSS	0 V	common to all domains

A.3.3. Absolute maximum ratings

The nominal supply voltage of the SAMPA_V4 chip is 1.25V with variation range of 5%, being: $1.1875V < 1.25V < 1.325V$.

Absolute maximum ratings are limiting values to be considered individually when all other parameters are within their specified operating range (table20).

Operating the SAMPA_V4 under conditions beyond its absolute maximum ratings may damage the device and affect the device reliability.

Table 22: Absolute maximum ratings

	Parameter	Rating
VDD_FE, VDD_FE2	Power supply voltage	1.18V to 1.33V
VDD_AD, VDD_DG, VDD_DR	Power supply voltage	1.18V to 1.33V
V_{IN}	Voltage applied to any input or output pin	-0.5V to 1.25V
T_S	Storage temperature	-55°C to +150°C
V_{HBM}	Electrostatic discharge rating, human body model	1500V
V_{CDM}	Electrostatic discharge rating, charge device model	200V

A.4. Package

The SAMPA_V4 mechanical specifications are presented in this chapter, including its physical dimensions and visible markings.

A.4.1. Package description

The SAMPA_V4 IC is available in the TFBGA package that includes a large center ground slug for electrical grounding, mechanical strength, and thermal continuity. The package has a 15 mm x 15 mm body size, 1.2 mm thickness and a 0.65 mm ball pitch. The package provides 372 balls. Figure 15 the mechanical data and package dimensions.

The SAMPA chip is a mixed signal chip, where extreme care should be taken to avoid interference and crosstalk between analog and digital domain. The package substrate should therefore keep well-separated traces of different domains. The large center slug must be soldered to PCB ground for electrical ground, mechanical support, and thermal relief.

The package keeps separated the different power domains of the die. Figure 16 presents shows the ball layout of the package. White cells are signals (either in or out), blue cells are GND, while orange are VDD (each tone identifies a different power domain).

Figures 17-20 show the layouts of the 4-substrate layers. The second layer is a ground plane, with shielding purposes, while in the others is visible the separation in different domains.

In order to improve overall performance, the package includes, on the substrate inside the package, a capacitor between ground and power for the two most sensitive domains: the power for the ADC (VDD_AD) and the voltage reference for the ADC (VREFP). In both cases a 100nF 0603 SMD capacitor is embedded in the package.

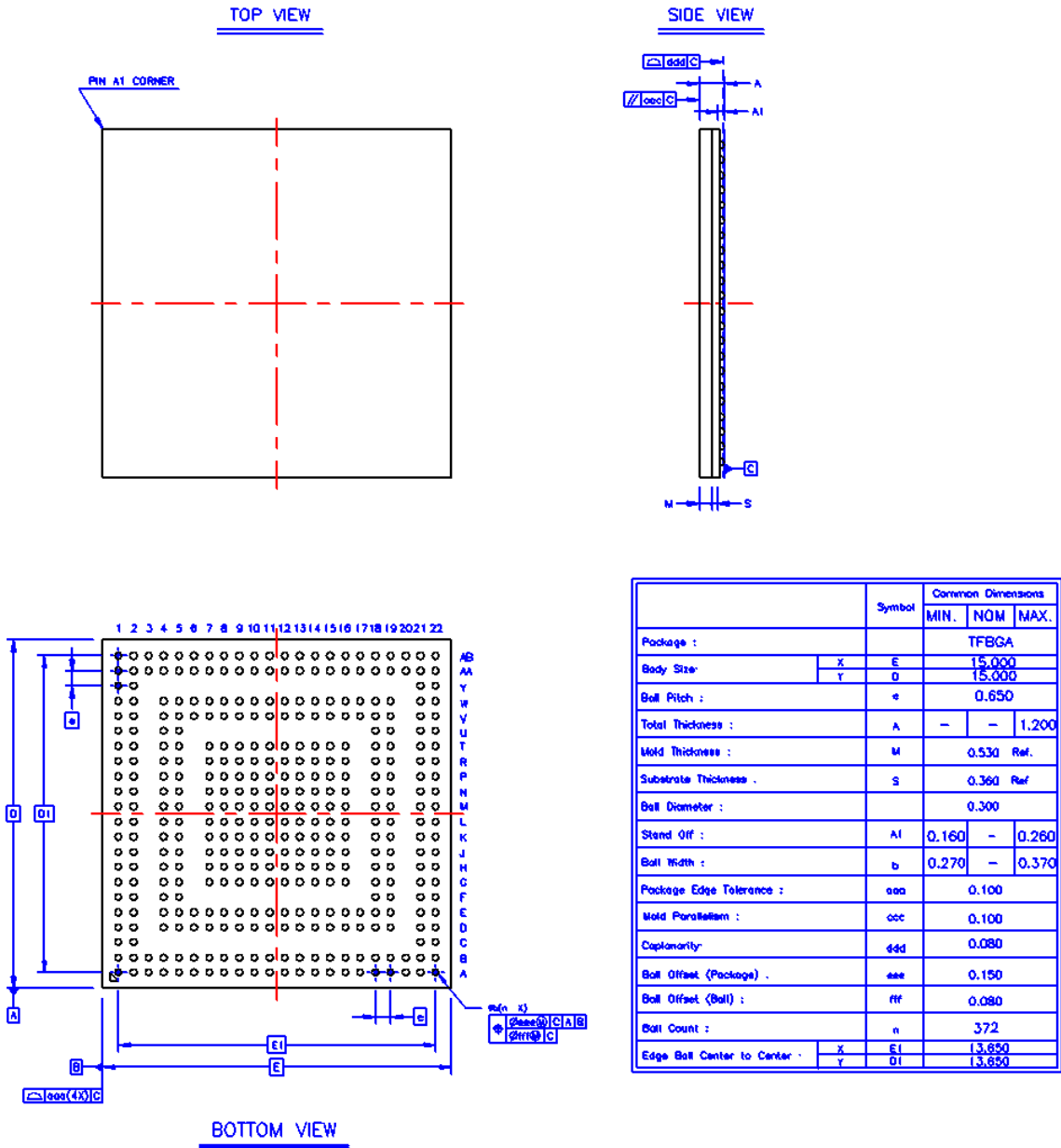


Figure 15: Mechanical data and package dimensions.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	IN[1]	IN[0]	N/C	V450	V600	V750	VREFP	VREFP	VREFP	clk_config[3]	clk_config[4]	clk_config[5]	VSS_DG	scik	sen4	sen2	sen0	N/C	N/C	sdo4-	N/C	sdo2-	A
B	IN[2]	N/C	VDD_FE2	VDD_FE2	VDD_AD	VDD_AD	VDD_AD	VREFP	VREFP	clk_config[0]	clk_config[1]	clk_config[2]	VSS_DG	clk_config[6]	TME	sd4	sd2	sd0	N/C	sdo4+	N/C	sdo2+	B
C	IN[3]	VSS_FE																			sd0-	sdo0+	C
D	IN[4]	N/C		VSS	VSS_AD	VSS_AD	VDD_AD	VDD_AD	VDD_AD	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VSS_DG	VSS_DG		sda_o	scl	D
E	IN[5]	VSS_FE		VDD_FE	VSS	VSS_AD	VDD_AD	VDD_AD	VDD_AD	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DR	VDD_DR	VDD_DG	NBflowsto p_in-	NBflowsto p_in+		VSS_DG	VSS_DG	E
F	IN[6]	N/C		VDD_FE	VSS_FE2																VSS_DG	VSS_DG	F
G	IN[7]	VSS_FE		VDD_FE	VSS_FE2		VSS_AD	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DR	VSS_DG	VDD_DG		NBflowsto p_out_SO 5-	NBflowsto p_out_SO 5+		VSS_DG	VSS_DG	G
H	IN[8]	IN[9]		VDD_FE	VSS_FE2		VSS_AD	VSS_DG	VSS_DG	VSS_DG	VSS	VSS_DG	VSS	VSS	VSS	VDD_DG		VSS_DG	VSS_DG		serialOut- [3]	serialOut+ [3]	H
J	IN[10]	IN[11]		VDD_FE	VSS_FE		VSS_AD	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DR	VSS_DG	VDD_DR		serialOut- [4]	serialOut+ [4]		VSS_DG	VSS_DG	J
K	IN[12]	IN[13]		VDD_FE	VSS_FE		VSS_AD	VSS_DG	VSS_DG	VSS_DG	VSS	VSS_DG	VSS	VSS_DR	VSS_DG	VDD_DG		VSS_DG	VSS_DG		serialOut- [2]	serialOut+ [2]	K
L	IN[14]	IN[15]		VDD_FE	VSS_FE		VSS_AD	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS	VSS	VDD_DG		serialOut- [0]	serialOut+ [0]		VSS_DG	VSS_DG	L
M	IN[16]	IN[17]		VDD_FE	VSS_FE		VSS_AD	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DR	VSS_DG	VDD_DG		VSS_DG	VSS_DG		serialOut- [1]	serialOut+ [1]	M
N	IN[18]	IN[19]		VDD_FE	VSS_FE		VSS_AD	VSS_DG	VSS_DG	VSS_DG	VSS	VSS_DG	VSS	VSS_DG	VSS_DR	VDD_DG		clkSOin-	clkSOin+		VSS_DG	VSS_DG	N
P	IN[20]	IN[21]		VDD_FE	VSS_FE		VSS_AD	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VDD_DR		VSS_DG	VSS_DG		Hrstb-	Hrstb+	P
R	IN[22]	IN[23]		VDD_FE	VSS_FE		VSS_AD	VSS_DG	VSS_DG	VSS_DG	VSS	VSS_DG	VSS	VSS	VSS	VDD_DG		clkBXin-	clkBXin+		VSS_DG	VSS_DG	R
T	IN[24]	VSS_FE		VDD_FE	VSS_FE2		VSS_AD	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DG	VSS_DR	VSS_DG	VDD_DG		VSS_DG	VSS_DG		trg-	trg+	T
U	IN[25]	N/C		VDD_FE	VSS_FE2													clkADCin-	clkADCin+		VSS_DG	VSS_DG	U
V	IN[26]	VSS_FE		VDD_FE	VSS	VSS_AD	VDD_AD	VDD_AD	VDD_AD	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DR	VDD_DG	VDD_DG	VSS_DG	VSS_DG		hb_trg-	hb_trg+	V
W	IN[27]	N/C		VSS	VSS_AD	VSS_AD	VDD_AD	VDD_AD	VDD_AD	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DG	VDD_DG	bx_sync1 rg-	bx_sync1 rg+		VSS_DG	VSS_DG	W
Y	IN[28]	VSS_FE																			sd01-	sd01+	Y
AA	IN[29]	N/C	CTS	CG<0>	VDD_FE2	VDD_FE2	VDD_FE2	VREFP	VREFP	hadd[2]	hadd[0]	sme	sd3	sen1	sno	TRST	TDI	TDO	N/C	sd03-	N/C	VSS_DG	AA
AB	IN[30]	IN[31]	N/C	CG<1>	N/C	POL	VREFP	VREFP	VREFP	hadd[3]	hadd[1]	sen3	sd1	PORin	PORout	TMS	TCLK	N/C	VSS_DG	sd03+	N/C	N/C	AB

Figure 16: BGA ball layout (Top View)

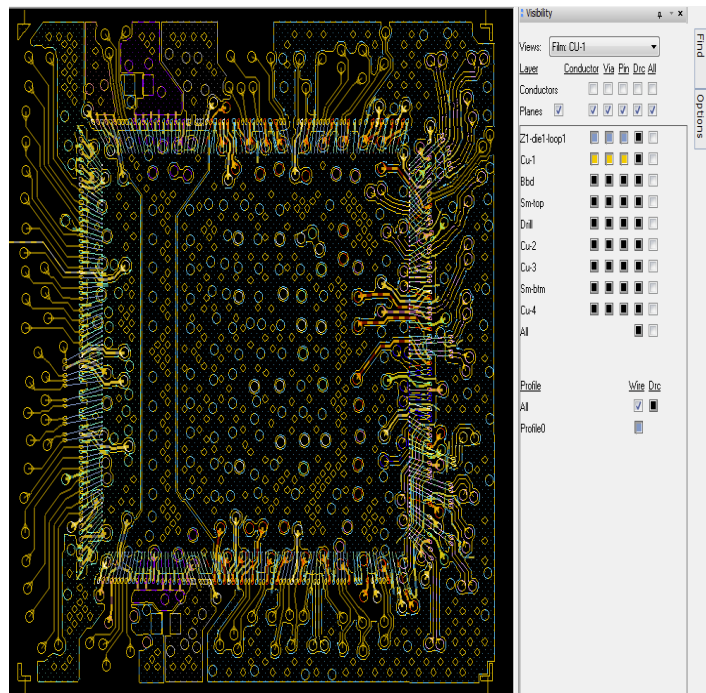


Figure 17: Layout of the first layer of the BGA substrate. Bond diagram is superimposed

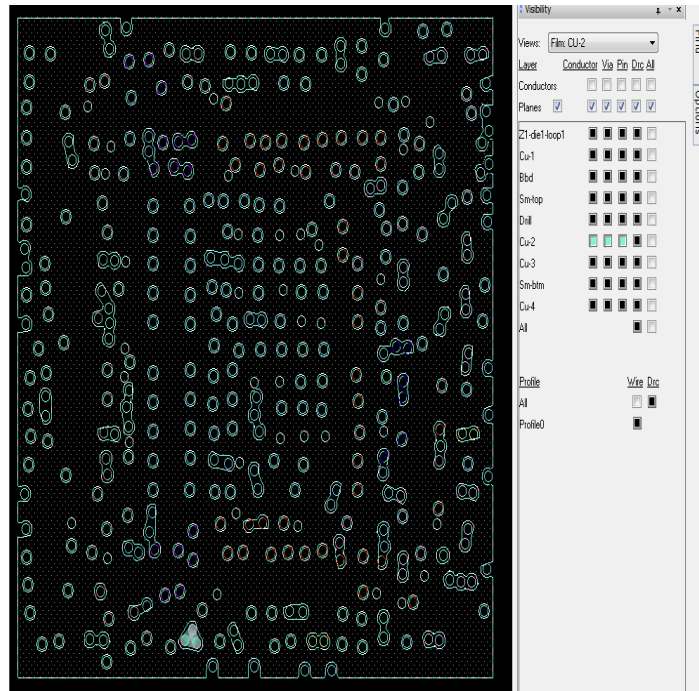


Figure 18: Layout of the 2nd layer of the BGA substrate, a pure GND plane

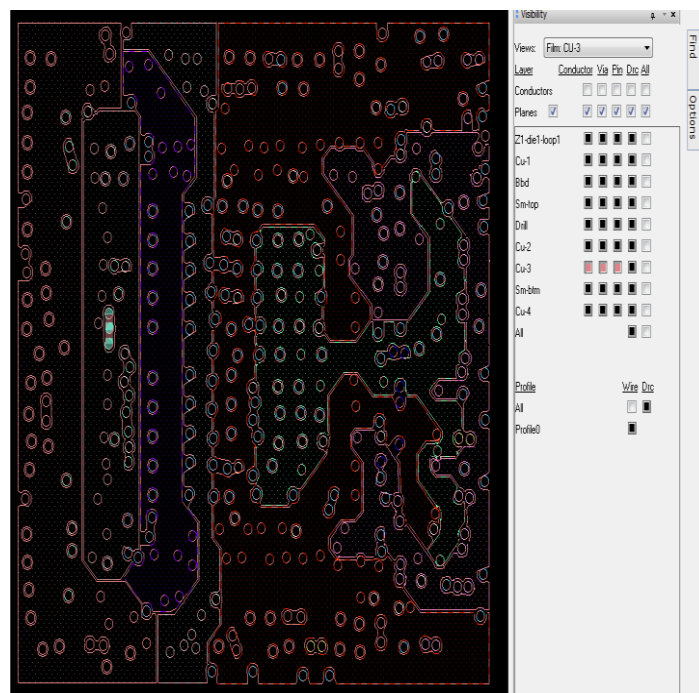


Figure 19: Layout of the 3rd layer of the BGA substrate. The presence of different domains is visible

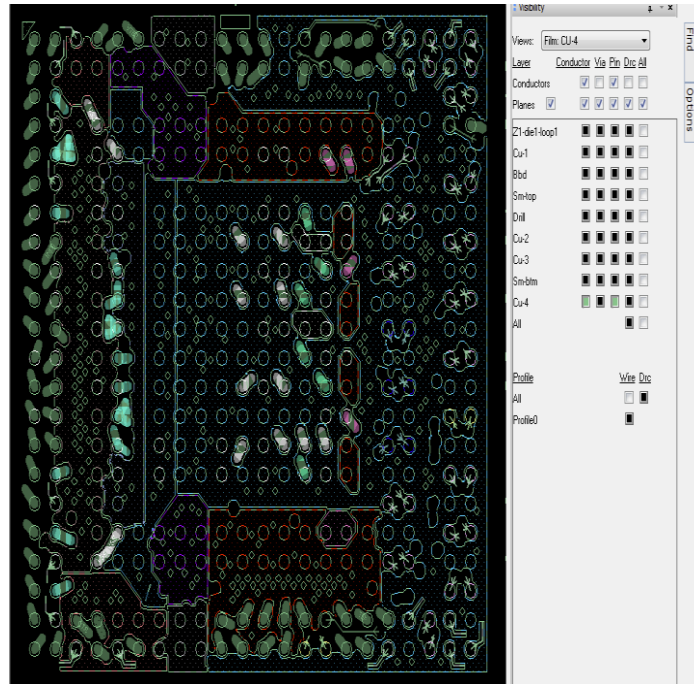


Figure 20: Layout of the 4th layer of the BGA substrate. Power domains separation is clearly visible (different colors)

A.4.2. Pinout

All input pins must be driven by a valid logic level: $0 < \text{“logic zero”} < 0.2 \text{ V}$ or $1.1 < \text{“logic one”} < 1.3 \text{ V}$. Unused single-ended input pins should be tie high or low through a resistor (the same resistor can serve many pins). Differential inputs must be set to “0” or “1” by tying the non-inverting input low/high and the inverting input high/low respectively. The method to tie low/high each input of a differential signal is the same as for the single-ended inputs. Output pins can be left floating. Pins marked N/C are unconnected in the package.

Table 23: Pinout part 1

Ball	Netname	Domain	IO type	Direction	Speed	Description
A1	IN[1]	Analog	Analog	in	0	Analog channel 1
A2	IN[0]	Analog	Analog	in	0	Analog channel 0
A3	N/C	-	-	-	-	Not connected
A4	V450	Analog	Power	in/out	0	Bandgap voltage reference (450mV)
A5	V600	Analog	Power	in/out	0	Bandgap voltage reference (600mV)
A6	V750	Analog	Power	in/out	0	Bandgap voltage reference (750mV)
A7	VREFP	Analog	Power	in	0	Voltage reference p
A8	VREFP	Analog	Power	in	0	Voltage reference p
A9	VREFP	Analog	Power	in	0	Voltage reference p
A10	clk_config[3]	Digital	Static	in	Static	Clock configuration
A11	clk_config[4]	Digital	Static	in	Static	Clock configuration
A12	clk_config[5]	Digital	Static	in	Static	Clock configuration
A13	VSS_DG	Digital	Power	in	0	Digital ground
A14	sclk	Digital	CMOS	in	20MHz	Scanchain test clock
A15	sen4	Digital	CMOS	in	20MHz	Scanchain test Scan Enable
A16	sen2	Digital	CMOS	in	20MHz	Scanchain test Scan Enable
A17	sen0	Digital	CMOS	in	20MHz	Scanchain test Scan Enable
A18	N/C	-	-	-	-	Not connected
A19	N/C	-	-	-	-	Not connected
A20	sdo4-	Digital	SLVS	out	160MHz	Scanchain test Scan Out SLVS
A21	N/C	-	-	-	-	Not connected
A22	sdo2-	Digital	SLVS	out	160MHz	Scanchain test Scan Out SLVS
B1	IN[2]	Analog	Analog	in	0	Analog channel 2
B2	N/C	-	-	-	-	Not connected
B3	VDD_FE2	Analog	Power	in	0	Analog core voltage SS and output buffer
B4	VDD_FE2	Analog	Power	in	0	Analog core voltage SS and output buffer
B5	VDD_AD	Analog	Power	in	0	ADC supply voltage
B6	VDD_AD	Analog	Power	in	0	ADC supply voltage
B7	VDD_AD	Analog	Power	in	0	ADC supply voltage
B8	VREFP	Analog	Power	in	0	Voltage reference p
B9	VREFP	Analog	Power	in	0	Voltage reference p
B10	clk_config[0]	Digital	Static	in	Static	Clock configuration
B11	clk_config[1]	Digital	Static	in	Static	Clock configuration
B12	clk_config[2]	Digital	Static	in	Static	Clock configuration
B13	VSS_DG	Digital	Power	in	0	Digital ground
B14	clk_config[6]	Digital	Static	in	Static	Clock configuration (Internal DSP Clock Gating)
B15	TME	Digital	CMOS	in	Static	Scanchain test – TEST MODE EN
B16	sdi4	Digital	CMOS	in	20MHz	Scanchain test Scan In
B17	sdi2	Digital	CMOS	in	20MHz	Scanchain test Scan In
B18	sdi0	Digital	CMOS	in	20MHz	Scanchain test Scan In
B19	N/C	-	-	-	-	Not connected
B20	sdo4+	Digital	SLVS	out	160MHz	Scanchain test Scan Out SLVS
B21	N/C	-	-	-	-	Not connected
B22	sdo2+	Digital	SLVS	out	160MHz	Scanchain test Scan Out SLVS

Table 24: Pinout part 2

Ball	Netname	Domain	IO type	Direction	Speed	Description
C1	IN[3]	Analog	Analog	in	0	Analog channel 3
C2	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
C21	sdo0-	Digital	SLVS	out	160MHz	Scanchain test Scan Out SLVS
C22	sdo0+	Digital	SLVS	out	160MHz	Scanchain test Scan Out SLVS
D1	IN[4]	Analog	Analog	in	0	Analog channel 4
D2	N/C	-	-	-	-	Not connected
D4	VSS	Analog/Digital	Power	in	0	PADRING ground
D5	VSS_AD	Analog	Power	in	0	ADC supply ground
D6	VSS_AD	Analog	Power	in	0	ADC supply ground
D7	VDD_AD	Analog	Power	in	0	ADC supply voltage
D8	VDD_AD	Analog	Power	in	0	ADC supply voltage
D9	VDD_AD	Analog	Power	in	0	ADC supply voltage
D10	VDD_DG	Digital	Power	in	0	Digital core voltage
D11	VDD_DG	Digital	Power	in	0	Digital core voltage
D12	VDD_DG	Digital	Power	in	0	Digital core voltage
D13	VDD_DG	Digital	Power	in	0	Digital core voltage
D14	VDD_DG	Digital	Power	in	0	Digital core voltage
D15	VDD_DG	Digital	Power	in	0	Digital core voltage
D16	VDD_DG	Digital	Power	in	0	Digital core voltage
D17	VDD_DG	Digital	Power	in	0	Digital core voltage
D18	VSS_DG	Digital	Power	in	0	Digital ground
D19	VSS_DG	Digital	Power	in	0	Digital ground
D21	sda_o	Digital	I2C	in/out	1MHz	I2C data
D22	scl	Digital	I2C	in	1MHz	I2C clock
E1	IN[5]	Analog	Analog	in	0	Analog channel 5
E2	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
E4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
E5	VSS	Analog/Digital	Power	in	0	PADRING ground
E6	VSS_AD	Analog	Power	in	0	ADC supply ground
E7	VDD_AD	Analog	Power	in	0	ADC supply voltage
E8	VDD_AD	Analog	Power	in	0	ADC supply voltage
E9	VDD_AD	Analog	Power	in	0	ADC supply voltage
E10	VDD_DG	Digital	Power	in	0	Digital core voltage
E11	VDD_DG	Digital	Power	in	0	Digital core voltage
E12	VDD_DG	Digital	Power	in	0	Digital core voltage
E13	VDD_DG	Digital	Power	in	0	Digital core voltage
E14	VDD_DG	Digital	Power	in	0	Digital core voltage
E15	VDD_DR	Digital	Power	in	0	Digital SLVS drivers voltage
E16	VDD_DR	Digital	Power	in	0	Digital SLVS drivers voltage
E17	VDD_DG	Digital	Power	in	0	Digital core voltage
E18	NBflowstop_in-	Digital	SLVS	in	160MHz	Stop neighbour data in n
E19	NBflowstop_in+	Digital	SLVS	in	160MHz	Stop neighbour data in p
E21	VSS_DG	Digital	Power	in	0	Digital ground
E22	VSS_DG	Digital	Power	in	0	Digital ground

Table 25: Pinout part 3

Ball	Netname	Domain	IO type	Direction	Speed	Description
F1	IN[6]	Analog	Analog	in	0	Analog channel 6
F2	N/C	-	-	-	-	Not connected
F4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
F5	VSS_FE2	Analog	Power	in	0	Analog ground SS and output buffer
F18	VSS_DG	Digital	Power	in	0	Digital ground
F19	VSS_DG	Digital	Power	in	0	Digital ground
F21	dinN-	Digital	SLVS	in	160MHz	Neighbour chip data n
F22	dinN+	Digital	SLVS	in	160MHz	Neighbour chip data p
G1	IN[7]	Analog	Analog	in	0	Analog channel 7
G2	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
G4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
G5	VSS_FE2	Analog	Power	in	0	Analog ground SS and output buffer
G7	VSS_AD	Analog	Power	in	0	ADC supply ground
G8	VSS_DG	Digital	Power	in	0	Digital ground
G9	VSS_DG	Digital	Power	in	0	Digital ground
G10	VSS_DG	Digital	Power	in	0	Digital ground
G11	VSS_DG	Digital	Power	in	0	Digital ground
G12	VSS_DG	Digital	Power	in	0	Digital ground
G13	VSS_DG	Digital	Power	in	0	Digital ground
G14	VSS_DR	Digital	Power	in	0	Digital SLVS drivers ground
G15	VSS_DG	Digital	Power	in	0	Digital ground
G16	VDD_DG	Digital	Power	in	0	Digital core voltage
G18	NBflowstop_o ut_SO5-	Digital	SLVS	out	160MHz	Stop neighbour data out or serial data link 5 n
G19	NBflowstop_o ut_SO5+	Digital	SLVS	out	160MHz	Stop neighbour data out or serial data link 5 p
G21	VSS_DG	Digital	Power	in	0	Digital ground
G22	VSS_DG	Digital	Power	in	0	Digital ground
H1	IN[8]	Analog	Analog	in	0	Analog channel 8
H2	IN[9]	Analog	Analog	in	0	Analog channel 9
H4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
H5	VSS_FE2	Analog	Power	in	0	Analog ground SS and output buffer
H7	VSS_AD	Analog	Power	in	0	ADC supply ground
H8	VSS_DG	Digital	Power	in	0	Digital ground
H9	VSS_DG	Digital	Power	in	0	Digital ground
H10	VSS_DG	Digital	Power	in	0	Digital ground
H11	VSS	Analog/Digital	Power	in	0	PADRING ground
H12	VSS_DG	Digital	Power	in	0	Digital ground
H13	VSS	Analog/Digital	Power	in	0	PADRING ground
H14	VSS	Analog/Digital	Power	in	0	PADRING ground
H15	VSS	Analog/Digital	Power	in	0	PADRING ground
H16	VDD_DG	Digital	Power	in	0	Digital core voltage
H18	VSS_DG	Digital	Power	in	0	Digital ground
H19	VSS_DG	Digital	Power	in	0	Digital ground
H21	serialOut-[3]	Digital	SLVS	out	160MHz	Serial data link 3 n
H22	serialOut+[3]	Digital	SLVS	out	160MHz	Serial data link 3 p

Table 26: Pinout part 4

Ball	Netname	Domain	IO type	Direction	Speed	Description
J1	IN[10]	Analog	Analog	in	0	Analog channel 10
J2	IN[11]	Analog	Analog	in	0	Analog channel 11
J4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
J5	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
J7	VSS_AD	Analog	Power	in	0	ADC supply ground
J8	VSS_DG	Digital	Power	in	0	Digital ground
J9	VSS_DG	Digital	Power	in	0	Digital ground
J10	VSS_DG	Digital	Power	in	0	Digital ground
J11	VSS_DG	Digital	Power	in	0	Digital ground
J12	VSS_DG	Digital	Power	in	0	Digital ground
J13	VSS_DG	Digital	Power	in	0	Digital ground
J14	VSS_DG	Digital	Power	in	0	Digital ground
J15	VSS_DR	Digital	Power	in	0	Digital SLVS drivers ground
J16	VDD_DR	Digital	Power	in	0	Digital SLVS drivers voltage
J18	serialOut-[4]	Digital	SLVS	out	160MHz	Serial data link 4 n
J19	serialOut+[4]	Digital	SLVS	out	160MHz	Serial data link 4 p
J21	VSS_DG	Digital	Power	in	0	Digital ground
J22	VSS_DG	Digital	Power	in	0	Digital ground
K1	IN[12]	Analog	Analog	in	0	Analog channel 12
K2	IN[13]	Analog	Analog	in	0	Analog channel 13
K4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
K5	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
K7	VSS_AD	Analog	Power	in	0	ADC supply ground
K8	VSS_DG	Digital	Power	in	0	Digital ground
K9	VSS_DG	Digital	Power	in	0	Digital ground
K10	VSS_DG	Digital	Power	in	0	Digital ground
K11	VSS	Analog/Digital	Power	in	0	PADRING ground
K12	VSS_DG	Digital	Power	in	0	Digital ground
K13	VSS	Analog/Digital	Power	in	0	PADRING ground
K14	VSS_DR	Digital	Power	in	0	Digital SLVS drivers ground
K15	VSS_DG	Digital	Power	in	0	Digital ground
K16	VDD_DG	Digital	Power	in	0	Digital core voltage
K18	VSS_DG	Digital	Power	in	0	Digital ground
K19	VSS_DG	Digital	Power	in	0	Digital ground
K21	serialOut-[2]	Digital	SLVS	out	160MHz	Serial data link 2 n
K22	serialOut+[2]	Digital	SLVS	out	160MHz	Serial data link 2 p
L1	IN[14]	Analog	Analog	in	0	Analog channel 14
L2	IN[15]	Analog	Analog	in	0	Analog channel 15
L4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
L5	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
L7	VSS_AD	Analog	Power	in	0	ADC supply ground
L8	VSS_DG	Digital	Power	in	0	Digital ground
L9	VSS_DG	Digital	Power	in	0	Digital ground
L10	VSS_DG	Digital	Power	in	0	Digital ground

Table 27: Pinout part 5

Ball	Netname	Domain	IO type	Direction	Speed	Description
M1	IN[16]	Analog	Analog	in	0	Analog channel 16
M2	IN[17]	Analog	Analog	in	0	Analog channel 17
M4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
M5	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
M7	VSS_AD	Analog	Power	in	0	ADC supply ground
M8	VSS_DG	Digital	Power	in	0	Digital ground
M9	VSS_DG	Digital	Power	in	0	Digital ground
M10	VSS_DG	Digital	Power	in	0	Digital ground
M11	VSS_DG	Digital	Power	in	0	Digital ground
M12	VSS_DG	Digital	Power	in	0	Digital ground
M13	VSS_DG	Digital	Power	in	0	Digital ground
M14	VSS_DR	Digital	Power	in	0	Digital SLVS drivers ground
M15	VSS_DG	Digital	Power	in	0	Digital ground
M16	VDD_DG	Digital	Power	in	0	Digital core voltage
M18	VSS_DG	Digital	Power	in	0	Digital ground
M19	VSS_DG	Digital	Power	in	0	Digital ground
M21	serialOut-[1]	Digital	SLVS	out	160MHz	Serial data link 1 n
M22	serialOut+[1]	Digital	SLVS	out	160MHz	Serial data link 1 p
N1	IN[18]	Analog	Analog	in	0	Analog channel 18
N2	IN[19]	Analog	Analog	in	0	Analog channel 19
N4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
N5	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
N7	VSS_AD	Analog	Power	in	0	ADC supply ground
N8	VSS_DG	Digital	Power	in	0	Digital ground
N9	VSS_DG	Digital	Power	in	0	Digital ground
N10	VSS_DG	Digital	Power	in	0	Digital ground
N11	VSS	Analog/Digital	Power	in	0	PADRING ground
N12	VSS_DG	Digital	Power	in	0	Digital ground
N13	VSS	Analog/Digital	Power	in	0	PADRING ground
N14	VSS_DG	Digital	Power	in	0	Digital ground
N15	VSS_DR	Digital	Power	in	0	Digital SLVS drivers ground
N16	VDD_DG	Digital	Power	in	0	Digital core voltage
N18	clkSOin-	Digital	SLVS	in	320MHz	Serial out clock n
N19	clkSOin+	Digital	SLVS	in	320MHz	Serial out clock p
N21	VSS_DG	Digital	Power	in	0	Digital ground
N22	VSS_DG	Digital	Power	in	0	Digital ground

Table 28: Pinout part 6

Ball	Netname	Domain	IO type	Direction	Speed	Description
P1	IN[20]	Analog	Analog	in	0	Analog channel 20
P2	IN[21]	Analog	Analog	in	0	Analog channel 21
P4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
P5	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
P7	VSS_AD	Analog	Power	in	0	ADC supply ground
P8	VSS_DG	Digital	Power	in	0	Digital ground
P9	VSS_DG	Digital	Power	in	0	Digital ground
P10	VSS_DG	Digital	Power	in	0	Digital ground
P11	VSS_DG	Digital	Power	in	0	Digital ground
P12	VSS_DG	Digital	Power	in	0	Digital ground
P13	VSS_DG	Digital	Power	in	0	Digital ground
P14	VSS_DG	Digital	Power	in	0	Digital ground
P15	VSS_DG	Digital	Power	in	0	Digital ground
P16	VDD_DR	Digital	Power	in	0	Digital SLVS drivers voltage
P18	VSS_DG	Digital	Power	in	0	Digital ground
P19	VSS_DG	Digital	Power	in	0	Digital ground
P21	Hrstb-	Digital	SLVS	in	160MHz	Reset n
P22	Hrstb+	Digital	SLVS	in	160MHz	Reset p
R1	IN[22]	Analog	Analog	in	0	Analog channel 22
R2	IN[23]	Analog	Analog	in	0	Analog channel 23
R4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
R5	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
R7	VSS_AD	Analog	Power	in	0	ADC supply ground
R8	VSS_DG	Digital	Power	in	0	Digital ground
R9	VSS_DG	Digital	Power	in	0	Digital ground
R10	VSS_DG	Digital	Power	in	0	Digital ground
R11	VSS	Analog/Digital	Power	in	0	PADRING ground
R12	VSS_DG	Digital	Power	in	0	Digital ground
R13	VSS	Analog/Digital	Power	in	0	PADRING ground
R14	VSS	Analog/Digital	Power	in	0	PADRING ground
R15	VSS	Analog/Digital	Power	in	0	PADRING ground
R16	VDD_DG	Digital	Power	in	0	Digital core voltage
R18	clkBXin-	Digital	SLVS	in	40MHz	Bunchcrossing clock n
R19	clkBXin+	Digital	SLVS	in	40MHz	Bunchcrossing clock p
R21	VSS_DG	Digital	Power	in	0	Digital ground
R22	VSS_DG	Digital	Power	in	0	Digital ground

Table 29: Pinout part 7

Ball	Netname	Domain	IO type	Direction	Speed	Description
T1	IN[24]	Analog	Analog	in	0	Analog channel 24
T2	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
T4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
T5	VSS_FE2	Analog	Power	in	0	Analog ground SS and output buffer
T7	VSS_AD	Analog	Power	in	0	ADC supply ground
T8	VSS_DG	Digital	Power	in	0	Digital ground
T9	VSS_DG	Digital	Power	in	0	Digital ground
T10	VSS_DG	Digital	Power	in	0	Digital ground
T11	VSS_DG	Digital	Power	in	0	Digital ground
T12	VSS_DG	Digital	Power	in	0	Digital ground
T13	VSS_DG	Digital	Power	in	0	Digital ground
T14	VSS_DR	Digital	Power	in	0	Digital SLVS drivers ground
T15	VSS_DG	Digital	Power	in	0	Digital ground
T16	VDD_DG	Digital	Power	in	0	Digital core voltage
T18	VSS_DG	Digital	Power	in	0	Digital ground
T19	VSS_DG	Digital	Power	in	0	Digital ground
T21	trg-	Digital	SLVS	in	160MHz	Event trigger n
T22	trg+	Digital	SLVS	in	160MHz	Event trigger p
U1	IN[25]	Analog	Analog	in	0	Analog channel 25
U2	N/C	-	-	-	-	Not connected
U4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
U5	VSS_FE2	Analog	Power	in	0	Analog ground SS and output buffer
U18	clkADCin-	Digital	SLVS	in	20MHz	ADC clock n
U19	clkADCin+	Digital	SLVS	in	20MHz	ADC clock p
U21	VSS_DG	Digital	Power	in	0	Digital ground
U22	VSS_DG	Digital	Power	in	0	Digital ground
V1	IN[26]	Analog	Analog	in	0	Analog channel 26
V2	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
V4	VDD_FE	Analog	Power	in	0	Analog core voltage FS and CSA
V5	VSS	Analog/Digital	Power	in	0	PADRING ground
V6	VSS_AD	Analog	Power	in	0	ADC supply ground
V7	VDD_AD	Analog	Power	in	0	ADC supply voltage
V8	VDD_AD	Analog	Power	in	0	ADC supply voltage
V9	VDD_AD	Analog	Power	in	0	ADC supply voltage
V10	VDD_DG	Digital	Power	in	0	Digital core voltage
V11	VDD_DG	Digital	Power	in	0	Digital core voltage
V12	VDD_DG	Digital	Power	in	0	Digital core voltage
V13	VDD_DG	Digital	Power	in	0	Digital core voltage
V14	VDD_DG	Digital	Power	in	0	Digital core voltage
V15	VDD_DR	Digital	Power	in	0	Digital SLVS drivers voltage
V16	VDD_DR	Digital	Power	in	0	Digital SLVS drivers voltage
V17	VDD_DG	Digital	Power	in	0	Digital core voltage
V18	VSS_DG	Digital	Power	in	0	Digital ground
V19	VSS_DG	Digital	Power	in	0	Digital ground
V21	hb_trg-	Digital	SLVS	in	160MHz	Heartbeat trigger n
V22	hb_trg+	Digital	SLVS	in	160MHz	Heartbeat trigger p

Table 30: Pinout part 8

Ball	Netname	Domain	IO type	Direction	Speed	Description
W1	IN[27]	Analog	Analog	in	0	Analog channel 27
W2	N/C	-	-	-	-	Not connected
W4	VSS	Analog/Digital	Power	in	0	PADRING ground
W5	VSS_AD	Analog	Power	in	0	ADC supply ground
W6	VSS_AD	Analog	Power	in	0	ADC supply ground
W7	VDD_AD	Analog	Power	in	0	ADC supply voltage
W8	VDD_AD	Analog	Power	in	0	ADC supply voltage
W9	VDD_AD	Analog	Power	in	0	ADC supply voltage
W10	VDD_DG	Digital	Power	in	0	Digital core voltage
W11	VDD_DG	Digital	Power	in	0	Digital core voltage
W12	VDD_DG	Digital	Power	in	0	Digital core voltage
W13	VDD_DG	Digital	Power	in	0	Digital core voltage
W14	VDD_DG	Digital	Power	in	0	Digital core voltage
W15	VDD_DG	Digital	Power	in	0	Digital core voltage
W16	VDD_DG	Digital	Power	in	0	Digital core voltage
W17	VDD_DG	Digital	Power	in	0	Digital core voltage
W18	bx_sync_trg-	Digital	SLVS	in	160MHz	Bunchcrossing counter sync n
W19	bx_sync_trg+	Digital	SLVS	in	160MHz	Bunchcrossing counter sync p
W21	VSS_DG	Digital	Power	in	0	Digital ground
W22	VSS_DG	Digital	Power	in	0	Digital ground
Y1	IN[28]	Analog	Analog	in	0	Analog channel 28
Y2	VSS_FE	Analog	Power	in	0	Analog ground FS and CSA
Y21	sdo1-	Digital	SLVS	out	160MHz	Scanchain test Scan Out SLVS
Y22	sdo1+	Digital	SLVS	out	160MHz	Scanchain test Scan Out SLVS
AA1	IN[29]	Analog	Analog	in	0	Analog channel 29
AA2	N/C	-	-	-	-	Not connected
AA3	CTS	Analog	Static	in	Static	Shaping configuration
AA4	CG<0>	Analog	Static	in	Static	Gain configuration
AA5	VDD_FE2	Analog	Power	in	0	Analog core voltage SS and output buffer
AA6	VDD_FE2	Analog	Power	in	0	Analog core voltage SS and output buffer
AA7	VDD_FE2	Analog	Power	in	0	Analog core voltage SS and output buffer
AA8	VREFP	Analog	Power	in	0	Voltage reference p
AA9	VREFP	Analog	Power	in	0	Voltage reference p
AA10	hadd[2]	Digital	Static	in	Static	Chip address
AA11	hadd[0]	Digital	Static	in	Static	Chip address
AA12	sme	Digital	CMOS	in	Static	MEM Test En
AA13	sdi3	Digital	CMOS	in	20MHz	Scanchain test Scan In
AA14	sen1	Digital	CMOS	in	20MHz	Scanchain test Scan Enable
AA15	smo	Digital	CMOS	out	20MHz	MEM Test Out
AA16	TRST	Digital	CMOS	in	20MHz	JTAG
AA17	TDI	Digital	CMOS	in	20MHz	JTAG
AA18	TDO	Digital	CMOS	out	20MHz	JTAG
AA19	N/C	-	-	-	-	Not connected
AA20	sdo3-	Digital	SLVS	out	160MHz	Scanchain test Scan Out SLVS
AA21	N/C	-	-	-	-	Not connected
AA22	VSS_DG	Digital	Power	in	0	Digital ground

Table 31: Pinout part 9

Ball	Netname	Domain	IO type	Direction	Speed	Description
AB1	IN[30]	Analog	Analog	in	0	Analog channel 30
AB2	IN[31]	Analog	Analog	in	0	Analog channel 31
AB3	N/C	-	-	-	-	Not connected
AB4	CG<1>	Analog	Static	in	Static	Gain configuration
AB5	N/C	-	-	-	-	Not connected
AB6	POL	Analog	Static	in	Static	Polarity configuration
AB7	VREFP	Analog	Power	in	0	Voltage reference p
AB8	VREFP	Analog	Power	in	0	Voltage reference p
AB9	VREFP	Analog	Power	in	0	Voltage reference p
AB10	hadd[3]	Digital	Static	in	Static	Chip address
AB11	hadd[1]	Digital	Static	in	Static	Chip address
AB12	sen3	Digital	CMOS	in	20MHz	Scanchain test Scan Enable
AB13	sdi1	Digital	CMOS	in	20MHz	Scanchain test Scan In
AB14	PORin	Digital	CMOS	in	Static	Power on reset input
AB15	PORout	Digital	CMOS	out	Static	Power on reset output
AB16	TMS	Digital	CMOS	in	20MHz	JTAG
AB17	TCLK	Digital	CMOS	in	20MHz	JTAG
AB18	N/C	-	-	-	-	Not connected
AB19	VSS_DG	Digital	Power	in	0	Digital ground
AB20	sdo3+	Digital	SLVS	out	160MHz	Scanchain test Scan Out SLVS
AB21	N/C	-	-	-	-	Not connected
AB22	N/C	-	-	-	-	Not connected

A.5. Application Notes

A.5.1. Power-on Recommendations

The recommended power-up procedure for SAMPA V4 chip is to first ramp up the power supply voltage, then wait approximately 50 ms for the PoR (Power-on Reset) flag, and only after the PoR flag the system clock should be applied to the IC.

The Power-on Reset flag is available through the open-drain output pin AB15.

If the user chooses to use the internal recommended PoR flag, package pins AB15 (PORout) and AB14 (PORin) should be externally connected, as shown in figure 21. In case the user prefers to use an external PoR flag, it should be connected to pin AB14. Take note that pin AB14 is a CMOS active LOW level input signal with internal pull-up. Regarding the use of an external PoR flag, a time delay of at least 40ms must be waited after the power supply power-up.

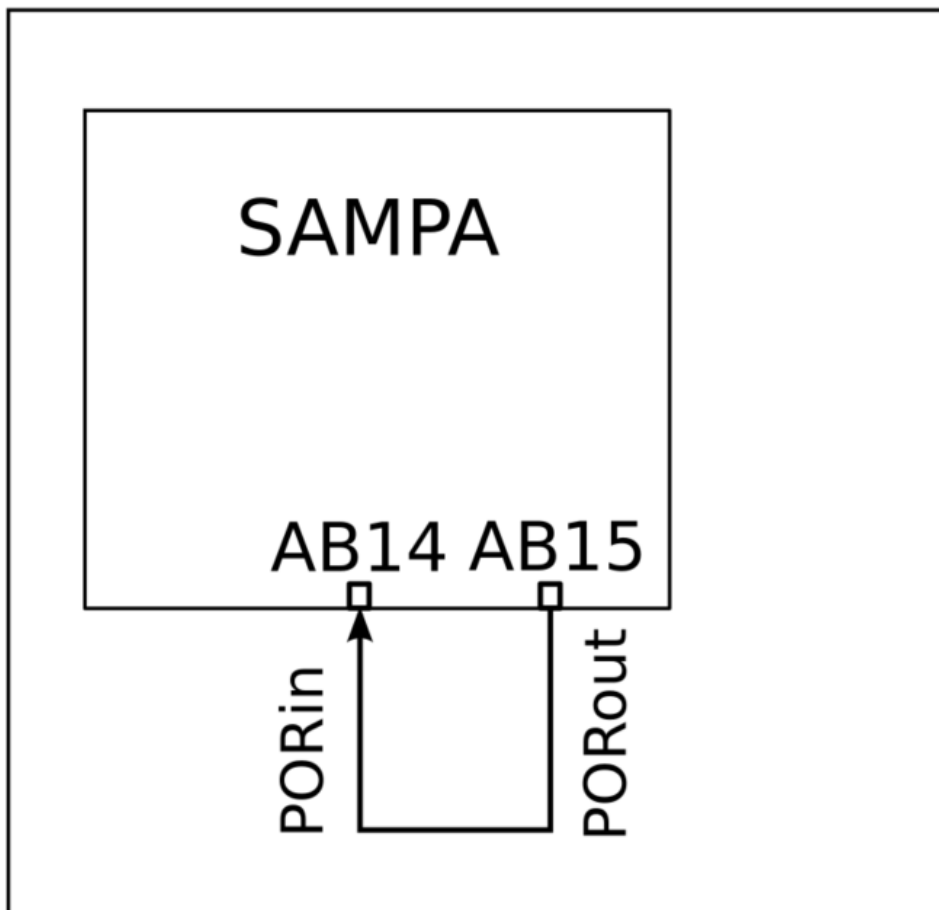


Figure 21: SAMPA PORin to PORout connection.

If the system clock is fed into the SAMPA V4 ASIC before the Power on Reset, the system may start to operate in an irreversible incorrect state. In order to avoid such behavior, the system clock should only be enabled to the chip after the PoR flag.

The ideal power-on timing diagram is shown in figure 22. It represents the power supply ramp up occurring first, the PoR flag occurring after approximately 50 ms, and after this, the system clock may start.

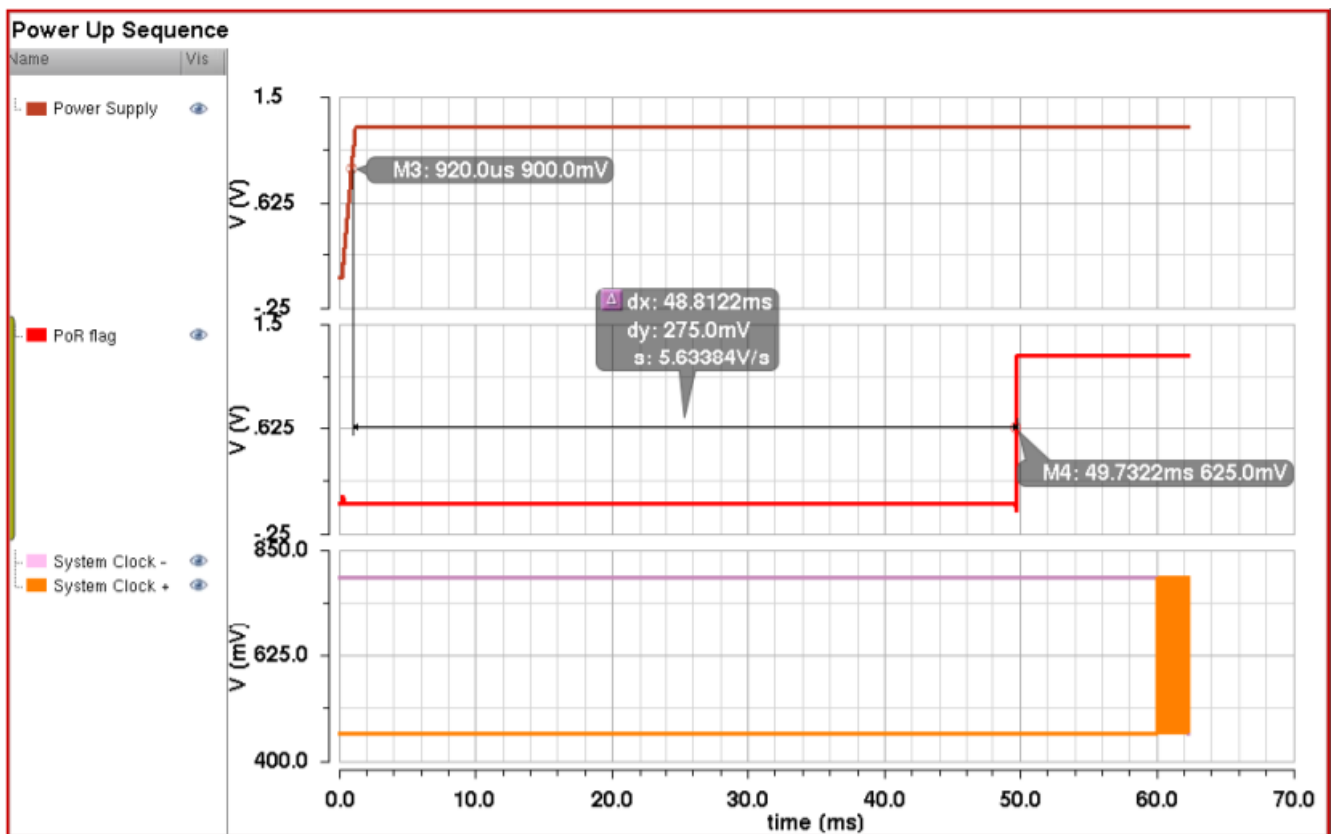


Figure 22: Ideal SAMPA V4 ASIC Power Up Sequence.