LEONARDO AMORESE GALLO GOMES

Design of phase shifters in nanowire membrane technology and VCOs in CMOS technology at millimeter-waves for future full front-end integration

São Paulo / Grenoble

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RESUMO

Esta tese de doutorado está inserida no complexo contexto de telecomunicações em ondas milimétricas, abordando dois elementos importantíssimos de um transceptor nesta faixa de frequências: defasadores e osciladores controlados por tensão.

Os defasadores projetados neste trabalho são baseados na plataforma tecnológica da membrana de nanofios metálicos (MnM, acrônimo em inglês), utilizando linhas de onda-lenta suspensas e cristal líquido. As linhas suspensas têm a principal vantagem de apresentarem perdas de transmissão reduzidas devido às baixas oferecidas pelo ar, mantendo a redução de comprimento devido ao efeito de onda lenta. A adição de cristal líquido às linhas suspensas faz intensificar o efeito de onda lenta e permite o controle da velocidade de fase da linha. Este acréscimo tem como efeito adicional baixar a tensão de *pull-in* da linha suspensa, que pode funcionar como um defasador MEMS. O chaveamento eletrostático da linha causa uma variação importante na velocidade de fase. O resultado são defasadores compactos e com alta figura de mérito. Os valores de figura de mérito em 60 GHz são de 43.8 °/dB para a defasagem gerada apenas por cristal líquido e de 108 °/dB para a combinação do cristal líquido com o chaveamento eletrostático MEMS. Estes resultados mostram o forte potencial desta topologia para aplicações em ondas milimétricas.

Os osciladores controlados por tensão foram projetados numa tecnologia BiCMOS otimizada para aplicações em altas frequências, a BiCMOS 55-nm desenvolvida pela *ST Microelectronics*. Esta tecnologia disponibiliza dispositivos de alto desempenho, assim como um conjunto de camadas metálicas de baixas perdas em altas frequências. Os osciladores utilizam um circuito tanque inovador baseado em um ressoador de toco de quarto de comprimento de onda baseado em linhas coplanares de onda-lenta (S-CPS) carregadas periodicamente com varactores MOS. Foi desenvolvida a geometria do circuito tanque objetivando maximizar o controle do varactor na velocidade de fase da linha, assim como um procedimento de projeto que permite se determinar o melhor ressoador dado um conjunto de parâmetros de projeto. Além disto, foram explorados outros elementos ligados ao ressoador S-CPS: o primeiro é um estudo da configuração

da célula de compensação de perdas do circuito tanque; a segunda é a tomada de potência diretamente do tanque, sem a necessidade de amplificador *buffer* entre o tanque e a carga; terceiro e último, o emprego de chaves eletrônicas para se controlar um transformador sintonizável baseado em linhas S-CPS. Os osciladores projetados, centrados em 80 GHz, apresentam faixa de excursão de frequência superiores a 10 %, com figura de mérito melhor do que -170 dB, tendo sido projetado um oscilador com banda de oscilação de quase 20 GHz, cobrindo a banda-E completamente e continuamente. Estes resultados demonstram que o ressoador S-CPS é uma topologia muito poderosa, inovadora e flexível que permite o projeto de osciladores compactos e de alto desempenho para aplicações em ondas milimétricas.

Palavras-chave: CMOS, ondas milimétricas, microeletrônica, circuitos integrados, oscilador, defasador, interposer, linha de onda lenta, óxido de alumina anódica (AAO), telecomunicações.

RÉSUMÉ

Cette thèse de doctorat concerne le domaine des circuits et systèmes de communication en bande millimétrique, avec un focus sur deux éléments importants d'un transceiver, à savoir les déphaseurs et les oscillateurs commandés en tension (VCOs).

La première partie de la thèse concerne la conception, la réalisation et la caractérisation de déphaseurs. Une technologie de type membrane à nanofils métalliques a été utilisée pour les déphaseurs, utilisant à la fois des lignes suspendues de type MEMS et des cristaux liquides comme éléments d'accord. Les lignes suspendues possèdent l'intérêt de conduire à des pertes d'insertion faibles du fait que le diélectrique est l'air. Elles sont miniaturisées grâce à un effet d'onde lente obtenu par l'utilisation d'un lit de nanofils métalliques verticaux sous le ruban d'une ligne microruban. L'insertion des cristaux liquides sous le ruban suspendu permet de contrôler la constante diélectrique effective de la ligne, et donc le déphasage engendré. Cela accentue également l'effet d'onde lente du fait de la constante diélectrique des cristaux liquides, mais en contrepartie bien sûr conduit à une augmentation des pertes diélectriques

Cela conduit également à un effet très positif en abaissant la tension de « pull-in » de l'aspect MEMS.

Le cumul des deux effets (cristaux liquides et MEMS) a permis de démontrer des déphaseurs compacts et performants. La figure de mérite obtenue atteint ainsi 43.8 °/dB avec un contrôle uniquement basé sur la polarisation des cristaux liquides, et 108 °/dB lorsque les deux effets sont combinés. Ces résultats à l'état de l'art montrent le potentiel élevé de la technique utilisée pour la réalisation de déphaseurs en bande millimétrique.

La seconde partie de la thèse concerne la conception, la réalisation et la caractérisation de VCOs, en technologie BiCMOS 55 nm de STMicroelectronics.

Cette technologie propose des actifs hautes performances au sein du Front-End-Of-Line ainsi qu'un Back-End-Of-Line très performant pour la conception des passifs. Les VCOs étudiés au sein du la thèse utilisent des résonateurs innovants basés sur des lignes de type CPS (« Coplanar Stripline ») à ondes lentes, chargées périodiquement par des varactors de type AMOS

(« Accumulation MOS »). Plusieurs générations de VCOs ont été réalisées.

La première réalisation a concerné le développement d'une topologie de résonateur permettant de maximiser la variation de phase des résonateurs à travers le contrôle de la capacité des varactors, grâce à une procédure de design permettant une optimisation automatique à partir d'un jeu de paramètres de design.

Par la suite, d'autres innovations ont été apportées à cette première réalisation :

- Une étude permettant d'optimiser la configuration du circuit de compensation des pertes,
- Une topologie sans buffer, permettant de réduire de manière drastique la consommation,
- L'utilisation de switchs permettant de commuter deux résonateurs afin d'élargir la bande d'accord des VCOs.

Toutes les générations de VCOs ont été conçues en bande E autour de 80 GHz, avec un objectif d'accord en fréquence au minimum de 10%. La figure de mérite de l'ensemble des générations est meilleure que -170 dB.

La dernière génération basée sur des résonnateurs commutés permet d'envisager un accord de l'ordre de 20% permettant de couvrir la totalité de la bande E.

L'ensemble des résultats obtenus montre ainsi que l'approche utilisant des résonateurs basés sur des lignes à ondes lentes de type CPS offre un fort potentiel, que ce soit en termes de performances ou de flexibilité de design permettant d'obtenir des résonateurs très compacts en bande millimétrique. Remarquons que cela peut paraître paradoxal de vouloir fournir des efforts en termes de miniaturisation en bande E où la longueur des lignes devient modérée, mais ce serait oublier le coût des technologies qui croît de manière exponentielle avec la performance des actifs et des passifs, nécessitant ainsi des efforts importants en termes de miniaturisation.

Mots clés : Technologie CMOS, technologie membranes à nanofils, ondes millimétriques, microélectronique, oscillateurs, déphaseurs, lignes à ondes lentes, télécommunications.

ABSTRACT

This doctoral thesis is inserted into the complex context of millimeter-wave telecommunications, dealing with two very important elements in a transceiver for such frequencies: phase shifters and voltage-controlled oscillators.

The phase shifters designed in this work are based on the metallic nanowire membrane technology platform (MnM), using suspended, slow-wave lines and liquid crystal. The suspended lines have the main advantage of showing low transmission losses, thanks to the absence of losses of air, keeping the length reduction thanks to the slow-wave effect. The insertion of liquid crystal to the suspended lines intensifies the slow-wave effect and allows the phase velocity controls of the line. Also, it lowers the pull-in voltage of the line, allowing it to work as a MEMS phase-shifter. This electrostatic switching causes a significative decrease of phase velocity, resulting in compact and high-performance phase shifters. The values for the figure of merit are 43.8 °/dB for a pure liquid crystal phase shifter and 108 °/dB for a phase-shifter that combines the phase shift generated by the liquid crystal and MEMS switching. These results show the strong potential of this topology for millimeter wave applications.

The voltage-controlled oscillators were designed in a RF-oriented BiCMOS technology, the 55-nm BiCMOS technology developed by ST Microelectronics. This technology offers high-performance devices and a low-loss back-end. The oscillators use a novel tank circuit based in quarter-wavelength stubs based in slow-wave coplanar striplines (S-CPS) periodically loaded by MOS varactors. The design started with the development of a resonator topology that maximizes varactor control over the phase velocity of the line, as well as a design procedure that enables the determination of the best possible resonator, given a set of design parameters. Also, some other elements of the oscillator were explored: first, the study of the tank loss compensation configuration; second, a bufferless topology, where the output power is derived directly from the tank circuit; third and last, the use of electronic switches to control a tunable transformer based on S-CPS. The oscillators were designed having a center frequency of 80 GHz and all have a frequency tuning range better than 10 %, while displaying a figure of merit better than -170 dB. One of the oscillators displayed a frequency tuning

range of almost 20 %, covering the E-band completely and continually. These results show that the varactor-loaded S-CPS resonator is an innovative oscillator topology that is very powerful and flexible, enabling the design of compact and high-performance oscillator of millimeter-wave applications.

Key words: CMOS, millimeter waves, microelectronics, integrated circuits, oscillator, phase shifter, interposer, slow-wave line, anodic aluminum oxide (AAO), telecommunications.

CONTENTS

1 INTRODUCTION

1.1 CONTEXT OF THIS THESIS

Human society has been evolving the way of transmitting knowledge and information ever since the invention of the written language. We, as a society, have come a long way since the first clay tablets have been written: in this rather long meantime we have invented the press, which printed standardized letters onto a paper sheet, greatly quickening the production of books; we have invented radio communications, which transmit information by means of electronically mixing an audio signal to a high-frequency carrier and propagate it on air; we have invented the internet, a medium of transmitting and accessing packets of digital data in a scale and breadth never ever dreamt before. We have received data from the far ends of the solar system, billions of kilometers away. We now have the means of knowing what goes on at the other side of the planet almost in real time. And, with our ever-increasing capability for communication and transmitting information and knowledge, the innate human drive for more keeps pushing the installed telecommunication facilities on, stressing the infrastructure and calling for innovative solutions for current problems and for new technologies and techniques for solving problems that are yet to come.

This need for higher bandwidth is clearly seen by looking at the different specifications for the cellular network generations since the first iteration, or 1G, from the 1980's. Cellular network then was in place to carry analog communications between users in range of a retransmitting antenna. Then, in the 1990's, 2G allowed the digital transmission of the voice signal, which increased call quality, and enabled simple data transfer capability to the users, like SMS messaging and, at the end of its life cycle, simple internet access. In the 2000's, 3G enabled users to access the internet and upload/download images and audio, with download speeds up to 10 Mbps. The 2010's saw the 4G, which high-speed internet connection and bandwidth, with download speeds up to 1 Gbps. This generation enabled the end-user to benefit from high-definition voice transmission, mobile TV, HD video streaming, gaming services, etc.

The ongoing Covid-19 pandemic, at the time of the writing of this manuscript, demanded lockdown and social isolation measures to be taken across the world, which drove the demand for internet connectivity higher than

never before [1], both on fixed and cellular networks. This, of course, added to the increasing tendency in data consumption. According to Figure 1, the volume of data consumed in both cellular and fixed networks almost quadrupled in the period between 2016 and 2021. Cellular network alone saw a jump from 86 petabytes to 335 petabytes in this period. The increasing number of users and the necessary bandwidth to accommodate them plus and to enable new functionalities, makes it necessary to move forward again.

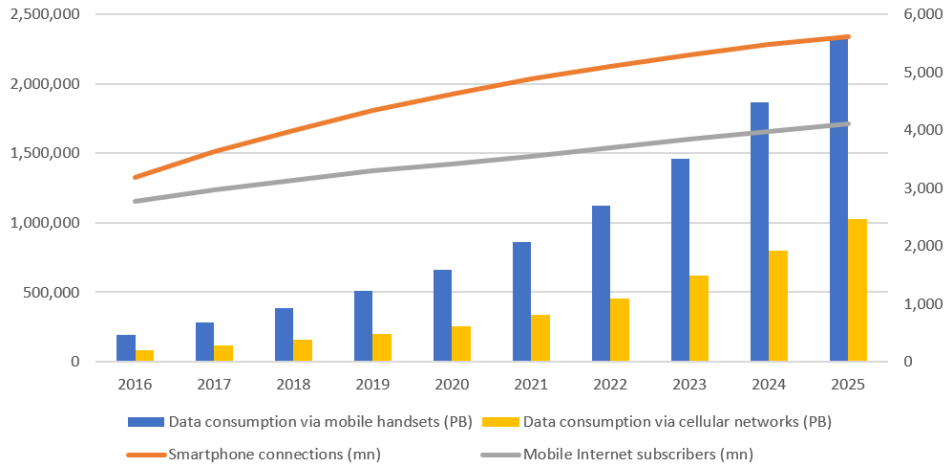


Figure 1 – Worldwide data consumption between 2016 and 2021 and trend for the near future, between 2022 and 2025. Source:[2]

The 5G is in the process of being adopted in various urban centers across the world, having reached the number of 1662 cities across 65 countries as of 2021 [3]. This fifth-generation cellular network is aimed for massive multiple input and multiple output (MIMO) networks with capabilities to enable gigabit download speeds, as much as 20 Gbps 5G will be able to accommodate end-user applications such as ultra-HD video streaming, real-time HD video calls, virtual reality, wearable wireless devices, etc. Also, the massive bandwidth is being aimed to accommodate the Internet of Things (IoT) devices that are expected to be deployed in the following years.

One of the new solutions and technologies being brought with the 5G standard are the wireless links using millimeter-waves (mmW), which comprises the frequency range from 30 GHz up to 300 GHz. By increasing the carrier frequency, the link is capable of providing more bandwidth to the end users, which solves the problem of accommodating more, data-hungry users. However, this gain in bandwidth comes at a price: mmW have more free-path losses, and are

more easily absorbed by walls and foliage, which calls for another change of perspective regarding the design of mmW links, which shifts from long-range, broadcasting links to smarter, shorter-range links. Example of mmW bands that have been allocated is: 24-30 GHz for 5G mm-wave links, the unlicensed 57-66 GHz (V-band) for high-speed, short-range links such as IEEE 802.11ad protocol, the 71-76 GHz, 81-86 GHz bands (E-band) for backhauling and 76-81 GHz for automotive radar, etc.

To compensate for the propagation losses, the transmission gain must be increased, and the most power-efficient way to do so is to employ antenna arrays to focus the radiated power. This, however, also comes with a price: the antenna array cannot illuminate a wide solid angle anymore, so the mmW beam needs to be steered to illuminate the end-users. One technique to do so is to employ a beam-steerable front-end: the antennas are fed by phase-shifters, and by carefully changing the phase on each antenna, the radiation direction can be changed.

A mmW beam-steering transceiver front-end is a complex system that needs to tackle a number of tasks: from amplification to signal generation, mixing and up/down conversion, signal switching and filtering and the electronic steering of the antenna array irradiation pattern. The basic block diagram for a beam-steering front-end is shown in Figure 2, where a 2-antenna, 60 GHz receiver RFIC implemented in 130-nm CMOS is depicted.

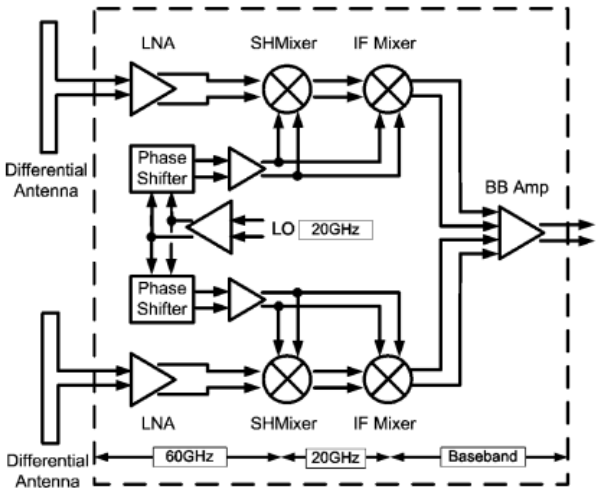


Figure 2 – Block diagram of a 2-antenna, monolithic beam-steering front-end at 60 GHz implemented in a 130 nm CMOS process. Here only the antennas and low-noise amplifiers are implemented in the carrier frequency, the sub-harmonic mixer, intermediate frequency mixer and local oscillator are implemented in the intermediate frequency, 20 GHz. Source: [4]

Here the basic building blocks can be seen: low noise amplifiers to amplify the incoming signal; phase-shifters to realize the beam-steering; power combiners; a local oscillator; and a base-band amplifier to boost the power level of the demodulated signal. It is straightforward to say that a transmitter would employ power amplifiers and power dividers instead. Other examples of such front-ends at 60 GHz and 26 GHz-28 GHz include [5] [6] [7] [8] [9].

The designer needs to choose the topology carefully. The front-end can all be done in the carrier frequency, reducing the die area as the lambda-based components, such as phase-shifters, power divider and interconnecting transmission lines, will be scaled down, but this will increase their insertion loss to a degree. Also, it would increase the burden on the active circuits, as the transistors will be invariably working close to their cutoff frequency, thus increasing the DC power consumption, reflecting the higher transconductance (g_m) needed to maintain the desired performance parameters. On another hand, some parts could be designed to work on the intermediate frequency, but that would increase the number of mixers in the circuit, as each branch would require a separate up/downconversion mixer, increasing the circuit complexity. Not considering whether the antennas would be implemented on chip, on the package or on the interconnection substrate, each posing their own benefits and shortcomings. Thus, there is not a simple, “one-size-fits-all” solution for designing a beam-steering, mmW front-end.

1.2 OBJECTIVE

This doctoral thesis is inserted in this high-frequency and high-complexity context. The goal of this work is to design two of the building blocks of a high-performance, mmW beam-steering front-end: a voltage-controller oscillator (VCO) at 80 GHz and a phase shifter at 60 GHz.

The reason to have chosen these two very different blocks is the nature of the design and the importance of these blocks. Even though an oscillator and a variable transmission line are two very dissimilar devices, they both employ the same concept at their core: they are electrically-tunable devices which employ some kind of variable capacitance to achieve their goal, either generating different output frequencies or having different conduction phase. VCOs are one of the most important building blocks in a transceiver, either in the generation of

the carrier frequency, LO frequency or clock in phase-locked loop systems. Phase-shifters are the parts that will create the electric phase shift that will steer the antenna array beam, thus they are one of the core devices of a mmW beam-steering front-end.

The phase-shifters will be realized using the Metallic-nanowire-Membrane (MnM) technology platform, for their high-performing passive devices, developed at the *Laboratório de Microeletrônica da Universidade de São Paulo* (LME-USP). The VCO will be designed in an advanced, RF-optimized BiCMOS technology developed by STMicrolectronics. Both designs will be made around slow-wave transmission lines for their compactness and improved electrical performance over traditional microstrip lines.

This doctoral thesis marches toward the design of a mmW front-end with beam-steering capabilities. This front-end would utilize the MnM technology platform to realize the RFIC integration and off-chip passive devices, because of its reported high-performance devices and low fabrication cost. The RFICs would be designed using (Bi)CMOS processes, since they enable well-performing circuits at a competitive cost when compared to III-V processes. Figure 3shows a cross-section of such a mmW front-end, showing several devices and integration techniques that are either already developed (such as the nanowire vias and the LCP-MnM antenna) or in development as part of the research work of other colleagues.

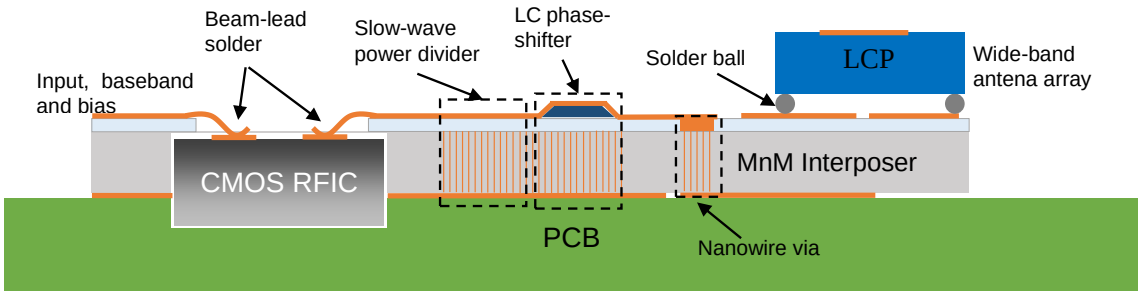


Figure 3 - Cross-section of a MnM-based mmW front-end, showing several devices and integration techniques to realize it. Source: author.

1.3 BIBLIOGRAPHICAL ANALYSIS AND STATE OF THE ART

This section will present a brief state-of-the-art on mmW phase-shifters and CMOS-based VCOs.

1.3.1 PHASE-SHIFTERS

Phase shifters can be classified in two categories: active and passive phase-shifters. Active phase shifters consume power and suffer from some non-linearities [10,11], leading to complex thermal dissipation mechanisms for systems with large antenna array. Hence, they are not envisioned in this project.

Several technologies have been used to develop passive phase shifters at mmW, including CMOS/BiCMOS, BST, Liquid Crystal and MEMS. A brief state-of-the-art shows that the phase shifters demonstrated so far either exhibit unacceptable insertion loss, or occupy large surfaces.

A careful comparison of phase shifters realized in all these technologies is not simple, since one has to consider not only the size and the electrical performance, but also the cost, the reliability, and, especially for MEMS, the packaging issue. Here, the phase shifters are only compared in terms of size and electrical performance. The classical Figure of Merit (FOM) is used, defined by the ratio of the maximum phase shift over the maximum insertion loss.

Contrary to MEMS phase shifters, their CMOS/BiCMOS counterparts offer much smaller footprint (0.075 mm² [12] and 0.034 mm² [13]) in a Reflection-Type Phase Shifters (RTPS), but their electrical performance is poor (11°/dB [12] and 13°/dB [13]) since MOS varactors used as tuning elements exhibit Q-factors limited to about 10 at mmW [14]. However, the reduced area yields a high FOM /Area ratio (146°/(dB·mm²) [12] and 382°/(dB·mm²) [13]).

In general, BST-based devices show good electrical performance at RF frequencies, however, the BST loss tangent increases dramatically with frequency, which limits its electrical performance at mmW. For example, [15] reports a FOM of 23°/dB with a footprint of 1.2 mm² at 60 GHz.

Liquid crystal-based phase shifters can show a high FOM at higher frequencies, since LC loss tangent decreases with frequency [16]. A FOM of 42°/dB at 76 GHz was reported in [17]. However, due to the moderate variation of the dielectric constant of the LC, the area of LC phase shifters is usually large, 0.65 mm² in this case. In [18], a slow-wave CPW (S-CPW) was combined with MEMS and LC to take advantage of their high FOM, while reducing the size and response time of the phase shifter. A FOM of 52°/dB at 45 GHz with a 0.38 mm² footprint was obtained. In [19], a continuously tunable phase shifter using a LC-

filled stripline realized on LTCC was demonstrated. The total area occupied by the stripline and LC is 14.6 mm^2, leading to a FOM greater than 47°/dB between 30 GHz and 34 GHz.

Another type of passive phase shifter is being developed by USP-LME and TU-Darmstadt, Germany in the framework of the DFG project “Novel continuously tunable and miniaturized passive Slow-Wave Phase Shifters with fast response time for millimeter wave applications based on a combined Liquid Crystal (LC) and Nanowire-filled Membrane Technology” in order to develop a liquid crystal-based phase shifter on the MnM. This novel phase shifter uses the MnM slow-wave microstrip line, enabling area reduction and, because it is fabricated directly on the MnM substrate, ease of integration with the rest of the beam-steering front-end. [20]

1.3.2 CMOS VOLTAGE-CONTROLLED OSCILLATORS AT E-BAND

An electronic oscillator can be simplified down to an inductor-capacitor resonant circuit fed back by an inverting amplifier. The resonator has a self-oscillating frequency, at which its equivalent impedance will be purely real and equal to its equivalent losses, caused by ohmic losses in the conductors, dielectric losses due to the periodic repolarization of electrical dipoles in the capacitor’s dielectric, substrate losses due to eddy currents in the case of an integrated resonator, etc. These losses naturally cause power dissipation in the resonator, resulting in an exponentially-fading output – the resonator will ring, oscillate for a short time until the signal fades out. If the feedback amplifier can (over)compensate this dissipation, the ringing can be indefinitely sustained, and an oscillator is created. This is a rather extensive explanation of the Barkhausen criterion: oscillation in a closed-loop system will occur always when the closed-loop gain is equal to 1. If this gain is larger than 1 in magnitude, the system is unstable and its output would rise exponentially, thus a self-sustaining oscillator has to have some sort of gain limiting mechanism to prevent self-destruction or other undesired effects. In the case of the electronic oscillator there is an inherent self-limiting mechanism thanks to the strong non-linearity large signal behavior of a transistor: the voltage gain drops abruptly when the signal amplitude is closer to either power rail (i.e., to ground or to V_{DD}). This causes the average gain to remain stable, and the oscillations, self-sustained.

The feedback amplifier can be modelled as a negative resistance in parallel with the equivalent losses of the resonator, and its exact realization will depend on the design. One of the most popular topologies for the loss-compensation amplifier in CMOS technologies is the cross-coupled pair (CCP), which can be understood as two cascaded, tuned and fed-back common-source amplifiers.

A voltage-controlled oscillator (VCO) is an oscillator whose output frequency is controlled by an electric input. The frequency tuning mechanism is usually done with a variable capacitance, or varactor, which is a voltage-controlled capacitor. Thus, the most basic kind of VCO is based on a varactor-inductor tank [21]. For monolithic VCOs, the inductor is realized by a planar coil realized on the back-end of the chip and the varactor, either using a reverse-biased diode or a metal-oxide-semiconductor (MOS) capacitor. The inductor-varactor tank performs very well up until the upper limit of the microwave band, as the quality factor (Q-factor) of both the inductor and MOS varactor is well above 10 at frequencies below 10 GHz [22]. At mmW, however, the Q-factor of MOS varactor suffers a dramatic drop, dominated by the gate series resistance [23], and their low Q-factor dominates the Q-factor of the resonant tank. Inductors also do suffer from Q-factor drop, especially because of conductor ohmic losses and substrate losses. Nevertheless, improving the inductor Q-factor still improves the overall Q-factor of the Tank, but the mechanisms to improve the Q-factor have some particularities because of effects that happen at mmW: for example, the patterned ground shield, which is an efficient solution to shield the substrate from the eddy current losses at microwave frequencies, turns to be detrimental in mmW because of their own losses [24]. One proposed workaround is to realize the inductors as stubs of slow-wave coplanar waveguides (S-CPW), whose Q-factor can be higher than 30 at mmW [25]. However, even if a custom inductor displays better Q-factor than a standard, planar inductor, the Q-factor of the resonator is still dominated by the varactors.

The use of standing-wave resonators instead of lumped inductor-capacitor tanks was proposed to improve the Q-factor of the resonator [26]. This kind of oscillator is called a standing-wave oscillator (SWO). In this kind of oscillator, the resonant frequency happens at frequencies where the electrical length of the transmission line equals odd multiples of $\lambda/2$ for open-circuit-terminated stubs [27] [28] or odd multiples of $\lambda/4$ for short-circuit-terminated stubs, with the

possibility of multi-mode, or multi-band oscillation by loading the stub to force a degenerate resonant mode [27] [29]. However, the main bottleneck still remains the low Q-factor of monolithic varactors. To avoid use of varactors inside the resonator, [30] proposes the use of digitally-controlled transmission lines acting as switched capacitors. The Q-factor is indeed improved thanks to a high-quality differential transmission line, but the frequency tuning is not continuous, which can be a limiting factor in some applications.

1.3.2.1 VCO Figures of Merit

The importance of a high-Q resonator is that the phase noise of an oscillator is inversely proportional to the Q-factor of its tank. Random noise in an oscillator loop will cause two types of perturbations in the output signal: amplitude noise, which is random fluctuation on the signal amplitude, and phase noise, random shifts in the signal phase. The feedback loop of an oscillator rejects amplitude noise, but there is no compensation mechanism for phase noise. The phase-noise can be expressed as shown by Leeson's phase noise equation:

$$L(\Delta\omega) = 10\log_{10}\left[\frac{2kT}{P_{sig}}\cdot\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \quad (1)$$

where $L(\Delta\omega)$ is the phase noise at a $\Delta\omega$ offset from the fundamental, T is the absolute temperature, k is the Boltzmann constant, P_{sig} is the signal power available at the feedback amplifier's input, ω_0 is the oscillating frequency, and Q is the loaded Q-factor of the resonator. This equation helps offer insight into the phenomena that contribute to phase noise, rather than offering an accurate value for it. Phase noise is inversely proportional to P_{sig} and to Q. Thus, to reduce the phase noise, either the tank Q-factor or the P_{sig} need to be increased. Increasing P_{sig} will result in an increase in DC power consumption, which isn't always desirable. However, increasing the tank Q-factor will also have the effect of reducing the required DC power consumption to ensure oscillation startup, consequently increasing P_{sig}. In conclusion, the design of a high-Q resonator is very important for a high-performance VCO.

The phase noise is quantified as the power relative to the carrier frequency on a bandwidth Δf around the carrier, measured in dBc/Hz. For mmW VCOs, a

phase noise below -100 dBc/Hz at Δf = 1 MHz is desirable.

One metric used to quantify the performance of an oscillator is the classical figure of merit (FOM), which is defined as:

$$FOM = PN - 20 \cdot log\left(\frac{F_{osc}}{\Delta f} + \frac{FTR}{10}\right) + 10 \cdot log\left(\frac{P_{diss}}{1mW}\right) \quad (2)$$

where PN is the best-case phase noise in dBc/Hz, F_{osc} is the center oscillation frequency, Δf is the frequency offset where the phase noise is measured, FTR is the frequency tuning range in percent and P_{diss} is the DC power consumption of the VCO core. The smaller this FOM is, the better the VCO.

Another way of characterizing the VCO is by calculating its DC to RF efficiency. To keep the comparison fair, the efficiency calculated in this work will consider all DC power dissipation, both from the VCO core and from the buffers. The DC to RF efficiency is calculated, then, as:

$$Eff = \frac{10^{\frac{Pout+3dB}{10}}}{V_{DD} \cdot (I_{total})} \quad (3)$$

where V_{DD} is the supply voltage, I_{total} is the total current consumption of the VCO (i.e., core consumption plus helper circuits such as buffers) and P_{out} is the single-ended power output in dBm. Since a CCP VCO is a differential circuit by nature, and because both outputs are symmetrical, the total differential output power is the double of the single-ended output power, which translates to adding 3 dBm to P_{out}.

1.3.2.2 State-of-the-art

Table 1 contains the state-of-the-art of monolithic, CMOS-based VCOs. This revision focuses on continuously-tunable VCOs, or in VCOs that have some mechanism of band-switching to widen its tuning range. The VCOs contained in this state-of-the-art employ the same basic topology, that is, a resonating tank fed back by a negative resistance cell. Thus, excluding techniques such as injection locking or coupled resonators.

Table 1 - Monolithic CMOS VCO state-of-the-art.

Ref.	**Tech.**	F_{OSC} (GHz)	***Cont. FTR*** (%)	$P_{DC}{}^{\#}$ (mW)	***PN*@ 10 MHz** (dBc/Hz)	**FOM@ 10 MHz** (dBc/Hz)	$P_{out}{}^{\#\#}$ (dBm)
[25]	65-nm CMOS	76.5	6.27	14.3	-109	175.1	-1.5
[31]	65-nm CMOS	73.8	N/A	8.4	-112.2	-180	-17
[32]	65-nm CMOS	81.5	14	33	-97.3*	-179.7*	N/A
[33]	90-nm CMOS	56.7	16	8.7	−118.7	−184.3	-3.6
[34]	130-nm CMOS	91	0.5	46	-86.2*	-169.6*	+4.5
[35]	65-nm CMOS	70.2	N/A	7.7	-112	-180.4	N/A
[36]-1	65-nm CMOS	75.9	N/A	12	-109.4	-176.2	N/A
[36]-2	65-nm CMOS	89.4	N/A	11	-108.3	-176.9	N/A
[37]	65-nm CMOS	64	7	5	-113.7	-182.8	-17
[38]	40-nm CMOS	86.2	5.8	28.4	-118.8	-183.2	N/A
[39]	65-nm CMOS	105	9.5	54	-92.8*	-175.5*	+4.5
[40]	65-nm CMOS	62.8	N/A	21.5	-114.95	-177.6	-10
[41]	65-nm CMOS	59	5.4	16.5	-112	-175.5	-0.9
[42]	55-nm CMOS	77.3	3.25	15.1	-115.1	-181	-1.12
[53]	55-nm CMOS	77.1	4.79	5.69	−115	−185.0	-4.5

*PN and FOM at 1MHz offset; #whenever available, core power is presented; ##Pout generally requires extra DC power (not necessarily shown) due to buffers. Furthermore, if single-ended power is reported, we add 3 dB to the reported value

2 MNM TECHNOLOGY PHASE SHIFTERS

This chapter will present all the passive components designed, fabricated and characterized on the Metallic nanowire Membrane (MnM) interposer technology, with the objective to build a mmW phase shifter. A short overview of the MnM technology platform will be presented, then the phase shifter will be presented in detail.

The Metallic nanowire Membrane interposer technology uses a thin membrane made of Anodic Aluminum Oxide (AAO) as substrate for mechanical integration of different devices and for passive RF structures and interconnections. The interposer technology has been in development for almost 10 years at the *Laboratório de Microeletrônica da Universidade de São Paulo* (LME-USP), and its fabrication processes and electrical characterization of the substrate are already mature.

The MnM interposer technology was already used to design innovative and high-performance passive devices in mmW, such as TSV transitions [43], 3D spiral inductors [44], slow-wave transmission lines and waveguides [45] [46] and antennas [47], showing its good performance as RF substrate and versatility as interposer technology. Table 2 shows the state-of-the art for interconnections on interposers at mmW, showing both the losses and sizes of through-substrate vias (TSV) and electrical parameters of transmission lines. The porous alumina used as substrate for the MnM interposer technology features results that rival, or excel, the state-of-the-art.

Table 2 - State-of-the-art of through-substrate vias and transmission lines on interposers for mmW.

	Via			***Transmission Lines***			
Substrate Material	***Transmission loss of two transitions (dB)***	***Via size***	***Via length (µm)***	***Type***	***α (dB/mm) @60 GHz***	ε_{reff}	Z_C **(Ω)**
Glass	*0.07 @ 20 GHz*	*Ø 40 µm*	*64*				
Glass	*0.68 @ 50 GHz*	*Ø 55 µm*	*366*				
LCP	*0.24 @ 40 GHz*	*Ø 105 µm*	*51*	*CPW*	*1.5*	*1.5*	*50*
LCP	*2 @ 110 GHz*	*Ø 50 µm*	*51*				
Si (HR)	*0.06 @ 40 GHz*	*190 µm x120 µm*	*100*	*CPW*	*0.5*	*4.5*	*50*
Si (HR)	*1.06 @ 75 GHZ*	*Ø 42 µm*	*250*				
Porous Alumina	***0.46 dB @ 110 GHz***	***20 µm x 45 µm***	***50***	***CPW µS***	***< 0.4***	***5.2-3.8***	***44-140***
Porous Alumina	***0.2 dB @ 110 GHz***	***50 µm x 32 µm***	***50***	***SW-µS***	***0.62-1.0***	***90-20***	***10-43***

2.1 OVERVIEW OF THE MNM INTERPOSER TECHNOLOGY

AAO is a self-organized material with a honeycomb-like structure of high-density arrays of parallel nanopores. The nanopores are formed by anodization of aluminum in certain conditions that balance the local growth and dissolution of the aluminum oxide. The pore diameter can be controlled with great precision from a few nanometers up to a few hundred nanometers. The membrane is then detached from the aluminum electrode and its thickness is controlled as needed, with values ranging from a few nanometers up to hundreds of micrometers.

Alumina itself is an excellent substrate for microwaves and for mmW. It is characterized at mm-wave frequencies [48] and it displays low substrate losses throughout, thus enabling the fabrication of high-performance passive devices. One of the issues with alumina, however, is its hardness and chemical stability. This makes etching or drilling holes into the substrate, to form TSVs, for example, a very difficult process, which in turn tends to limit the minimum via diameter. The presence of nanopores through the substrate add flexibility to the substrate, because if the nanopores are filled with metal, they can serve as basis for high-performance, high form factor TSVs and for slow-wave microstrip lines. Thus, the need for making holes in the substrate is lifted.

There are various AAO membrane manufacturers, which offer them in a wide range of different porosities, pore diameters and thicknesses. Figure 4 shows some membranes available from Inredox [49], and the nanopores in detail.

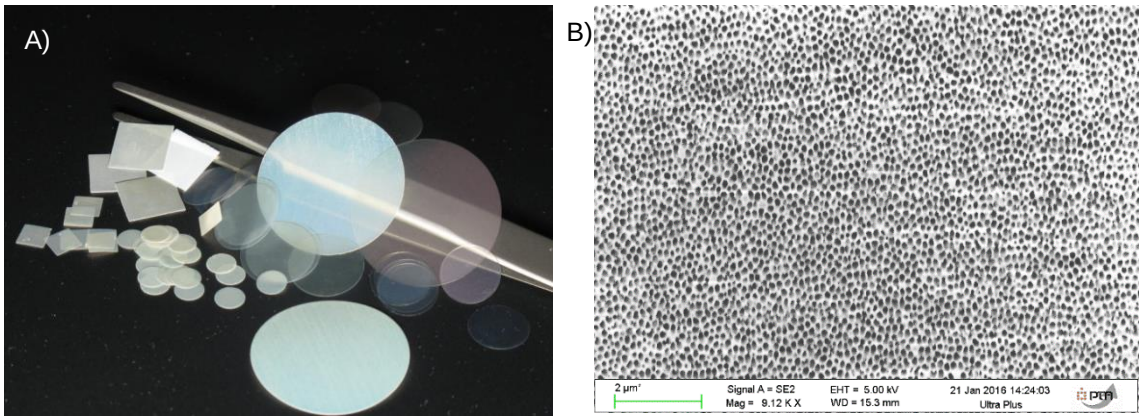


Figure 4 – A) AAO membranes in different diameters, thicknesses and pore diameters. B) Electron scan of a membrane showing the nanopores. Source: https://www.inredox.com/products/nanofab-toolbox/aao-wafers-packs/ and author.

The MnM interposer technology uses 50 µm-thick AAO wafers with 40 nm of pore diameter. The wafer diameter is 1 inch, about 2.54 cm. The membranes

are annealed at 600 °C after fabrication by request of our research group to improve its electrical characteristics. The nanoporous membrane was characterized up until 67 GHz in previous works and its electrical characteristics are shown in Table 3.

Table 3 - Electrical characteristics of the AAO membrane used in the MnM interposer technology.

Parameter	Value
$\boldsymbol{\varepsilon_r}$	6.7
$tan(\delta)$	0.015
σ_{Cu}	4.17 MS/m
$\sigma_{NANOWIRES}$	100 kS/m

Every interposer technology is linked to a fabrication process, such as CMOS for Si-based interposers, or LTCC/HTCC for ceramic substrates. In the case of the MnM interposer technology, the fabrication process as well as the individual steps are developed and carried entirely at the facilities of the Laboratório de Microeletrônica da Universidade de São Paulo (LME-USP). The different steps depend on the exact devices being fabricated. They are: thin film deposition via magnetosputtering; wafer polishing; electroplating; damascene metal thickening; localized substrate corrosion; photolithography; sacrificial layer deposition, etc. For a more detailed description of the in-house fabrication process developed for the MnM devices, the reader is encouraged to read Júlio Pinheiro's doctoral thesis [50].

The MnM interposer technology will be used as basis for all passive devices described in this work.

2.2 MNM PHASE SHIFTER

The phase shifter designed on the MnM interposer technology uses several different concepts to realize a compact, well-performing phase shifter working at mmW. The phase shifter itself is based on the MnM slow-wave microstrip lines. In short terms, the electric field is concentrated in the insulant material between the signal strip and the copper nanowires, increasing the unit length capacitance of the line while not disturbing the magnetic field distribution between the strip and the ground plane in a significant matter. Thus, the phase velocity decreases and with it the physical dimensions of the devices. It has the side effect of decreasing the characteristic impedance of the structure, but this leads to further

size reduction. Figure 5 illustrates this concept by comparing the electric and magnetic field distribution between a traditional, non-slow-wave microstrip line, and a slow-wave microstrip line.

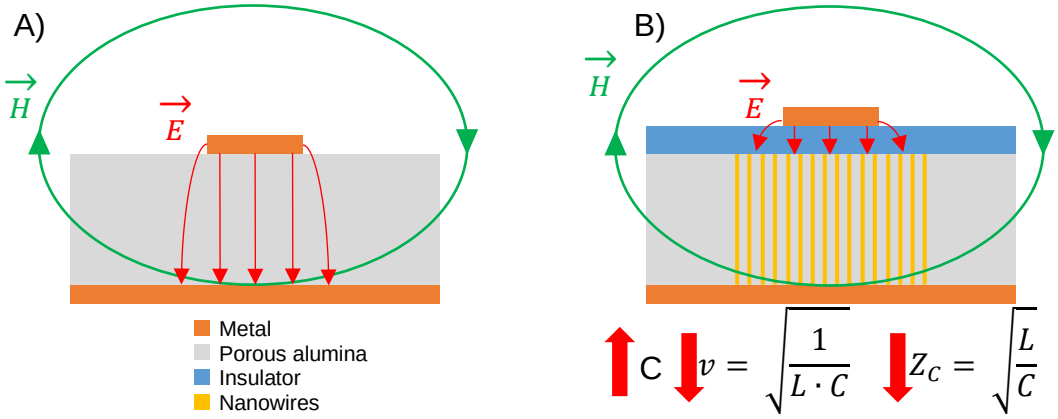


Figure 5 - Slow-wave mechanism of the MnM slow-wave microstrip lines. A) shows the cross-section of a traditional microstrip line on the MnM substrate with the electric and magnetic fields sketched over the structure. B) shows the cross section of a slow-wave microstrip line, showing the confinement of the electric field and the consequent reduction in phase velocity and characteristic impedance. Source: author.

Taking this concept as the core for the MnM phase shifter, the phase velocity, thus the electrical length, can be controlled by varying the unit length capacitance of the slow-wave microstrip line. This can be achieved by two means: either by changing the dielectric constant of the insulator material, or changing the distance between the strip and the nanowires. If an air cavity is created between the strip and the nanowires, and such cavity is filled with an electrically-tunable material, both tuning methods can be achieved. The novel suspended microstrip line topology developed in this thesis enables both tuning methods and is, thus, the core of the MnM phase shifter.

Next, the main elements of the MnM phase shifter will be presented and explained in detail, starting by the suspended microstrip lines.

2.2.1 SUSPENDED MICROSTRIP LINES

The suspended microstrip lines are based on the slow-wave microstrip lines presented above, but the strip is elevated from the nanowires on the substrate and the gap between strip and nanowires is filled with air. This way, the device retains some electric field containment at the benefit of decreased propagation losses because of the absence of losses in air, with the side effect of increasing the characteristic impedance of the transmission line when compared to a slow-

wave microstrip line with the same dimensions.

This section presents the structure of the device and its equivalent model, which will be used to design some devices for characterization. Then, the measurement results will be presented and compared to EM simulations.

2.2.1.1 Structure

The strip has to be periodically anchored to the substrate, because long suspended sections are more prone to stiction because of static charges or surface tensions of solvents used during the fabrication process. Naturally the anchoring will add some parasitic effects that will interfere with the functioning of the desired, suspended strip, so the electrical length of the anchoring has to be kept as small as the fabrication process allows. The final structure, thus, is a periodic series of long, suspended sections with short anchoring sections between them. Figure 6 shows a simplified 3D view of the suspended microstrip line section and a longitudinal cross-section that shows both the suspended regions as well as the anchoring.

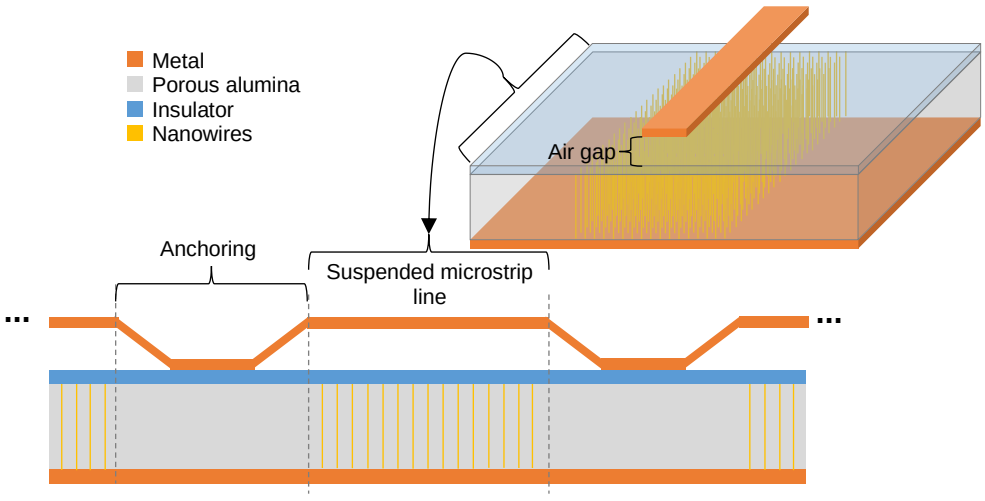


Figure 6 – Simplified structure of the suspended microstrip lines containing a 3D view and a longitudinal cross-section showing the periodoc anchorings necessary to keep the strip from sticking to the substrate during fabrication. Source: author.

2.2.1.2 Model

The equivalent electrical model for the suspended microstrip line reflects the periodic nature of the device itself, and so it will be divided into its building blocks: the suspended slow-wave microstrip section, and the anchoring section.

Figure 7 shows the longitudinal cross-section of the suspended microstrip line plus its anchoring and the equivalent electrical model of every section and the relevant lengths of the device. The suspended microstrip is modelled as a slow-wave microstrip line, whose modelling is explained in [51], where insulator capacitance is modified to include the gap height (g) in its calculation (C_{GAP}), thus the gap is calculated as g plus the oxide thickness (t_{OX}). Aside from this modification, the nanowire inductance and resistance (L_{NW} and R_{NW}) and strip inductance (L_S) are calculated the same way as in a slow-wave microstrip line, as described in [52]. All variables are per unit length and should be multiplied by the suspended strip length (l_S) whenever applicable.

The anchoring section is comprised of a short length of traditional microstrip line plus two transitions: one coming from the previous suspended section and another leading to the following suspended section.

The transitions are modeled as a T-network comprising a series anchoring inductance and shunt capacitance (L_{ANCH} and C_{ANCH}). The microstrip line on the substrate is modelled by the standard microstrip line model. The anchoring length (l_{ANCH}) comprises both transition and the anchoring microstrip.

The model for the whole transmission line is simply a series concatenation of anchoring and suspended microstrip line sections. This way the anchoring parasitics are incorporated into the desired, suspended microstrip line response, as the anchoring is an integral part of this device.

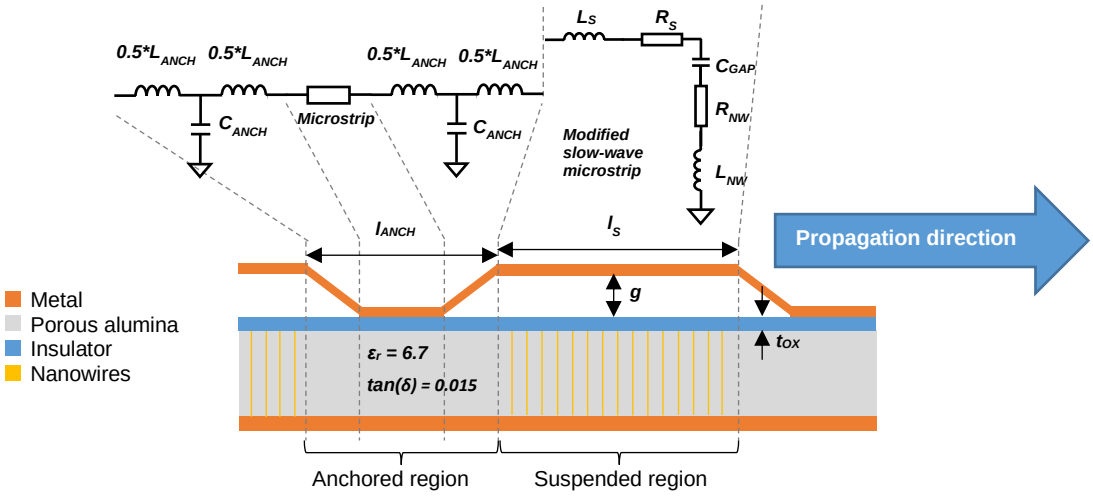


Figure 7 – Longitudinal cross-section of the suspended microstrip line showing its most important physical dimensions and the equivalent electrical model of each section (anchoring and suspended microstrip line). Source: author.

The design for a suspended microstrip line starts by defining the desired suspended line characteristics and then accounting for the anchoring parasitics. The suspended microstrip line characteristic impedance (Z_C) and effective dielectric constant (ε_{reff}) are a function of g and of the strip width (W_S). Figure 8 presents the Z_C and the ε_{reff} for the suspended microstrip line versus strip width for g = 2 µm and g = 4 µm, and also the Z_C and ε_{reff} for a slow-wave microstrip line with t_{OX} = 1 µm for reference, with Si dioxide for insulator.

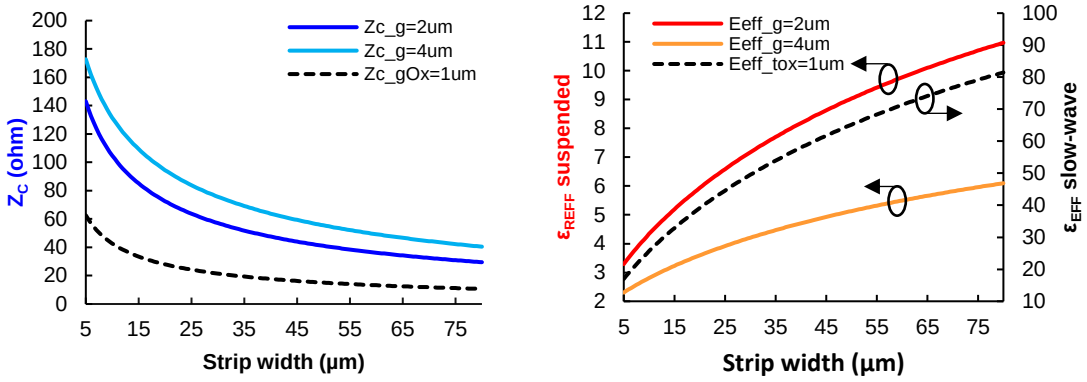


Figure 8 – Characteristic impedance and effective deielctric constant of the suspended microstrip line and slow-wave microstrip line in function of the strip width. Two gap heights are considered for the suspended lines: 2 µm and 4 µm. For the slow-wave microstrip lines, the insulator thickness is 1 µm. Source: author.

The Z_C increases with g and diminishes with W_S and can be as high as 175 Ω for W_S = 5 µm and g = 4 µm and as low as 30 Ω for W_S = 80 µm and g = 2 µm. ε_{reff} follows the inverse of this rule, diminishing with g and increasing with W_S, being as low as 2.3 for W_S = 5 µm and g = 4 µm and as high as 10.9 for W_S = 80 µm and g = 2 µm. On another hand, the slow-wave microstrip lines show Z_C between 56 Ω and 10 Ω and ε_{reff} between 17 and 80.9, showing the stronger slow-wave effect because of the reduced separation between strip and nanowires and the higher relative dielectric constant ε_r of the insulator (3.9 for SiO_2 against 1 for air).

To validate the accuracy of the model and the performance of the suspended microstrip lines, three different structures were designed and fabricated with W_S = 15 µm, 25 µm and 35 µm, respectively. The g was fixed at 4 µm because of fabrication constraints at the time these devices were fabricated.

2.2.1.3 Fabrication and measurements

The fabrication process for the suspended microstrip lines and RF pads happened as follows, and is illustrated in Figure 9. Starting with a bare AAO membrane, SiO_2 with 200 nm is deposited on the top side, by magnetron sputtering (Figure 9a). On the bottom side, a thin copper layer of approximately 30 nm is also deposited by sputtering (Figure 9b). The top SiO_2 is then patterned (Figure 9c) and used as mask for the selective copper nanowire growth (Figure 9d). Nanowires are grown by electrodeposition using MacDermid Enthone's MacuSpec PPR 100 acid copper plating process. After 1.5 hours of copper deposition using Periodic Pulse Reverse (PPR), a solid copper film is formed on the top side of the membrane. To expose the nanowires and remove this solid film, the top side is polished.

Another 300nm-thick SiO_2 film is deposited on the top side to serve as mask for the nanowire TSVs and to seal the still open nanopores (Figure 9e). The photoresist AZ9260 was deposited and patterned to be used as sacrificial material (Figure 9f) to form an air gap of ~4 µm. Figure 9g illustrates the deposition and definition of the top copper layer. For that, another thin copper layer was deposited by sputtering to be used as seed layer for the electrodeposition of copper using the same solution used for the nanowires. Photoresist was used to mask regions where the copper was not to be electrodeposited. On the exposed areas: microstrip with the suspended regions; anchors; and RF pads, the copper is thickened to 3 µm. Later, the copper seed is removed. The final step, illustrated in Figure 9h, is the release of the suspended line. The sample is submerged in acetone at 40°C for 1 hour, then for 5 minutes in isopropanol at 40°C.

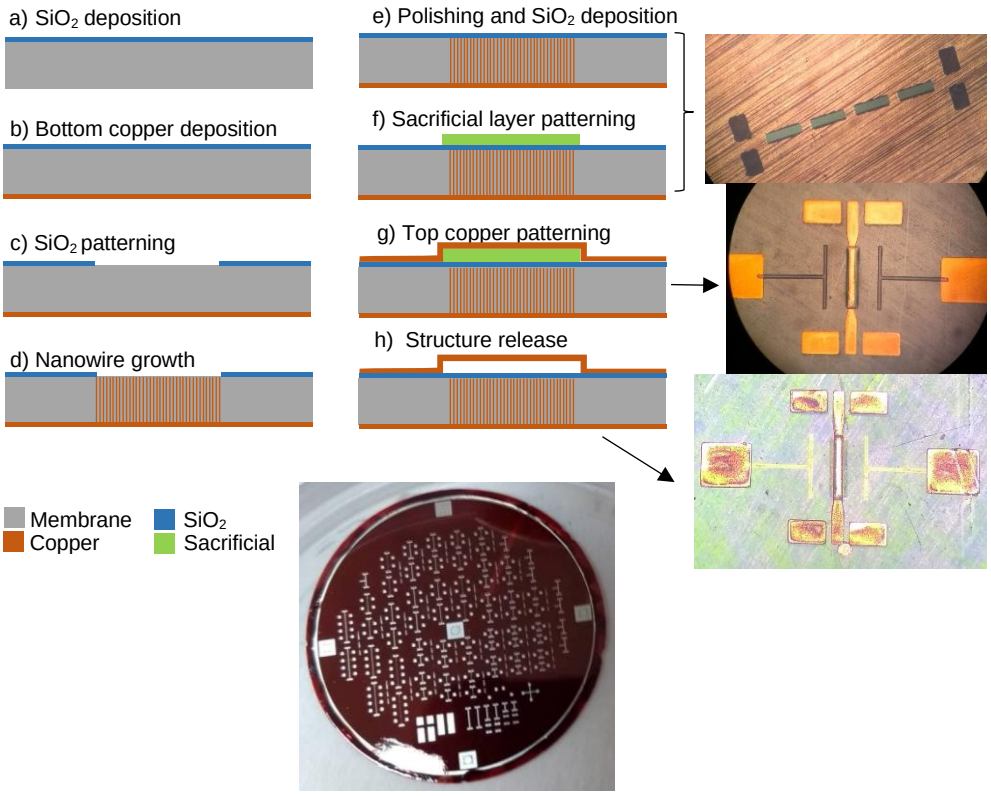


Figure 9 – Fabrication process used to fabricate the suspended microstrip lines on the MnM substrate and a photo of the completed membrane wafer. Source: author.

It is known from experience that the AZ9260 patterning process causes thickness variations across the length of the patterned region, being thicker close to the edges and thinner at the center. To verify the impact this variation has on the performance, lines with two different values of L_S were fabricated: 250 µm and 500 µm. In total, six different devices were fabricated. Their dimensions, number of suspended segments (N_S), as well as their ideal Z_C, are shown in Table 4. In all structures, the l_{ANCH} is 100 µm: 50 µm for the anchoring and 25 µm for each transition.

Table 4 - Ws, Ls, number of segments, total length and characteristic impedance of the fabricated suspended microstrip lines.

W_S (µm)	Z_C (Ω) (g = 4 µm)	L_S (µm)	N_S	Total length (µm)
15	109	250	4	1450
		500	2	1250
25	84	250	4	1450
		500	2	1250
35	63	250	4	1450
		500	2	1250

The suspended microstrip lines were characterized up to 67 GHz using

ground-signal-ground (GSG) probes (MPI Titan probes with 100 µm-pitch) in a manual probe station and a Keysight PNA N5227B vector network analyzer. A LRRM calibration was done. Unfortunately, due to process variations, no TRL calibration was possible. The raw S-parameter data of the DUTs plus accesses was de-embedded in ADS to enable the extraction of the DUT characteristics. The GSG pads were simulated in ADS momentum and then its S-parameter matrix was used for de-embedding. However, the de-embedded data contains imprecisions at frequencies below 20 GHz, due to the variation of the shunt capacitance between the GSG ground and the nanowires underneath.

Figure 10 shows a picture of the fabrication result of a suspended line with four suspended segments, whose L_S = 250 µm and W_S = 25 µm. The air gap, nanowire-filled regions and the profile of the GSG pads are shown in detail. No stiction was observed in any of the devices and a visual inspection revealed no obvious fabrication defects.

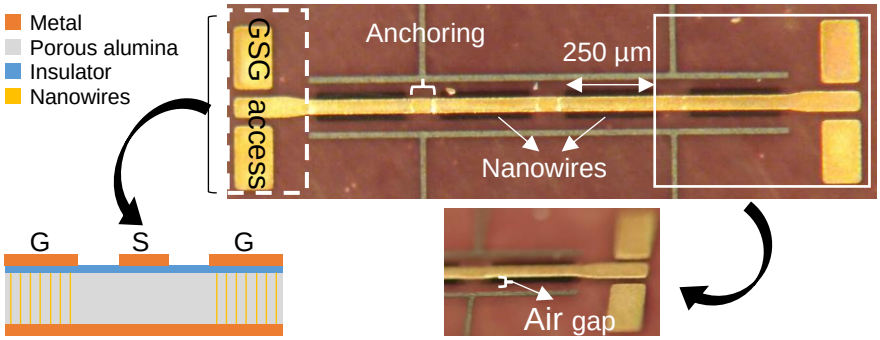


Figure 10 – Photo of a fabricated suspended microstrip line with W_S = 25 µm, 4 segments and L_S = 250 µm showing the RF pads, the regions filled with nanowires and the air gap between the substrate and the signal strip. Source: author.

Figure 11 shows the measured return loss and insertion loss of all fabricated devices. Also, it shows the comparison between two different devices and their respective EM simulation results, and the fitting from the model presented in Figure 7 and Figure 8.

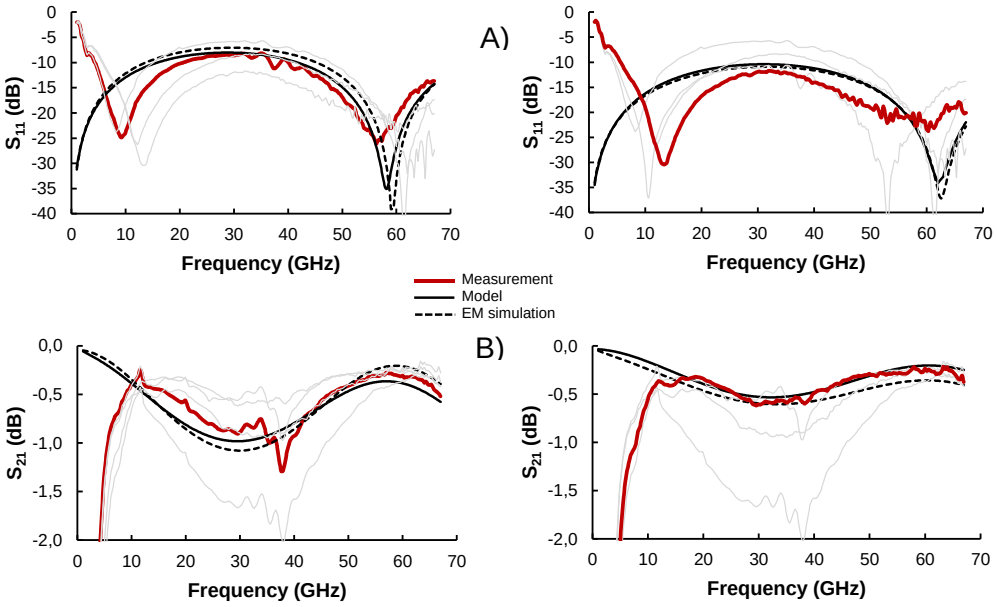


Figure 11 - Measured S-parameters of all fabricated suspended microstrip lines (light grey). In detail (red), the measurement is compared against the EM simulation (dashed black) and the proposed model (black). A) Comparison of return for 4 segments, W_S = 25 µm and L_s = 250 µm (left column) and for 2 segments, W_S = 35 µm and L_s = 500 µm (right column). B) Comparison of the insertion loss for the same devices. Source: author.

The model response was obtained by conducting a manual parametric fit using the measurement curves as template. It can be seen that the correlation between simulation, model and measurement is very good above 20 GHz, thus confirming the validity of the proposed model.

Table 5 contains the ε_{reff}, Z_C and attenuation constant (α) fitted for the slow-wave microstrip line of the two devices shown in detail in Figure 11 for both measurement and EM simulation. The values outside parenthesis are for the suspended segments only, and they are compared against the values given by the slow-wave microstrip line model shown in Figure 8. The values inside parenthesis, where applicable, refer to the suspended segments plus anchoring parasitics.

Table 5 – Characteristic impedance, effective dielectric constant and attenuation constant of the suspended microstrip line segments extracted from measurement and compared against EM simulations. Values in parenthesis are for suspended lines plus anchoring parasitics

4 segments, L_S = 250 µm, W_S = 25 µm			
	Measurement	**Simulation**	**Model (Figure 8)**
Z_C (Ω)	82 (75)	88 (81)	84
ε_{reff}	4.0 (4.8)	3.8 (4.6)	3.9
α (dB/mm @60GHz)	0.252	0.163	
2 segments, L_S = 500 µm, W_S = 35 µm			
	Measurement	**Simulation**	**Model (Figure 8)**
Z_C (Ω)	69 (66)	70 (68.6)	69.1
ε_{reff}	4.6 (5)	4.7 (4.95)	4.7
α (@60GHz)	0.292	0.168	
Anchoring parasitics			
	L_{ANCH}	**C_{ANCH}**	
W_S = 15 µm	3.58 pH	1.78 fF	
W_S = 25 µm	2.53 pH	2.82 fF	
W_S = 35 µm	2.41 pH	2.68 fF	

The anchoring indeed affects the propagation characteristics of the suspended microstrip line by increasing the equivalent shunt capacitance to ground, which reflects in increasing ε_{reff} and reducing Z_C. It can also be noted that the fabricated lines present more insertion loss than predicted by simulations. Figure 12 shows the attenuation constant α for all measured devices. The average α for these transmission lines at 60 GHz is 0.27 dB/mm.

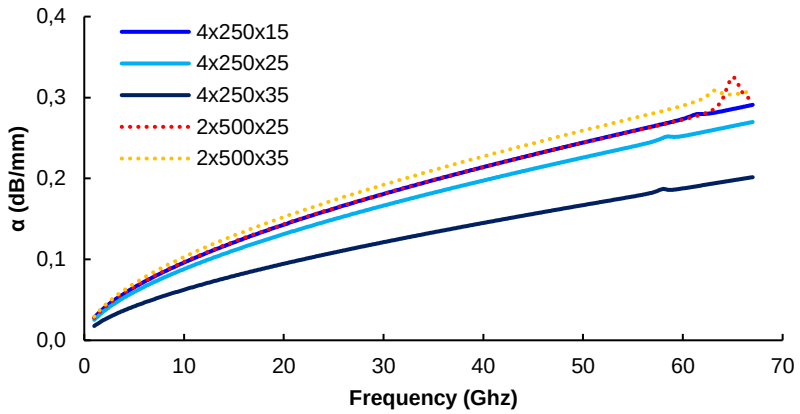


Figure 12 – Attenuation constant for the measured suspended microstrip lines. Source – author.

Next the transmission lines were compared against traditional microstrip lines, fabricated on the MnM substrate with no copper nanowires underneath

them. Figure 13 shows the Q-factor for the measured suspended microstrip lines compared against traditional microstrip lines of the same Z_C. It can be seen that the suspended microstrip lines perform as well as standard microstrip lines, outperforming them at frequencies above 30 GHz.

Because of the slow-wave effect, the suspended microstrip lines are very sensitive to the electrical characteristics of the gap material. Air, having no dielectric loss, make so that the main loss mechanism for the suspended microstrip lines is conductor loss from the signal strip and from the nanowires.

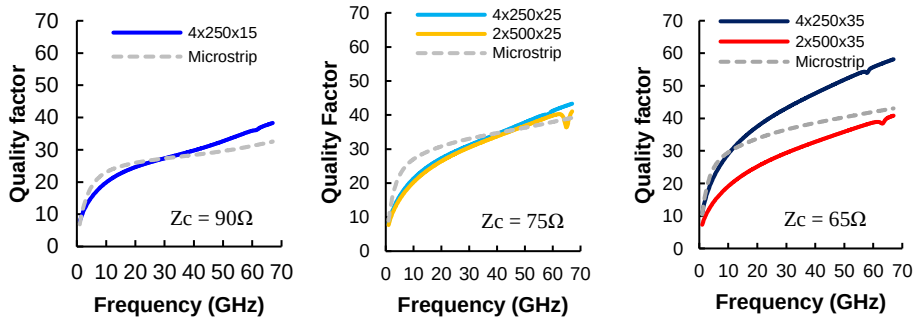


Figure 13 – Comparison of the quality factor between the measured suspended microstrip lines and traditional microstrip lines designed on the MnM substrate. Source – author.

2.2.1.4 Partial conclusions

The suspended microstrip lines were presented, as well as their equivalent electrical model. The suspended microstrip lines were fabricated, measured and these data were compared against EM simulations and against the parametric fit using the proposed electrical model. The correlation is very good, thus confirming the accuracy of the model. The suspended microstrip lines themselves have good RF performance and are a suitable element for high-Z_C interconnections.

2.2.2 Liquid crystal MnM phase-shifter

Having presented and discussed the suspended microstrip lines, now the MnM phase shifter is presented in this section. Figure 14 shows the basic structure of the MnM-LC phase shifter. It comprises a suspended microstrip line whose air cavity is filled by a LC solution.

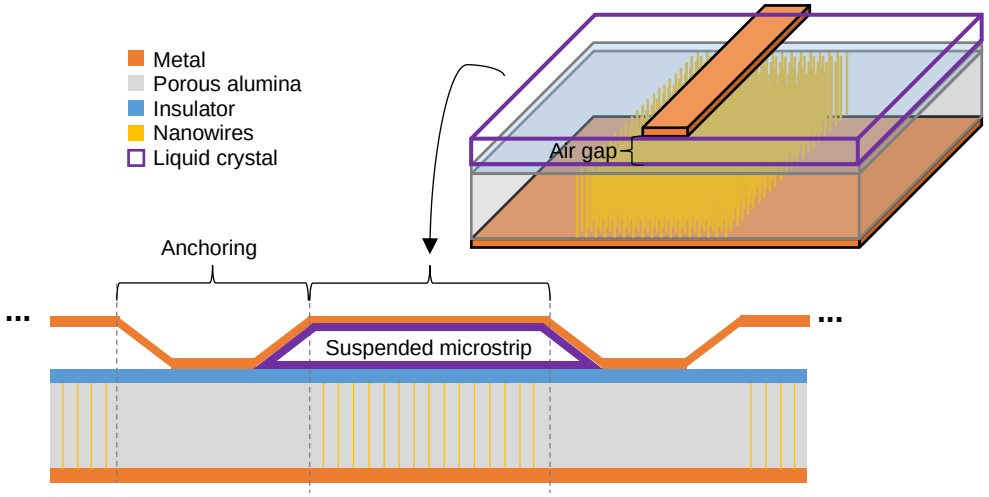


Figure 14 - Basic structure of the MnM liquid crystal phase shifter, showing a 3D-view of the suspended region and a cross-section of the anchoring plus suspended regions. Source: author.

The MnM phase shifter achieves phase velocity variation by changing C_{GAP} in two different ways. The first is by changing the gap distance, by applying a biasing potential higher than the pull-in voltage for the suspended line, so the line switches like a MEMS switch. The second is by modifying the ε_r of the gap material by adding an electrically-tunable material between the signal strip and the nanowires.

Liquid crystal (LC) solutions are the material of choice to be added to the gap because of two main reasons: the first being that LC loss tangent decreases with frequency; the second being that the LC reduces the pull-in voltage for the MEMS switching by an amount equal to ε_r and, being a liquid, won't impede the electrostatic switching from happening.

2.2.2.1 Overview of liquid crystals

LCs are a state of matter whose physical properties are between those of a liquid and of a solid: even though it may flow like a liquid, its molecules show some degree of large-scale ordering like a crystal. There are many different phases, or states, in LC substances, the most important for the needs of this work is the nematic phase. In the nematic phase, even though the LC molecules' distribution may be randomized, they display large-scale self-orientation because of their shape. When these molecules have a dominant dimension, they can be approximated as being rod-like. A LC substance whose molecules are rod-shaped is called a calamitic LC. Thus, a nematic calamitic LC has its rod-shaped

molecules self-oriented in a thread-like, large-scale structure. Even though they have capacity of self-alignment, LC molecules in a nematic calamitic LC can be re-oriented by external coercive forces in the form of electric or magnetic fields. In this work only the purely electric biasing will be used.

Nematic calamitic LCs show anisotropic electric and optical characteristics depending on the angle to the axis of orientation of the molecules, and this characteristic is what gives it their electric tunability. The two extreme states are when the rod-shaped molecules are oriented parallel to the RF fields and when they are orthogonal to the RF fields. The transition between these two states is continuous and is a function of the angle between the molecules and the external RF fields. Figure 15 exemplifies this phenomenon. The LC molecules, shown as elongated blue ellipsoids, are aligned to an external electric field (E_{bias}) and, being subjected to external RF fields, display different electric properties: Figure 15 A) the fields are orthogonal to the molecules, and the LC is characterized by $\varepsilon_{\perp}$ and $tan\ (\delta)_{\perp}$. In Figure 15 B) the fields are parallel to the molecules, and the LC is characterized by $\varepsilon_{//}$ and $tan\ (\delta)_{//}$. If the angle between the LC molecules and the RF fields is between 0° and 90°, the equivalent electrical characteristics of the LC will be an intermediate value between these two extremes and proportional to the dot product between the RF fields and the dominant axis of orientation of the LC molecules.

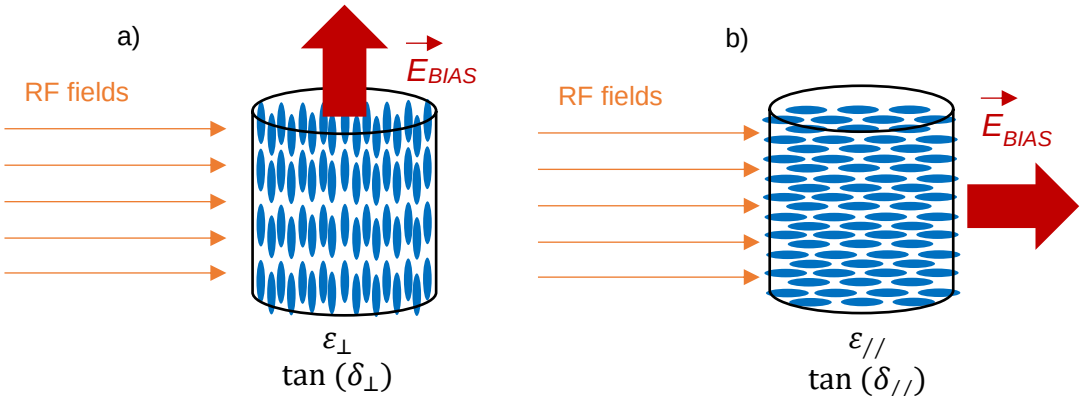


Figure 15 – Illustration of liquid crystal electric anisotropy towards external RF fields. The liquid crystal molecules are presented as light-blue ellipsoids. Source: author.

Table 6 shows the electrical characteristics of two different LC solutions at 19 GHz. BL111 is an older type of LC solution developed for LC display applications, however more recently new LC solutions were developed aimed specifically for microwave and mm-wave applications. These newer solutions,

such as GT3-23001 from Merck KGaA, Darmstadt, Germany, have lower losses and wider electric tunability, T_ε.

Table 6 – Electric characteristic of BL111 and GT3-23001 liquid crystal solutions at 19 GHz. Source: [53]

LC solution	$\varepsilon_{//}$	$tan(\delta_{//})$	$\varepsilon_{\perp}$	$tan(\delta_{\perp})$	T_ε(%)
BL111	3.25	0.0084	2.64	0.0218	18.77
GT3-23001	3.19	0.0035	2.41	0.0143	25.2

2.2.2.2 Phase shift mechanisms

The core structure for this LC phase shifter is the suspended microstrip line, where the LC is injected in the gap between the signal strip and the nanowires. The presence of the LC acts as the insulator material in the slow-wave microstrips presented in Figure 5.

Under no bias the LC molecules will rest parallel to the substrate, guided by the substrate surface. If, then, a positive voltage is applied between the signal strip and the grounded nanowires, the LC molecules will start to reorient themselves parallel to the biasing electric field. The electric field creates torque on the LC molecules, which is proportional to the field intensity. If the voltage is above a certain threshold, called the *Freedericksz threshold* (V_{FTH}) [54], the torque from the electric force will overcome the restoring torque and the LC molecules will start to reorient themselves parallel to the electric field. The angle between the LC molecules and the electric field will follow a continuous relation until the biasing voltage is high enough so the LC molecules are completely parallel to the electric fields. This translates to a change in the suspended microstrip ε_{reff} and, thus, in phase velocity. The change in phase velocity creates the phase shift.

Now, if the voltage is above another, higher threshold, which is the pull-in voltage for the suspended strip, the strip will switch, collapsing towards the nanowires like a MEMS switch. This will dramatically reduce the distance between the strip and the nanowires, strongly increasing C_{GAP} and, thus, decreasing the phase velocity. The LC will lower the pull-in voltage of the strip because of its relative dielectric constant. This mechanism creates strong phase shift in a binary way.

Figure 16 a) shows the 3D view of the suspended microstrip lines with LC injected around it, as well as a simplistic representation of the biasing

mechanism: a biasing voltage V_{bias} is applied between the suspended strip and the grounded nanowires below, superimposing the biasing electric field to the RF field of the suspended microstrip. The 1 MΩ resistor acts as current limiter in the event of dielectric breakdown to protect the devices and the RF probes.

Figure 16 b) shows a representation of the phase shift in function of V_{bias}: (i) for V_{bias} smaller than the V_{FTH}, the phase shift is zero because the molecules are not disturbed, the resultant force being the restorative elastic forces; (ii) for V_{bias} higher than V_{FTH}, the LC molecules start aligning themselves to the biasing field and V_{bias} has direct control over the phase shift; (iii) when V_{bias} reaches a saturation voltage (V_{LC_sat}), the LC molecules are fully parallel to the RF fields and the LC does not contribute to the phase shift, however, the electrostatic forces on the suspended strip may cause it to sag, reducing the gap distance a little and causing some phase shift; (iv) however, when V_{bias} reaches the pull-in voltage (V_{PI}), the suspended line switches and the gap distance is drastically reduced, resulting in strong phase shift.

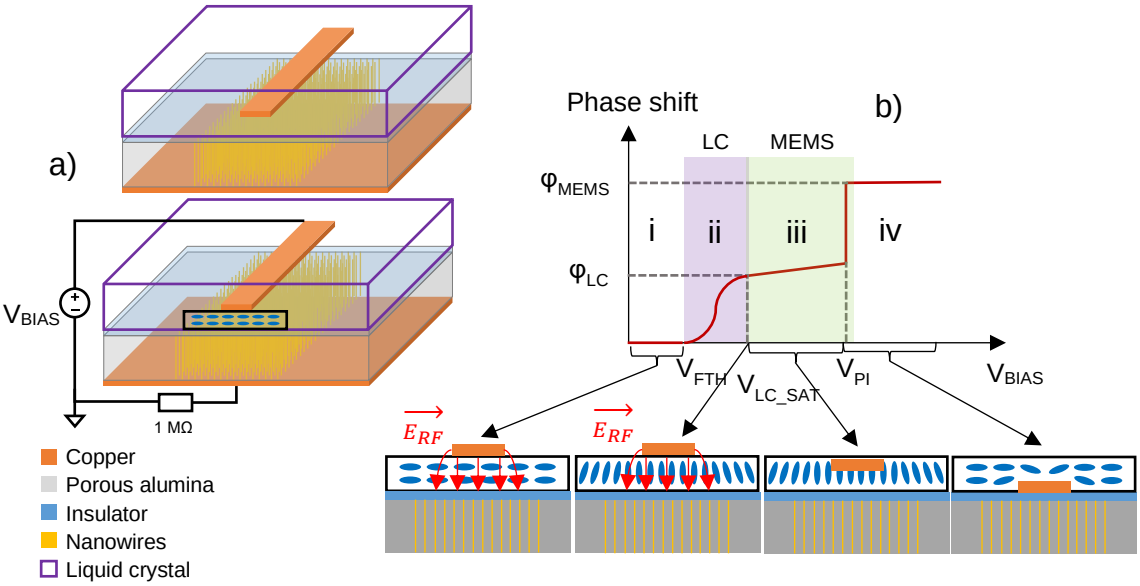


Figure 16 – a) A side view of the LC-MnM phase shifter showing the main elements and the biasing scheme to bias the liquid crystal and to create electrostatic switching. b) Phase shift of the LC-MnM phase shifter as a function of the applied bias voltage, showing in detail the signal strip position and the liquid crystal orientation in each region. Source: author.

2.2.2.3 Electric and mechanical modelling

Being based on the suspended microstrip lines, the MnM phase shifter shares the same model described in Figure 7. However, this time C_{GAP} is changed to a variable capacitance C_{LC}, which models the variable capacitance of the LC

plus MEMS switching. The LC losses are modelled by a parallel conductance, R_{P_LC}. The modified model is presented in Figure 17.

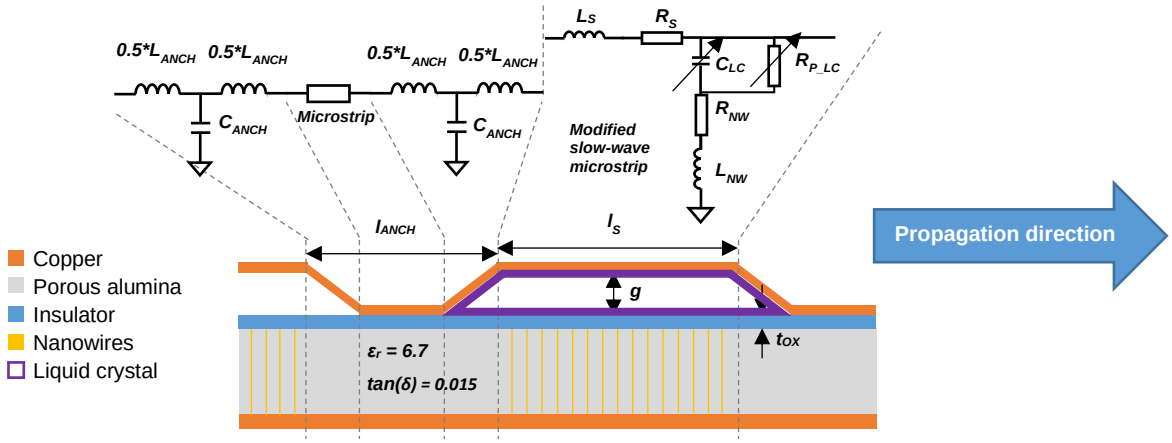


Figure 17 – Side view of a single segment of the LC-MnM phase shifter with its equivalent electrical model. Source: author.

As previously described, there are two important voltage values for the electric biasing of the MnM phase-shifter: the *Freedericksz threshold* V_{FTH} and the V_{PI}. The V_{FTH} is estimated as the electric field (E_{FTH}) where the electric force produces a torque that equals the torque from the restoring elastic force, and is given as [54]:

$$E_{FTH} = \frac{\pi}{g}\sqrt{\frac{K_{ii}}{\varepsilon_0 \cdot \Delta\varepsilon}} \tag{4}$$

where g is the LC cavity height, K_{ii} is the Frank elastic constant and $\Delta\varepsilon$ is the variation of dielectric constant of the LC mixture. However, this equation is an estimative, as K_{ii} is hard to evaluate in practical conditions, but it tells that E_{FTH} is dependent on the geometry of the cavity, and that by diminishing g, the required V_{FTH} can be reduced.

The other important voltage threshold, V_{PI}, arrives from the mechanical force equilibrium of the suspended microstrip, which is modeled as a suspended beam. The actual V_{PI} calculation of a fixed beam actuator involves a number of variables that are dependent on the actual material and structure, which can be very hard to determine in a practical setup. However, the V_{PI} calculation of a parallel plate MEMS actuator serves as a suitable estimative for the V_{PI} of a fixed beam. The ground plane and suspended strip are modelled as the fixed and moving plates, respectively. The equivalent restoring elastic force is modelled as

a spring with elastic constant K_S. This equivalent constant is derived by assuming a localized load at the center of the suspended strip. Even though the actual load is variable and distributed across the strip, this simplification results in the same mechanical deformation. Figure 18 a) shows the cross-section of a suspended microstrip line deformed by the electric force that results from the application of a biasing potential between the suspended strip and the ground plane, as well as the load simplification. Figure 18 b) shows the equivalent model for the fixed beam.

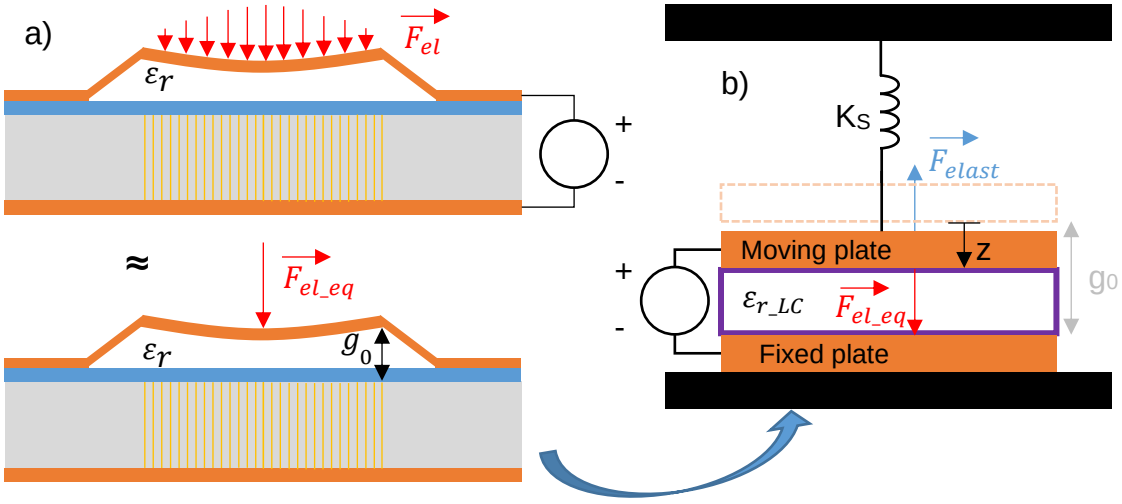


Figure 18 – a) Sagging of the suspended signal strip under the load of the electrostatic force that arises from the application of a biasing voltage, showing also the simplification of the force distribution to build an equivalent mechanical model. b) Equivalent mechanical model for a fixed beam loaded at the center by a localized load. Source: author.

By applying a potential between the moving and fixed plates the resulting electric force results in a vertical displacement (z) of the moving plate towards the fixed plate, which is counteracted by the spring elastic force, resulting in stable equilibrium. However, when $z = g_0/3$ the resulting equilibrium turns unstable, and any disturbance results in acceleration of the moving plate towards the fixed plate. The voltage that results in $z = g_0/3$ is called the V_{PI}. Equation (5) shows the V_{PI} of a fixed beam MEMS actuator simplified under two conditions: small deformations and localized load on the center of the fixed beam.

$$V_{PI} = V(z = g_0/3) = \sqrt{\frac{8K_S \cdot {g_0}^3}{27 \cdot \varepsilon_0 \cdot \varepsilon_{LC} \cdot W_S \cdot L_S}} \tag{5}$$

$$K_S = 32 \cdot E \cdot W_S \cdot \left(\frac{t}{L_S}\right)^3, \tag{6}$$

where g_0 is the gap height under no bias, K_S is the equivalent spring constant of a fixed beam, ε_0 and ε_{LC} are the vacuum permittivity and relative LC dielectric constant, W_S and L_S are the fixed beam width and length, respectively, E is the beam material Young modulus and t is the beam thickness. The only design variable that influences V_{PI} is L_S, the rest being process-dependent: E is a function of the material, copper for the case of the MnM technology; t is more or less fixed at around 3 µm to ensure good RF performance; ε_{LC} is dependent of the exact LC mixture to be used.

The actual switching does not happen equally across the length of the suspended microstrip line, being concentrated at the center of the device. The region where the suspended strip actually touches the insulating layer takes about $L_S/3$, thus the actual C_{LC} varies across the length. To simplify the modelling, the C_{LC} of the switched suspended microstrip line is supposed to be uniform.

Also, because of surface roughness, the contact between the metallic strip and the insulating layer is not perfect, so a very thin layer of either LC or air must be considered between these two parts. This thin layer will also be used to model the effects of any sacrificial material residue from the fabrication process.

The suspended strip was modelled by the same model presented in section 2.2.1, and the design process follows a similar path. This time, however, the characteristics of the LC is used instead of air. Figure 19 presents the Z_C and the ε_{reff} for the suspended microstrip line model, but loaded by LC, versus strip width for g = 4 µm, with a 200-nm-thick SiO_2 layer for insulation. The two states of the LC are presented to show the tuning capability of the device. Figure 19 also presents the Z_C and the ε_{reff} for the switched state, assuming different thicknesses for the layer of LC in its parallel state between the strip and the insulating SiO_2. The LC used for these calculations is the GT3-23001 mixture whose electrical characteristics are shown in Table 6.

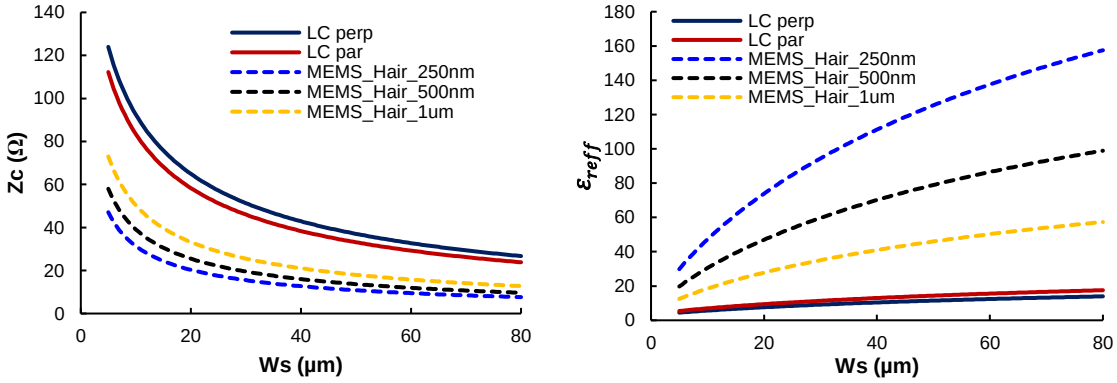


Figure 19 – Characteristic impedance and effective dielectric constant of the suspended segments of the LC-MnM phase shifter, obtained from the equivalent model of the suspended microstrip line with the addition of the liquid crystal effects. Source: author.

As expected, the switching increases the slow-wave effect dramatically, and the thickness of the added air gap degrades the amount of variation of C_{LC} of the suspended microstrip line. This increase of C_{LC} also decreases the Z_C to very low values.

2.2.2.4 Fabrication and measurement results

The fabrication process is the same as described in Section 2.2.1.3, but at the end the LC mixture is added to the structure with the aid of a syringe to minimize LC spillage, as there is no structure to confine the LC yet. In total, eleven different devices were fabricated. Their dimensions and number of suspended segments are shown in Table 7. In all structures, the l_{ANCH} is 100 μm: 50 μm for the anchoring and 25 μm for each transition. The nominal g is 4.2 μm: 4 μm for the cavity and 200 nm for the SiO_2 insulation layer. The V_{PI} for these devices is shown in Table 8 under two conditions: air-filled cavity and cavity filled with the GT3-23001 LC mixture.

Because of the high values of V_{PI}, which also reflect their smaller tendency to sag under larger biasing voltages, the structures with L_S = 250 μm were used to analyze the LC response, as the MEMS switching is well separated from the LC operation. The structures with L_S = 500 μm, in turn, were used to analyze the response from the MEMS plus LC. Also, the MEMS plus LC response is compared to the MEMS switching without LC.

Table 7 - W_s, L_s, number of segments, total length and characteristic impedance of the fabricated suspended microstrip lines for the LC MnM proof of concept.

W_S (µm)	L_S (µm)	Ns	Total length
15	250	4	1350
	500	1	550
	500	2	1250
	500	4	2350
25	250	4	1350
	500	1	550
	500	2	1250
	500	4	2350
35	250	4	1350
	500	1	550
	500	2	1250

Table 8 – Pull-in voltage for the suspended microstrip lines with and without LC injection.

L_S (µm)	V_{PI} air	V_{PI} LC
250	274 V	154 V
500	68.6 V	38.6 V

The measurements were carried out in two stages. The first, carried at the LME's mm-wave device characterization room, focused on testing the proof of concept. The phase shift versus biasing voltage was determined, as well as how the V_{PI} deviates from the values presented in Table 8, using an older LC solution: the BL111, whose electrical characteristics were presented in Table 6. The measurement setup is exactly the same as the one used to characterize the suspended microstrip lines. After gathering the necessary information, the devices were shipped to Darmstadt, Germany, where the performance measurements were carried using the better-performing, mm-wave-specific GT3-23001 LC solution. There the focus was to derive the final performance of the LC MnM phase shifters.

Figure 20 shows the phase shift of a device with L_S = 500 µm, N_S = 4 and W_S = 25 µm versus the biasing voltage at 60 GHz, and a photo of the DUT. The absence of a containing medium causes the LC to spill around the device and to flow over time, forcing the measurement time to be short as to avoid dramatic changes in the device electrical characteristics.

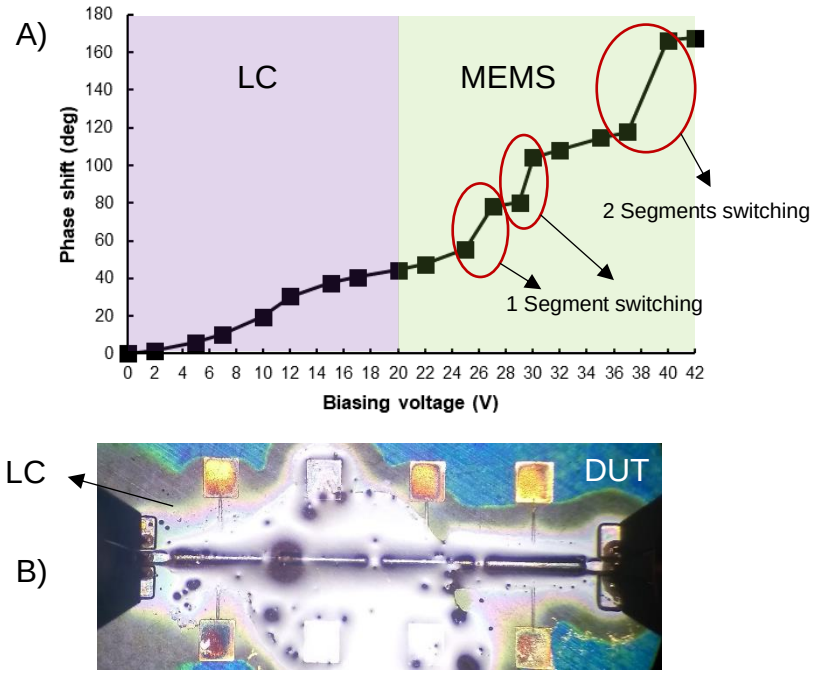


Figure 20 – a) Phase shift against biasing voltage of a device having L_S = 500 um, N_S = 4 and W_S = 25 um showing clearly the two different regions of operation of the LC MnM phase shifter. b) Device under test showing the liquid crystal injected under the device. Source: author.

The regions where the LC and where the electrostatic sagging and switching creates the phase shift are evident: below 20 V the response is dominated by the LC and is analog in nature, following a cosine-like shape. Above this value the phase-shift is dominated by electro-mechanical phenomena: between 20 V and 25 V the suspended segments sag under the increasing electric force imposed by the biasing until the segments start switching at different voltage values. The first segment switches between 25 V and 26 V, the second switches between 29 V and 30 V. The last two segments switch at roughly the same voltage, lying between 39 V and 40 V. Thus, three conclusions are drawn: the first is that the V_{FTH} doesn't affect the device, as the LC answers to biasing voltages as low as 1 V; the second is that the V_{LC_sat} is around 20 V for this cavity height; the third is that the V_{PI} can vary widely in a single device, in this case happening at 25 V, 29 V and 39 V. This, however, shows that a device can be designed to have incremental, digital phase-shift using a single biasing voltage scheme if the segments are designed to have different V_{PI}'s, and the way to do that would be to design segments with different L_S. Since L_S is the only design variable that directly controls the V_{PI}, as indicated by equation ((5), as the other variables depend on the fabrication process itself and cannot be changed

between different suspended microstrips fabricated on the same membrane.

To see how the V_{PI} changes across different devices, three different suspended microstrip lines, each one segment long, had their phase shift extracted against biasing voltage, but with broader voltage steps, to see after what biasing value the segments are guaranteed to have switched. Their phase shift at 60 GHz versus biasing is plotted in Figure 21.

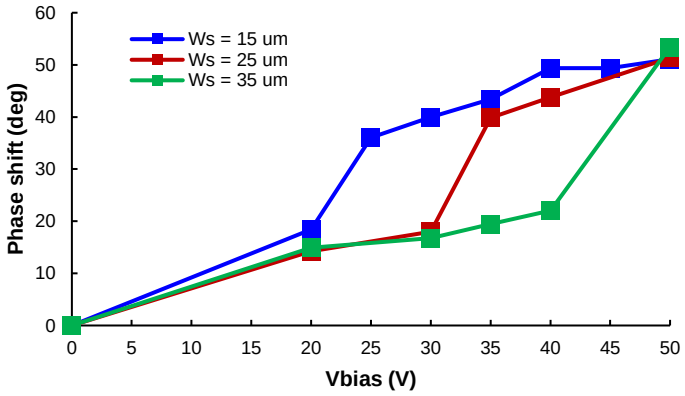


Figure 21 - Phase shift versus biasing voltage of three different LC 1-segment MnM phase shifters (N_S = 1), all having L_S = 500 µm. Source: author.

The MEMS switching in all these three devices can be clearly seen because of a steep phase jump. This jump happens between 20 V and 25 V for W_S = 15 µm, between 30 V and 35 V for W_S = 25 µm and, lastly, between 40 V and 50 V for W_S = 35 µm. Even though V_{PI} isn't a function of W_S, as indicated by equation ((5), other parameters such as residual stress in the suspended strip and the actual Young's module of the material do influence it. Nevertheless, these values show that a very large variation of V_{PI} is to be expected. So, for future measurements, a voltage of 50 V will be assumed for the switched state, because it is a guarantee that all suspended lines will have already switched.

2.2.2.5 LC performance

Having asserted the operating voltages of the LC MnM phase shifter, the pure LC performance was analyzed using the devices with sorter suspended lines (L_S = 250 µm and N_S = 4). Figure 22 shows the return loss and insertion loss of devices with W_S = 15 µm, 25 µm and 35 µm, respectively, and a comparison of the proposed model and EM simulation for the case W_S = 25 µm. The comparisons were made for the case of zero bias and for a biasing voltage of

20 V, which translate into the perpendicular and parallel LC molecules alignment, respectively. Likewise, the measurements were software de-embedded using the procedure described in section 2.2.1.3.

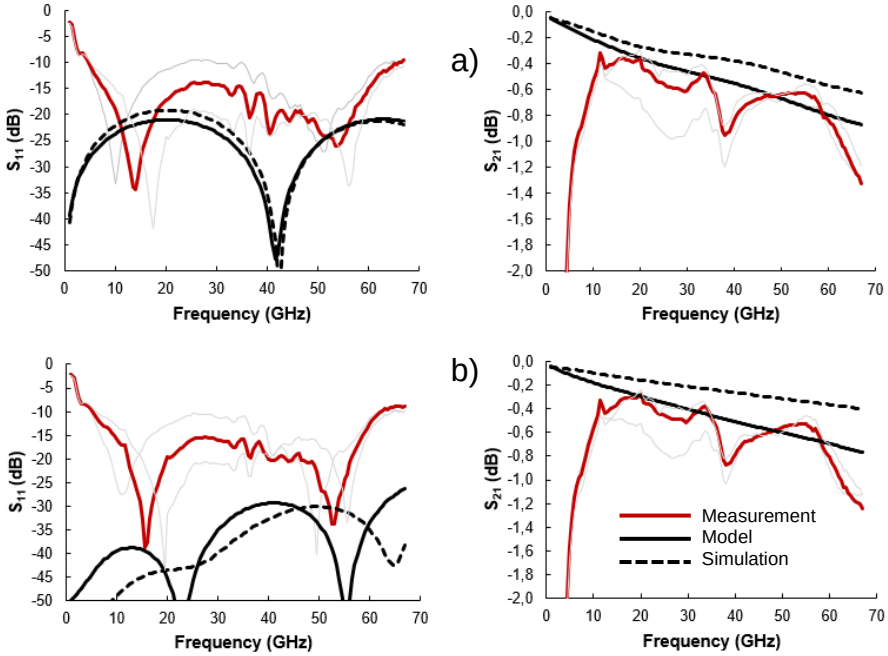


Figure 22 – Measured insertion loss and return loss of all LC-MnM phase shifters having L_s = 250 µm (light grey). In detail (red), the measurement of W_s = 25 µm is compared against the EM simulation (dashed black) and the proposed model (black). a) Comparison of return loss (right column) and insertion loss (left column) for 4 segments, W_s = 25 µm and L_s = 250 µm at zero bias condition. b) Same device, but now at V_{bias} = 20 V, higher than V_{LC_sat} . Source: author.

The agreement in the insertion loss regarding the measured data and the proposed model is quite good above 15 GHz for both 0 V and 20 V biasing, however for the return loss the agreement is not as good, and the reason for this is the capacitive de-embedding residual from the biasing pads. The agreement is better when comparing the EM simulations with the proposed model, even though the measured losses are higher. Table 9 contains the ε_{reff}, Z_C and α extracted from the measurements and from EM simulations, considering the suspended microstrip lines plus the anchoring parasitics.

Table 9 - Characteristic impedance, effective dielectric constant and attenuation constant of the LC-MnM phase shifter having Ws = 25 µm, Ls = 250µm and Ns = 4, extracted from measurement and compared against EM simulations.

	Measurement	**Simulation**	**Model (Figure 19)**
ε_{reff} **0V**	11.4	9.6	8.41
ε_{reff} **20V**	14.4	12.8	10.4
Z_C **0V**	55	56	57.2
Z_C **20V**	49	50	51.3

α 0V	0.56	0.44
α 20V	0.51	0.3

Anchoring parasitics			
	L_{ANCH} (pH)	**C_{ANCH} 0V (fF)**	**C_{ANCH} 20V (fF)**
W_S = 15 µm	3.58	2.61	2.96
W_S = 25 µm	2.53	3.31	3.7
W_S = 35 µm	2.41	3.89	4.3

Z_C is in very good agreement in all biasing conditions, however the ε_{reff} extracted from measurements is higher than what the model predicts in both biasing conditions. Even though the EM simulations indicate this is supposed to be the case, because of the parasitic effects from the anchoring sections, the drop in ε_{reff} is more significative. This would be an indicator that the excess capacitance after de-embedding is underestimated, probably because the LC flowed under the RF probes, adding extra capacitance in parallel with the DUT. However, the exact amount is hard to determine in simulation. As for the α, the LC adds its dielectric losses to the device, but the variation in α between biasing states in the measurement is smaller than expected from the simulations.

Figure 23 shows the α, phase shift and FOM extracted from measurement data for every structure presented in this subsection.

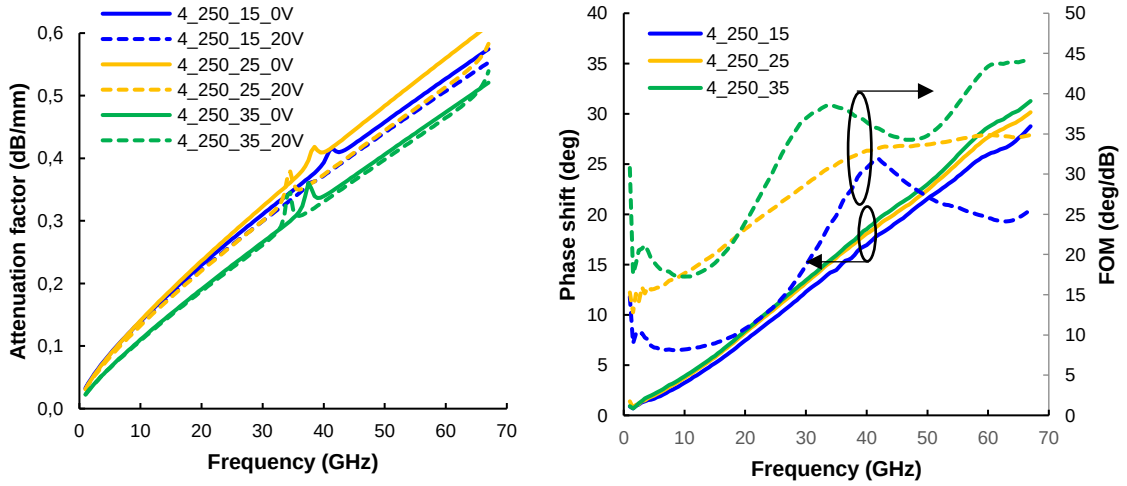


Figure 23 – Attenuation factor (left), phase shift and FOM (right) for the three LC-MnM phase shifters analyzed in this subsection. Source: author.

The average α for these devices at 60 GHz is 0.51 dB/mm, about the double than the average for the air-filled, suspended microstrip lines. The average phase shift observed at 60 GHz is 27.5°, which is fairly consistent for all the devices, increasing slightly with W_S. Given that the overall length of these phase shifters

is 1.35 mm, this average phase shift translates into a unit length phase shift of 20.4 °/mm. The FOM, however, does vary between devices and, because impedance mismatch, it also varies with frequency. The best case FOM for these devices was observed in the device whose W_S = 35 µm: 43.6 °/dB at 60 GHz for a phase shift of 29°.

2.2.2.6 MEMS performance

Having asserted the performance of the LC-created phase shift, now the phase shift created from the MEMS switching of the air-filled, suspended microstrip lines is investigated. As explained before, this section will deal with the devices with longer suspended regions (L_S = 500 µm).

Figure 24 shows the return loss and insertion loss of the devices that switched with V_{PI} under 90 V, and a comparison of the proposed model and EM simulation for the case W_S = 25 µm, N_S = 2. The comparisons were made for the case of zero bias and the completely switched state, which varied from device to device. Likewise, the measurements were software de-embedded using the procedure described in section 2.2.1.3.

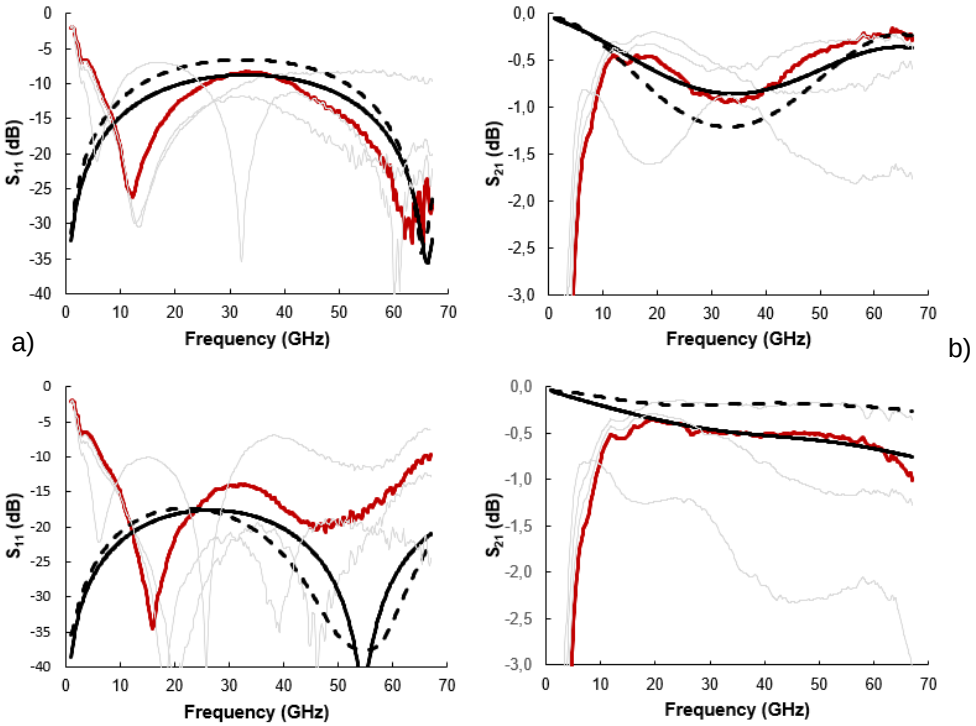


Figure 24 - Measured insertion loss and return loss of all suspended microstrip line, MEMS phase shifters having L_S = 250 µm (light grey). In detail (red), the measurement of W_S = 25 µm is compared against the EM simulation (dashed black) and the proposed model (black). a) Comparison of return loss (right column) and insertion loss (left column) for 4 segments, W_S = 25 µm, L_S = 500 µm and Ns = 2 at zero bias condition. b) Same device, but now at V_{BIAS} =

90 V, higher than V_{PI}. Source: author

The agreement in the insertion loss regarding the measured data and the proposed model is quite good above 15 GHz for both 0 V and maximum biasing. The air gap height in the simulation was assumed to be 1.25 µm, as this value resulted in the best agreement between simulation and measured response. Table 10 contains the ε_{reff}, Z_C and α extracted from the measurements and from EM simulations. The anchoring parasitics are the same as those contained in Table 5. Figure 25 shows the α, phase shift and FOM for three different suspended microstrip lines.

Table 10 – Characteristic impedance, effective dielectric constant and attenuation constant of the suspended line, MEMS phase shifter having Ws = 25 µm, Ls = 250µm and Ns = 4, extracted from measurement and compared against EM simulations.

	Measurement	**Simulation**
ε_{reff} **0 V**	4.8	4.6
ε_{reff} **90 V**	7.7	8.6
Z_C **0 V**	75	81
Z_C **90 V**	60	75
α **0V**	0.25	0.16
α **90 V**	0.57	0.2

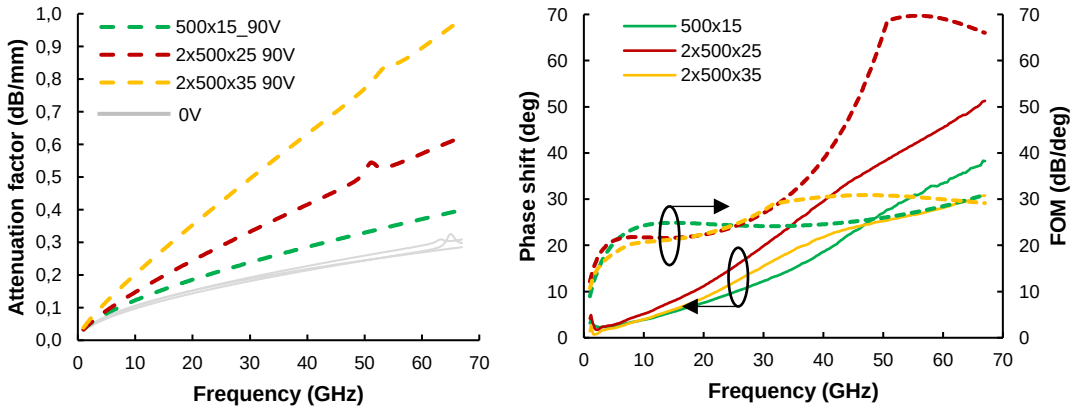


Figure 25 – Attenuation factor (left), phase shift and FOM (right) for the four suspended microstrip lines, MEMS phase shifters analyzed in this subsection. Source: author.

The α for the switched state at 60 GHz varies a lot from device to device, from 0.37 dB/mm on the 2x500x15 device to 0.90 dB/mm on the 2x500x35 device. The phase shift observed at 60 GHz varies between 31° on the 2x500x35 device to 45.5° on the 2x500x25 device. The cause for both effects is the same: leftover residue from the sacrificial photoresist. The 2x500x35 device has both the higher losses and the lowest phase shift, indicating that there is a thicker layer

of photoresist both adding more losses and limiting the switching performance. The best-performing phase-shifter, 2x500x25, has a normalized phase shift of 36 °/mm and a FOM of 69 °/dB, both at 60 GHz.

2.2.2.7 MEMS plus LC performance

The MEMS switching mechanism produces better-performing phase shifters than the pure LC biasing, at the cost of loss of continuous tuning and higher activation voltages. But, by combining both mechanisms, the performance of the device can be further improved, as the LC will lower the V_{PI} of the suspended microstrip lines and increase the phase shift. There are two ways to control the analog and digital tuning mechanisms independently: the first uses a single biasing supply to control both mechanisms, as $V_{PI} > V_{LC\_SAT}$; the second uses series capacitors to isolate different phase shifters, which are biased independently by two different biasing supplies. The first control method is investigated in this subsection.

Figure 26 shows the return loss and insertion loss, the phase shift and the FOM of a device of W_S = 25 µm, L_S = 500 µm and N_S = 4 for the unbiased case and for a biasing of 50 V, the fully-switched state. The measurements were software de-embedded using the procedure described in section 2.2.1.3.

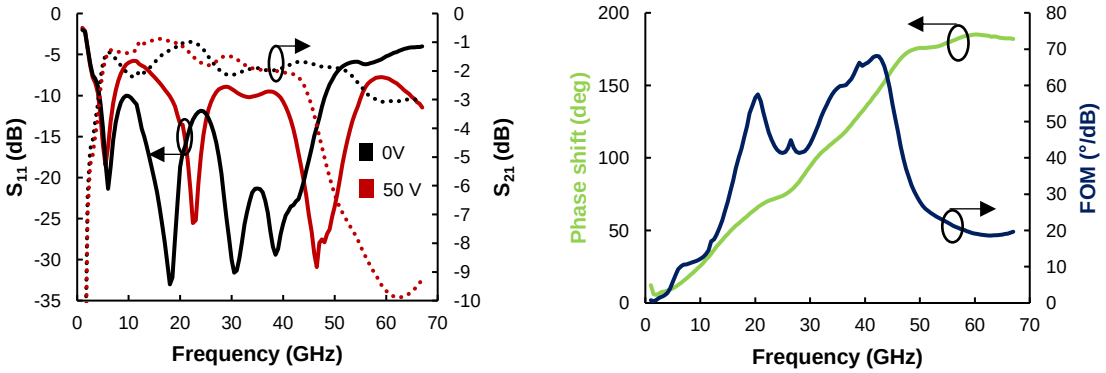


Figure 26 – Return loss and insertion loss (left), phase shift and FOM (right) for the LC-MnM MEMS phase shifter having W_S = 25 µm, L_S = 500 µm *and* N_S = *4. Source: author.*

Two noticeable effects can be observed. The first is the amount of phase shift that is generated, which amounts to 185° at 60 GHz on a device which is 2.4 mm long, translating to a normalized phase shift of 77 °/mm, the highest reported so far in this work, showing that indeed summing both mechanisms improves the overall phase shift. The second effect is a strong transmission zero

in the switched state at around 60 GHz, where S_{21} falls to -10 dB. This zero is caused by Bragg resonance, because of the local reflections between the now low-impedance suspended microstrip line and the higher impedance anchoring. The combination of four 500 µm – long suspended microstrip lines plus their 100-µm anchoring resonates at 62.5 GHz, an unfortunate coincidence. This Bragg resonance causes severe insertion loss in the phase shifter, which can be observed in the FOM plot: the FOM peaks at 68 °/dB at 42 GHz, before dropping sharply to 18.6 °/dB at 62.5 GHz.

To avoid exciting this resonance, the performance of the LC+MEMS phase shifter was evaluated using the 1-segment-long devices. Figure 27 shows the insertion loss and return loss of three single-segment devices with different W_S. The raw measurement data was de-embedded in ADS using the procedure explained in section 2.2.1.3.

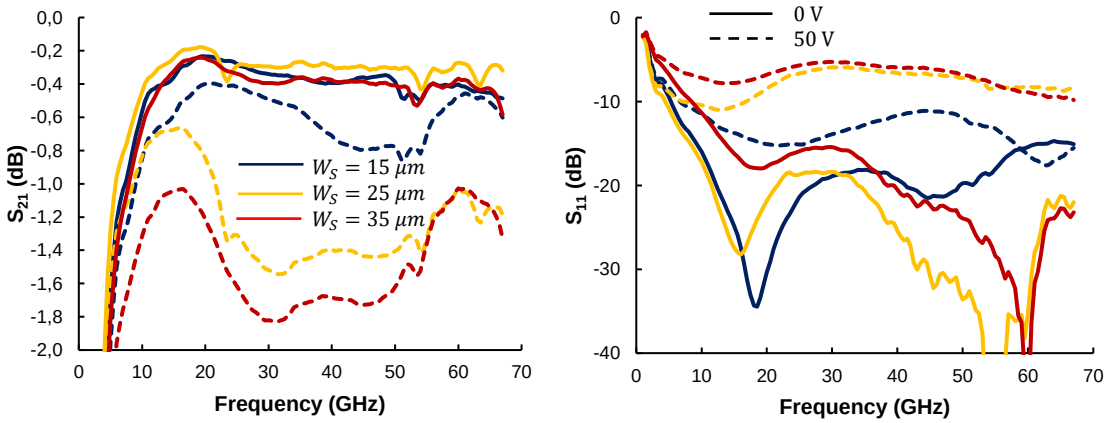


Figure 27 – Insertion loss (left) and return loss (right) for three different, single-segment LC-MnM MEMS phase shifters at zero bias and at V_{BIAS} = 50 V, larger than V_{PI} for all devices. Source: author.

The unbiased state suspended microstrip lines are all well-matched to 50 Ω, but they suffer from reflection losses caused by the severe drop in Z_C once the suspended microstrip lines are switched on. The exception appears to be the W_S = 15 µm case: the narrow line results in a less dramatic decrease in Z_C when switched, and the combination of unbiased LC inside the lower air cavity causes the Z_C to be in the vicinity of 60 Ω. Having assessed the insertion loss and reflection loss of these single-segment devices, Figure 28 presents the α, phase shift and FOM of these three devices.

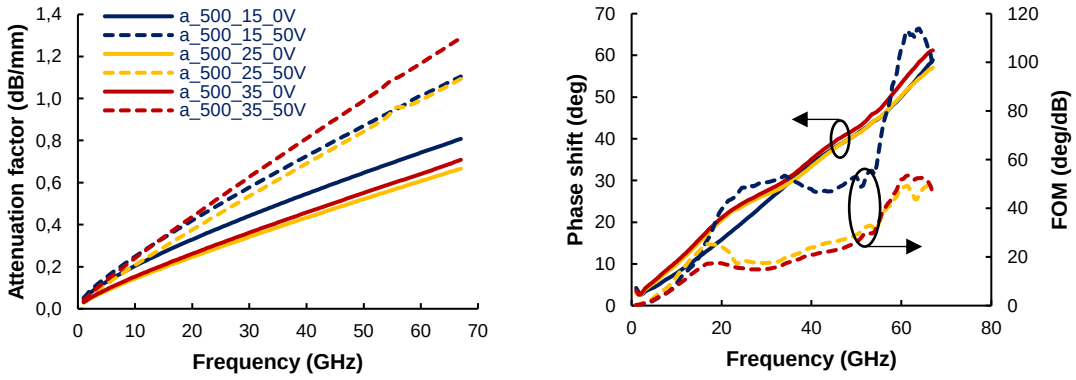


Figure 28 – Attenuation factor (left), phase shift and FOM (right) of the three, single-segment LC-MnM MEMS phase-shifters analyzed in this subsection. Source: author.

The α spread between devices is much smaller if compared to other multi-segment phase shifters reported in this work: the unbiased average α is 0.66 dB/mm, the fully switched average α is 1.1 dB/mm. The unbiased α is higher than the average α reported for the pure LC phase shifters in section 2.2.2.5, and also higher than the worst-case α of the pure MEMS phase shifters reported in section 2.2.2.6. However, when analyzing the phase shift and the FOM of these devices, it is where their performance shows its potential. The worst-case FOM at 60 GHz of these three phase shifters is 48 °/dB, and the best-case is at 108 °/dB. The FOM is rippled because of the impedance mismatch between the 50 Ω source and the device's own Z_c, but it does not obscure the fact that this device has the highest FOM reported in this work. The phase shift is very consistent, the average phase shift at 60 GHz being 51°. Taking the device length of 600 µm, the normalized phase shift is 85 °/mm.

2.2.3 CONCLUSIONS

In this chapter, it was presented the design, modelling, fabrication and characterization of a novel phase shifter based on a combination of devices and techniques. It uses a suspended, slow-wave microstrip line as a base structure for its compactness, thanks to the slow-wave effect, good propagation characteristics and the possibility to be used as a binary MEMS phase shifter. Then, by injecting LC in the volume between the suspended strip and the copper nanowires underneath, not only the necessary V_{PI} gets lowered by $\sqrt{\varepsilon_{r\_LC}}$, but the phase shifter gains two very important features: the first is continuous phase change, by applying a biasing voltage smaller than V_{PI}, but higher than the V_{FTH} of the LC; the second is a performance boost of its FOM, which is better than

either mechanism in separate. The best FOM for the pure LC phase shift was reported as 43.6 °/dB, and 69 °/dB for the pure MEMS phase shift: for the combined effects, the best reported FOM is 108 °/dB, all values extracted at 60 GHz. This fact shows the strong potential of this phase shifter topology. To compare the performance of the phase-shifter, their results will be placed against those of the state-of-the-art described in Section 1.3.1. This comparison is shown in Table 11.

Table 11 - Comparison of the phase-shiftes designed in this thesis against the state-of-the art. The results in bold are those designed in this thesis.

Ref.	**Tech/type**	$Freq$ (GHz)	**Tuning range** (º)	**FOM** (º/dB)	**Tuning method**
[12]	CMOS/reflection	50-65	87	11	Continuous
[13]	CMOS/reflection	54-66	90 (11.25)	13	3-bit binary
[15]	BST/loaded line	60	150	22	Continuous
[17]	LC/loaded line	76	96	42	Continuous
[18]	CMOS+LC/loaded line	45	275	52	Continuous
[19]	LC/loaded line	30-34	60	10	Continuous
Section 2.2.2.5	**LC/loaded line**	**60**	**29**	**43.6**	**Continuous**
Section 2.2.2.7	**LC+MEMS/loaded line**	**60**	**51**	**108**	**1-bit binary**

Future work suggestions include the optimization of this LC-MnM phase shifter to reduce the Z_C variation between unbiased and switched states, thus maximizing the final FOM of the device. Also, given the fact that V_{PI} is a sole function of the suspended line's L_S, this value can be tuned to create a multi-bit discrete phase shifter by putting a number of suspended microstrip line segments in series, each with a slightly different L_S, and thus V_{PI}, so that each segment can switch independently from the others. Also, a final suggestion would be to create a LC container around the device, to prevent the LC flowing into the RF probes, which create measurement and de-embedding errors, and also to allow a more uniform performance between different measurement runs.

3 CMOS E-BAND VOLTAGE-CONTROLLED OSCILLATORS

In order to satisfy the needs for increasing the frequency band of wireless communications, and to accommodate the ever-increasing need for higher data throughput, foundries have been working on the improvement of Si-based CMOS technologies for RF and mmW applications. In contrast with digital, low-frequency analog and RF, knowing only information about the front-end-of-line (FEOL) is not enough for a mmW designer, as the layering and disposition of the metallic and dielectric layers of the back-end-of-line (BEOL) is very important to design passive devices such as inductors and transmission lines.

There are two major wafer structures in commercially-available CMOS technologies: the Silicon-on-Insulator (SOI) and the classical, bulk Si. The bulk Si wafer is made of monocrystalline, lightly-doped, P-type Si a few hundred micrometers-thick where the active devices are patterned on top side by photolithographic processes. The SOI adds a thin layer of Si dioxide on top of a bulk wafer, and then a Si layer a few nanometers-thick is deposited on top of the oxide, where the active devices are patterned. The thickness of the Si layer determines if the depletion layer from the devices own functioning will cause it to fully deplete (FD-SOI) or only partially deplete (PD-SOI). The combination of the thin, depleted Si and the buried oxide layer results in performance improvement of FD-SOI-based MOSFETs over the bulk-based MOSFETs.

Bulk CMOS processes have their own advantages: first, bulk wafers are more easily available and, thus, lower cost; second, the thickness of the Si wafer enables the fabrication of devices requiring deep N or P wells, such as bipolar junction transistors (BJT) and diodes. Also, depending on the process, the fabrication of bipolar devices designed for high-frequency applications, such as Si-germanium heterojunction bipolar transistors (SiGe HBTs) is possible, at the cost of increased process complexity and cost. Thus, bulk CMOS is the technology of choice for low-cost, commercial applications.

The FEOL of a mmW-oriented CMOS technology must offer two main assets to designers: the first is high-speed transistors, with unit gain frequency (f_t) and maximum frequency (f_{max}) above the desired operating frequency; the second is robust, measurement-based SPICE model of the devices to allow accurate simulations and designs at mmW.

The first asset is a function of the device physics (field effect or bipolar) and of the technological node. This is more or less dealt with because of the miniaturization drive of digital applications, where the gate length of MOSFETs was already driven to the deep, sub-micrometer region that ensures mm-wave compatible f_t and f_{max}. N-channel MOSFET f_t and f_{max} reached the range of tens of GHz since the mid 90's with the 250-nm CMOS node, and reached the 100 GHz range in the beginning of the 00's, with the 90-nm node. This can be seen in the f_t and f_{max} curves presented in Figure 29 for CMOS processes between 250 nm and 90 nm.

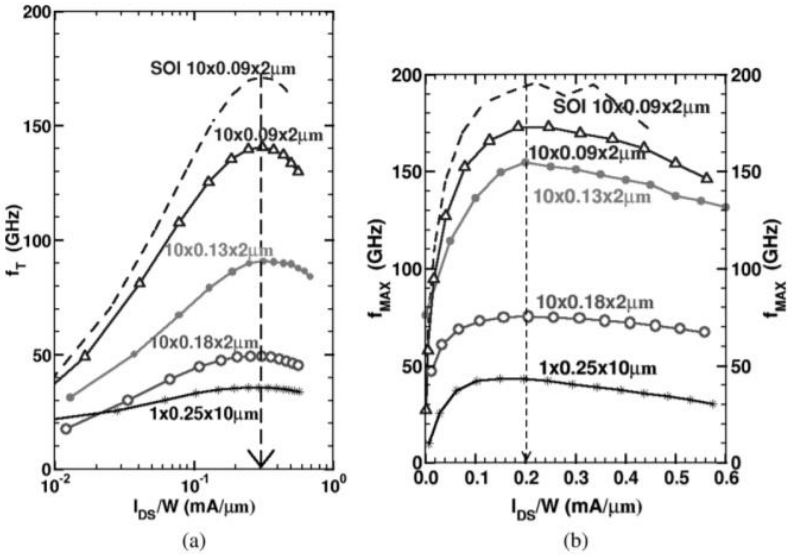


Figure 29 - f_t (a) and f_{max} (b) of n-channel MOSFETs of different CMOS technological nodes versus drain current density. The nodes are: 250 nm, 180 nm, 130 nm and 90 nm bulk processes. The 90 nm, SOI process is also included for comparison. Source: [55]

Recently, with 5-nm nodes, the f_{max} for FinFET MOS transistors reached the 600 GHz mark [56], thus demonstrating the state of Si-based devices. SiGe HBTs do show improved RF performance over Si MOSFETs, specifically higher f_t and f_{max} and lower noise figure. Considering f_t as a figure of merit, a SiGe HBT has comparable f_t performance to n-channel MOSFETs at roughly twice the minimum feature size, that is, a n-channel MOSFET whose channel length is 90 nm has roughly the same f_t as a npn HBT whose emitter length is 180 nm. Figure 30 shows the evolution of f_t of SiGe HBTs, Si MOSFETs and of other III-V device technologies from 2005 and 2013, indicating that Si MOSFETs are at least competitive in terms of speed against III-V devices and against SiGe HBTs. III-V technologies include semiconductor materials such as gallium arsenide

(GaAs), indium phosphide (InP) and gallium nitride (GaN).

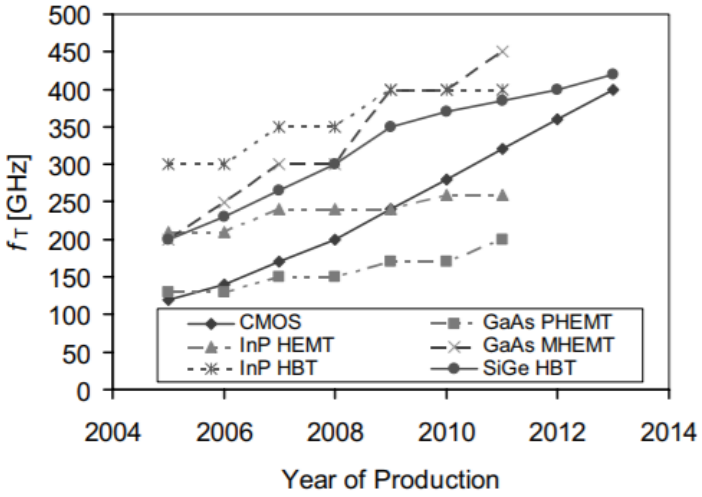


Figure 30 - f_t of Si-based MOSFETs, SiGe HBTs and III-V transistors between 2005 and 2013. Source: [55]

In the BEOL, however, is where the needs of digital and mm-wave designs conflict. In digital applications, that make the majority of the IC production worldwide, metal layers have to be thin, to ensure high integration density, and dielectric layers have to be equally thin and low-K, to ensure low capacitive coupling and low signal propagation delays. BEOLs of digital-oriented technologies are usually thin, with only a few micrometers separating the top and bottom metals. These characteristics are even more apparent in more advanced technologies, where the trend is to reduce metal, dielectric and BEOL thicknesses. Mm-wave applications, however, need thicker metals and BEOLs with equally thicker dielectric layers to ensure high Q-factor of larger passive devices such as transmission lines and planar inductors. Every extra micrometer of top-bottom metal separation leads to large improvement in losses and Q-factor.

The emergence of the market needs for monolithic, mm-wave circuits or mixed-signal mm-wave circuits has forced foundries to adapt the BEOLs of older technologies to accommodate the needs of RF designs, including one or more thicker metal layers, higher-K dielectrics for the upper part of the BEOL, and include RF-characterized inductor and capacitor parametric cells (PCells). Figure 31 shows two different ways a BEOL of a standard, digital CMOS technology can be adapted for mmW needs: the first is re-designing the metal and dielectric layers, increasing thicknesses and distances of the topmost layers, as can be seen by comparison of the standard 130-nm CMOS and the BiCMOS 9MW, 130-nm technology, both from ST Microelectronics; the second is adding thicker metal

layers on top of the BEOL, thus keeping the high-integration capabilities of the lower metals while adding the low-loss metal that mm-wave passive devices need, which can be seen by comparing the BEOL of ST Microelectronics' 65-nm CMOS process and the 55-nm BiCMOS process.

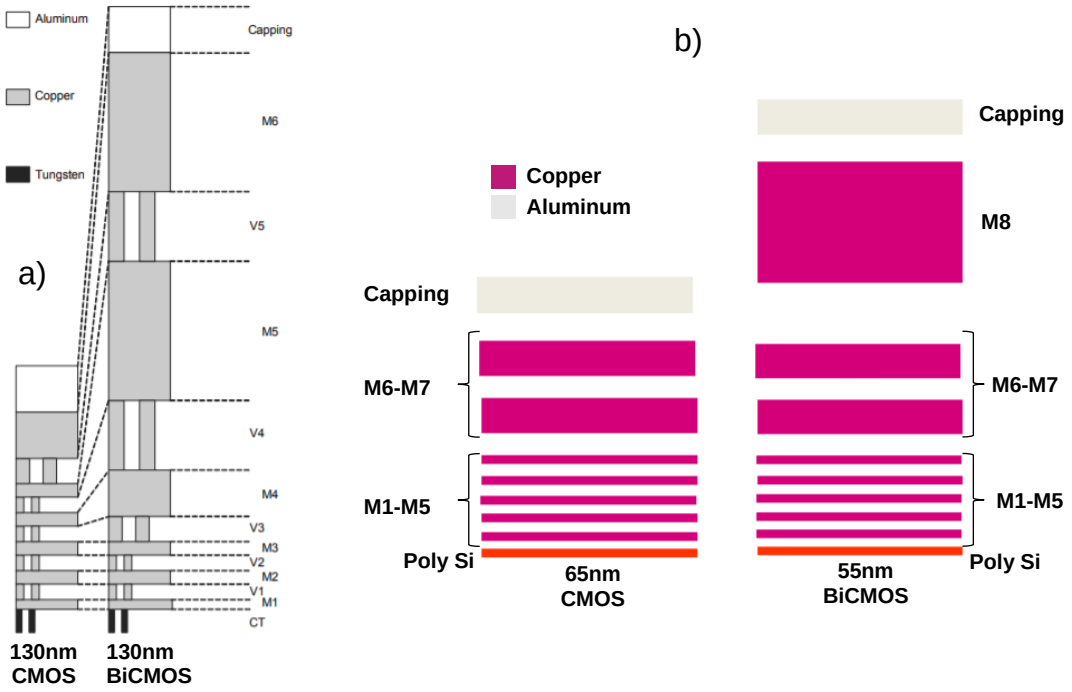


Figure 31 – Comparison between the BEOLs of standard, digital-oriented CMOS, and of mm-wave-oriented BiCMOS technologies. a) 130-nm CMOS versus 130-nm BiCMOS and b) 65-nm CMOS versus 55-nm BiCMOS. Source: author.

In [57], a comparative study was conducted regarding the performance of W-band transformers and the pros and cons of different transformer topologies in two different BEOLs for the same technological node. The technology in question is a 28 nm FD-SOI process by ST Microelectronics using the standard, 8-layer digital BEOL and a mm-wave optimized BEOL, featuring 8 layers of thicker metals and dielectrics. The study found that the standard BEOL can be competitive in certain contexts where the fringing capacitance is important, as the thicker metals from the mm-wave BEOL do increase the fringing fields and capacitive coupling between metallic strips laid out in the same layer. However, the added distance between the top layers and the substrate does decrease the losses, as well as the thicker metals do reduce ohmic losses, especially for single planar inductors.

3.1 TECHNOLOGY OF CHOICE: STM 55-NM BICMOS

In this context, the technology of choice to realize the designs of the E-band (71 GHz - 76 GHz, 81 GHz - 86 GHz) oscillators is the 55-nm BiCMOS technology from ST Microelectronics [58]. This technology is an evolution and optimization from a core 65-nm CMOS technology, having in sight the needs of RF and mm-wave applications, and the latest iteration of ST Microelectronics' bulk BiCMOS technologies aimed for mmW.

3.1.1 FRONT-END CAPABILITIES

This technology offers RF-optimized MOSFETs, accumulation-type MOS varactors, high-resistance to low-resistance resistors, PIN diodes and npn, SiGe HBTs, as well as native bipolar junction transistors (BJTs) and pn junction diodes and high-density digital cells, I/O devices, ESD protection, etc.

The n-channel and p-channel RF MOSFETs offers greater design flexibility and accuracy thanks to their robust SPICE model. The PCell layout employs substrate guard-rings, techniques to reduce gate resistance, and by allowing a multi-finger layout, also reduce drain and source contact resistances. Discounting the effects of interconnection parasitics from the PCell, these RF MOSFETs have peak f_t > 150 GHz and peak f_{max} ~ 200 GHz, thus being well-suited for E-band applications.

The accumulation-type MOS varactors come in two different types, namely thin and thick gate oxide devices. These devices come as PCells offering good design flexibility and including some features to simplify the layout, such as substrate guard rings.

The polysilicon resistors offered by this technology come in various different types, such as silicided, n+ resistors (lower sheet resistance), p+ and n+ unsilicided polysilicon resistors, p+ active region resistors and high-resistivity, unsilicided polysilicon resistors (higher sheet resistance). These resistors come with accurate RF modelling that take into consideration capacitive coupling to substrate and other higher-order effects.

The PIN diodes available at this time are experimental in nature, however they do show promising results. No Si-based SPICE model is available, and the PCell is still going through layout optimization.

The npn, SiGe HBTs are available in three different types: high-speed, high-

voltage and medium voltage. The high-speed HBTs are optimized for mmW and have measured f_t > 320 GHz and f_{max} > 390 GHz, thus enabling designs at higher operating bands inside mmW. These devices are properly modelled with accurate SPICE models for high frequency and other higher order effects, such as self-heating.

For the sake of the E-band VCO designs, the components of interest are the n-channel RF MOSFETs, the MOS varactors and the PIN diodes.

3.1.2 BACK-END CAPABILITIES

The BEOL of this technology is composed of eight copper layers, plus aluminum capping, and offers monolithic high-integration capability and low-loss RF device. The basic BEOL stack is presented in Figure 32.

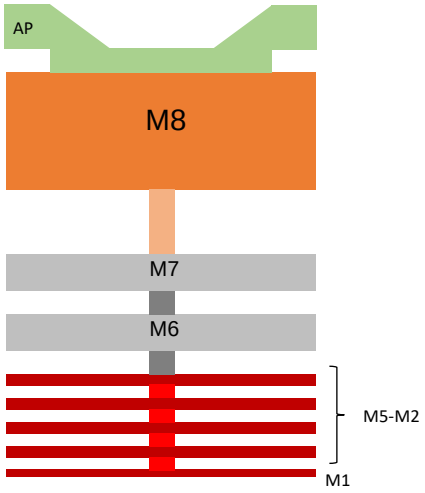


Figure 32 - The Back-end of line stack of the 55-nm BiCMOS technology, showing the metallic layers and vias. Source: author.

The thin lower metals (M1-M5) are enveloped by low-K dielectrics, and aimed at the high-density digital cells and transistor-level interconnections. The intermediate metals (M6-M7) are thicker and are used in the standard CMOS process for clock and power distribution in digital applications, and as low-loss interconnections in multi-turn inductors in RF applications. The topmost metal, M8, is an ultra-thick layer, and is recommended for routing the signal strips of transmission lines and inductors, as well as routing power lines because of the higher current density they can withstand because of the higher thickness. The added distance between M8 and M1, compounded with the greater thickness of the M8 layer, enables microstrip lines with lower attenuation factor. The aluminum caping layer (AP) is used to realize contacts for probes and they can be also used

to make RF components.

The PDK offers microstrip line PCells, as well as planar, spiral inductors and RF-oriented, high-density, mesh metal-oxide-metal (MOM) capacitors. The microstrip lines come in two different types, single-ended and differential, both having a wide range of characteristic impedances. The planar inductors come in many different types, but in two main families: lower frequency, higher inductance inductors and lower inductance, higher frequency, mm-wave inductors. The MOM capacitors available come in two different types: with and without patterned ground shield. The MOM capacitors are the only capacitor PCell that are accurately modelled at mmW. Inductors and microstrip lines do include accurate, high-frequency SPICE models.

One important aspect of the STM 55-nm BiCMOS technology is the optical shrink employed in the mask generation. Since this technology uses the same design environment as the 65-nm CMOS technology whom it derives, all physical dimensions in layout receive a dimension shrink of 0.9 times during mask generation. The BEOL PCells are already adjusted for this, however all custom devices must compensate for the shrinking.

3.2 SLOW-WAVE COPLANAR STRIPLINES (S-CPS)

Even though the BEOL solves the problem of interconnection losses and ohmic losses in larger RF devices, there is still the problem that comes from the losses in the Si substrate.

In bulk CMOS it is necessary to use low resistivity Si wafers because of the necessity for latch-up immunity between the n well of p-channel devices and the p well of n-channel devices in compact CMOS circuits. However, the low resistivity of the Si increases the losses in the substrate due to eddy currents. These extra losses degrade the Q-factor of planar inductors and of unshielded transmission lines, such as coplanar waveguide (CPW) and coplanar stripline (CPS), and planar inductors. The use of patterned ground shields underneath inductors does help mitigate the substrate eddy current losses, but in higher frequencies the ohmic losses from the shield degrades the Q-factor of the inductors, as indicated in [59].

One alternative to avoid excessive losses in transmission lines is to use microstrip lines or grounded CPWs (GCPW), as the continuous ground plane

itself shields the RF fields from the bulk Si. However, because the separation between the ground plane and signal strip has to be maximized to ensure good Q-factor, the ground plane must be made out of the lowest, thinnest metals of the BEOL, increasing the ohmic losses of the transmission line. Also, this solution might not be the most commercially-effective solution since the lines' ε_{reff} is low, limited by the low-K dielectrics own ε_r, leading to physically long transmission lines. This results in large surface area occupation, because of the lateral clearance to avoid unwanted coupling to other devices or to the ground tiling.

Another, more practical solution is to use shielded transmission lines, such as the shielded, or slow-wave CPW (S-CPW) [60]. In this topology, the three conductors of a classical CPW, the signal and the two coplanar ground strips, are shielded from the bulk Si underneath by a periodical, floating array of metallic fingers. The RF electric field gets trapped between the floating shield and the signal strips, thus avoiding most of the ohmic losses in the bulk Si. However, because of the non-ferromagnetic nature of the materials involved in standard CMOS processes, the RF magnetic fields remain largely undisturbed. The confinement of the RF electric field causes the increase on the unit length capacitance of the transmission line, leaving the unit length inductance unchanged, leads to the decrease of the transmission line's phase velocity, and consequently, the slow-wave effect. The slow-wave effect has the advantageous result of reducing the required physical length of a transmission line to realize a given electrical length, thus leading to miniaturization. Also, it leads to reducing the Z_C of a transmission line for a given strip width, widening the Z_C range of the technology. Figure 33 shows the basic structure of a S-CPW, as well as its cross-section, comparing the electric and magnetic field distribution between a CPW and a S-CPW.

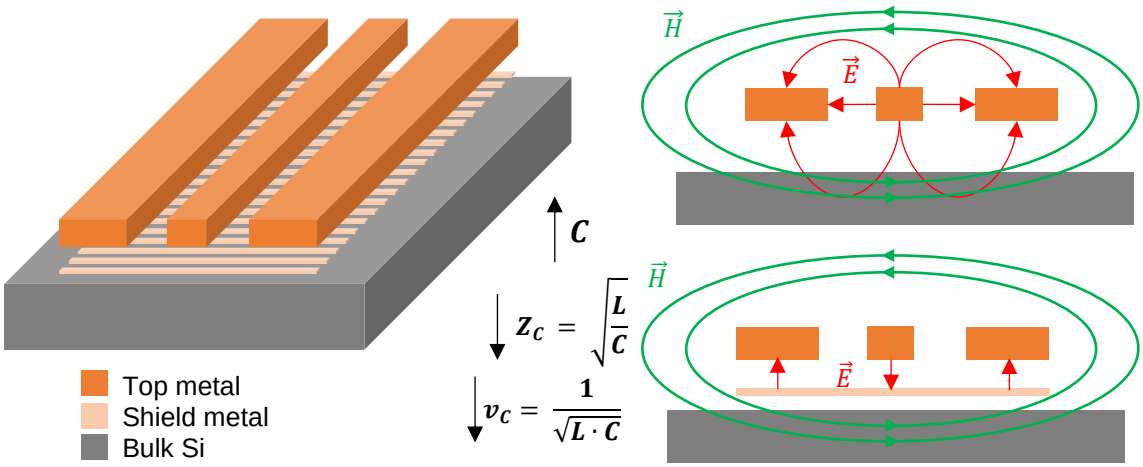


Figure 33 – The basic structure of a S-CPW. Source: author.

Now, if one of the ground strips is eliminated, the resulting structure is called a shielded coplanar stripline (S-CPS) [61]. The working principle is the same of the S-CPW, maintaining all the advantages of the S-CPW over unshielded transmission line topologies, being more compact at the cost of reduced noise immunity. And, because of the absence of the ground strips, the S-CPS offers more design flexibility to design distributed differential devices, such as inductors and resonators.

The S-CPS is inherently a single-ended transmission line topology, having one signal strip and one return, or ground, strip. The basic structure of the S-CPS, its RLRC electrical model and the design parameters are presented in Figure 34.

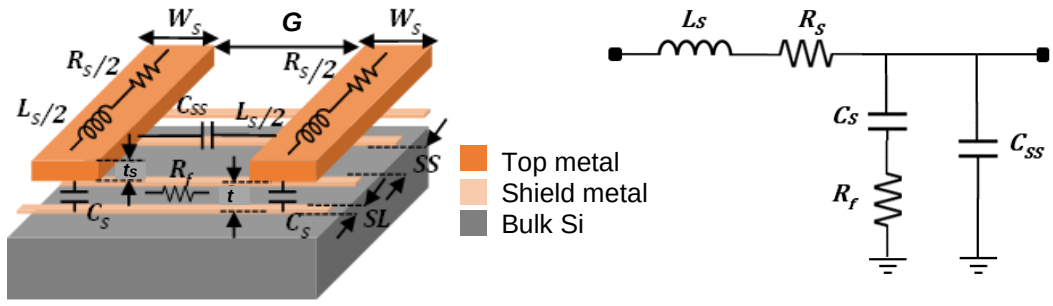


Figure 34 – Basic S-CPS structure and its equivalent, lumped electrical model. Source: author.

The strips have width W_S and thickness t_S, being spaced by the gap G. The floating ribbons have widths SL and pitch SS. The separation between strips and the shield is t. All model elements are supposed to be unit length. The equivalent model is based on the S-CPW model reported in [62]. The model reflects the

structure of the transmission line, modelling the transmission parameters and the loss mechanisms. The capacitive elements, the strip to shield capacitance (C_S) and the inter-strip capacitance (C_{SS}) are calculated in the same way as described in [61]. The strip series resistance (R_S) is calculated as described in [63], and the strip series inductance (L_S) is calculated using the same method described in [64], but using the following modification because of the difference in number of ground conductors on the S-CPS and S-CPW:

$$L_S = (M_{sisi} - M_{sisj})/2. \tag{7}$$

where L_s is the strip self-inductance of the transmission line, M_{sisi} is the partial mutual inductance of one of the strips, and M_{sisj} is the cross mutual inductance between both strips. The shield resistance (R_f) is calculated as being the equivalent resistance of each finger, considering the skin effect for the desired frequency, divided by the number of fingers in the desired length.

This model adequately represents the propagation effects of the transmission line when one of the conductor strips is taken as reference. However, if the strips are asymmetrical, or if the S-CPS is used to implement a differential device, such as a center-tapped inductor, it is necessary to present more information about the actual transmission line structure to better reflect the behavior of the device. To this end, the individual L_S, R_S and C_S are represented as shown in Figure 35, where an asymmetrical S-CPS is shown with all its individual model components.

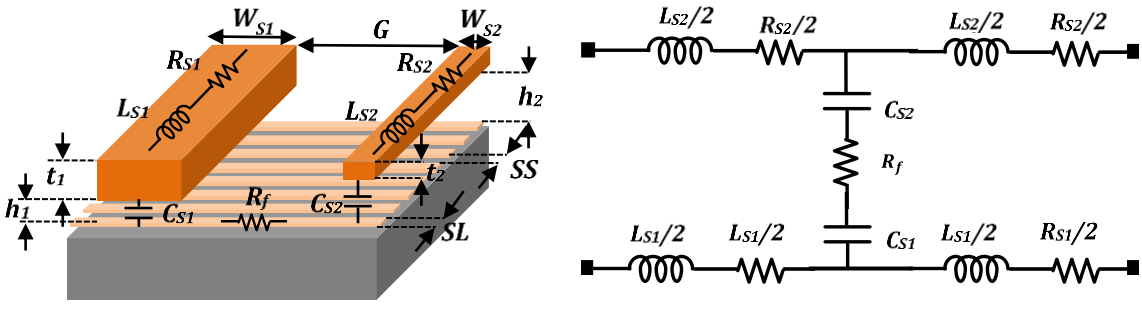


Figure 35 – A more general structure for the S-CPS, showing signal strip asymmetry, which is added into the lumped model in the form of asymmetrical series inductance and resistance and shunt capacitance. Source: author.

R_{S1}, R_{S2}, C_{S1} and C_{S2} are the series resistance and shunt capacitance of each strip, numbered as 1 and 2. L_{S1} and L_{S2} are the strip 1 and 2 self-inductances.

These values are different between the strips to represent the different current and voltage distribution across the device, which models the different electric and magnetic fields distribution in each strip. The method for computing the resistances and capacitances remain unchanged, however L_{S1} and L_{S2} are calculated as:

$$L_{Si} = M_{sisi} - M_{sisj},\ i,j \in [1,2]. \quad (8)$$

This more complete model will be used as basis for the resonators designed in the following sections, as it can be used simultaneously in transient/harmonic balance and S-parameter simulations.

The shielding provided by the floating ribbons drastically reduces the losses of the transmission line, and increases the Q-factor from structures that uses the same topology. This reduction in losses can be seen by calculating the Q-factor of the transmission lines and comparing it against unshielded transmission lines. In Figure 36 the simulated Q-factor for S-CPS is compared against the unshielded CPS and traditional microstrip lines. The transmission lines were designed to have the same Z_C = 50 Ω. At 80 GHz, the Q-factor of the S-CPS is about 40, which is more than the double of a microstrip line and the effect of the shielding is more emphasized if the S-CPS is compared against the unshielded CPS.

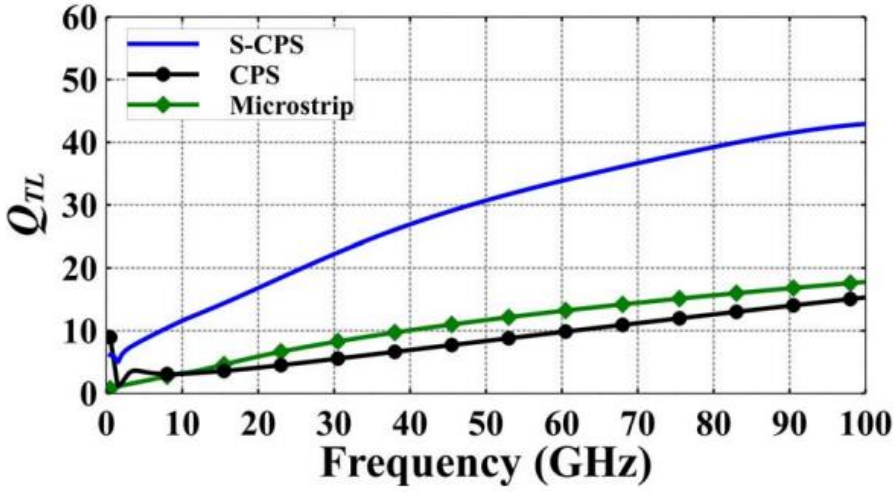


Figure 36 - Quality factor of three different transmission line topologies: Slow-wave Coplanar Stripline, Coplanar Stripline without shielding and microstrip line. Source: [65]

The next sections present some VCO designs using the S-CPS topology to realize a tunable resonator. Each design presents an optimization step of either the resonator or the design, pursuing better understanding of the structure and better performance.

3.3 STANDING-WAVE OSCILLATOR BASED ON DISTRIBUTED S-CPS RESONATOR

In this section, the basic structure for the distributed, tunable S-CPS resonator is presented, as well as its equivalent electrical model and all relevant parasitic components. The oscillator design flow is presented as well, covering all the important components and devices. The goal of this design was to arrive at an optimized S-CPS structure, in an effort to minimize tank losses. The next subsections explain the main building blocks of the proposed VCO, as well as the design procedure for each block and for the complete VCO.

3.3.1 DISTRIBUTED S-CPS RESONATOR

The resonator is the core of every VCO design in more than one way. Not only it will set the frequency tuning range (FTR) and the central oscillating frequency (F_{OSC}) of the VCO, but its equivalent losses and Q-factor will directly influence the phase noise (PN) performance of the VCO, and its DC power consumption. It will, thus, set the VCO performance.

The proposed tunable, distributed S-CPS resonator takes place of the inductive and capacitive elements of the classical, parallel inductor-varactor tank circuit. The capacitive element is distributed across the S-CPS distributed inductor to create a loaded-line phase shifter. They are connected between the strips and the shield, controlling the C_S, thus changing the phase velocity. And if the S-CPS resonator implements a λ/4 resonator, the resonant frequency of the circuit can be changed, so a variable tank circuit is created.

The reasoning behind this topology is the loss reduction of the inductive part and of the capacitive part of the resonator simultaneously. First, consider the inductive element. Classically, in monolithic CMOS VCOs, the inductor is realized by spiral, planar inductors. These inductors use a multi-turn strip and an optional patterned ground plane. Now, an inductor synthesized with a short-terminated length of S-CPS draws from the advantage of better shielding from the substrate and lower shield loss when compared to the planar inductor. This can be verified if the Q-factor of a planar inductor is compared to the Q-factor of a S-CPS inductor, both having the same equivalent inductance (L_{eq}) at a given frequency. In Figure 37, the L_{eq} and Q-factor of an inductor PCell from the 55-nm BiCMOS

technology and of an equivalent, S-CPS-based inductor are compared. The data from the S-CPS inductor are obtained from the model presented in Figure 35 and from EM simulations carried out in Ansys HFSS. Both inductances were designed to have L_{eq} = 107 pH at 80 GHz, as part of the design of a 77 GHz VCO [53].

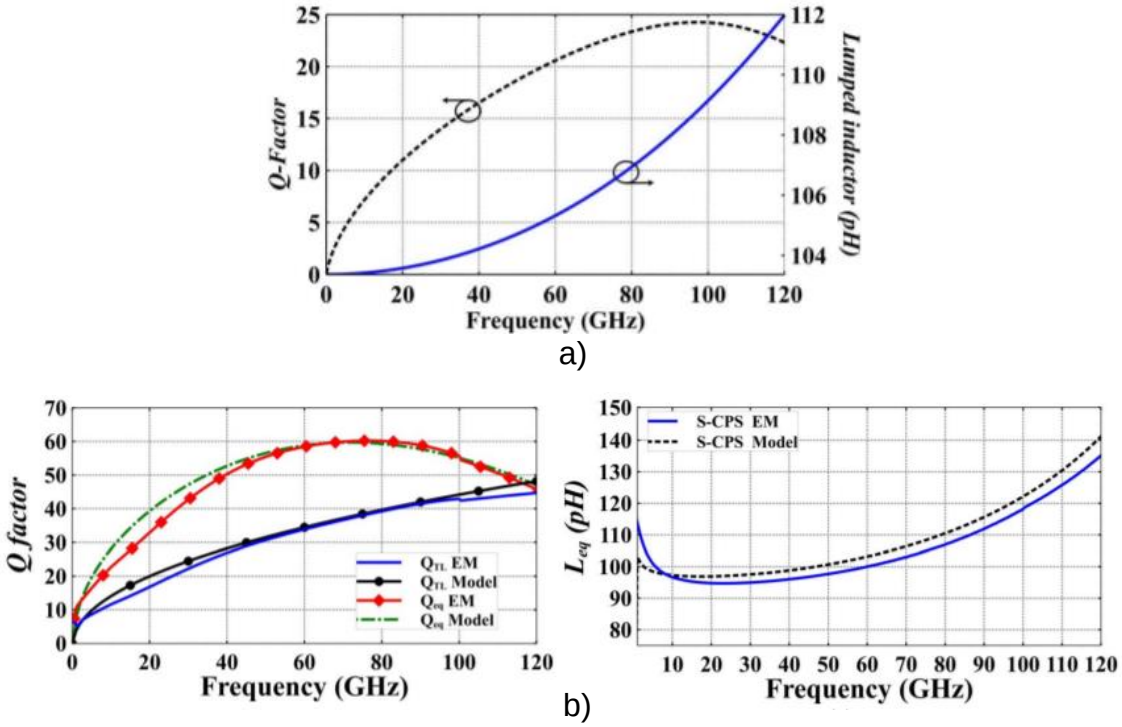


Figure 37 – Comparison of the quality factor of PCell inductors (a), and S-CPS-based inductors (b), both having the same equivalent inductance of 107 pH at 80 GHz . Source: [53]

The Q-factor of the distributed inductor is expressed in terms of its L_{eq} and equivalent losses, as a traditional inductor would be. However, the Q-factor can also be expressed in terms of the propagation characteristics of the S-CPS.

It can be seen the dramatic improvement in Q-factor coming from using S-CPS to implement inductors. The Q-factor of the S-CPS inductor at 80 GHz, shown in Figure 37 b), is around 60, compared to the PCell inductor, whose Q-factor is close to 22, as shown in Figure 37 a).

Now, concerning the capacitive part of the resonator. The classical inductor-varactor tank uses a large, lumped accumulation-type MOS varactor to realize the variable capacitance. Losses on accumulation-type MOS varactors follow a more or less inverse relation with its channel area, and, thus, with the nominal capacitance [23]. Thus, smaller varactors have higher Q-factor than larger varactors. However, for very small varactors, the intrinsic, PCell interconnection parasitics dominate the losses, dropping the Q-factor, so there should be a range

of varactor sizes that has the overall highest Q-factor. The varactor capacitance tuning range, TR, however, is proportional to the channel length. The TR is hereby defined as:

$$TR = \frac{C_{max} - C_{min}}{C_{nominal}} \tag{9}$$

Also, the losses in accumulation-type MOS varactors vary with biasing, as shown in Figure 38, where the capacitance and Q-factor for a thick-oxide, PCell varactor is plotted against the biasing voltage between gate and substrate terminals. The gate is tied at 1.2 V and the biasing voltage is applied to the substrate terminal via a RF choke, realized by a 62 kΩ high-resistivity unsilicided polysilicon resistor. The varactor has a nominal, central capacitance of 4.9 fF.

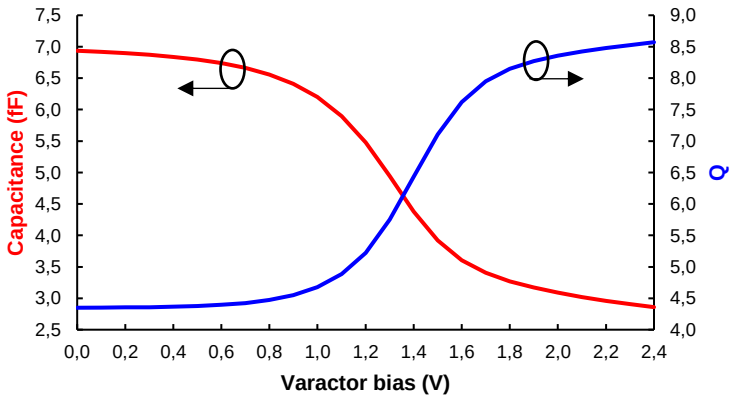


Figure 38 - Accumulation-type MOS varactor capacitance and Q-factor versus the biasing voltage. Source: author.

The design variables for PCell MOS varactors in the 55-nm BiCMOS technology are: finger, or channel, length (L_f) and width (W_f), number of fingers (nf) and number of PCells in parallel ($nbcell$). Both nf and $nbcell$ act as multiplying factors for the device capacitance, however, because increasing nf results in Q-factor drop, only $nbcell$ was used. Thus, for every varactor considered from now on, nf = 1. The TR and Q-factor, simulated at 80 GHz, of a single varactor, $nbcell$ = 1, in function of W_f and L_f, are presented in Figure 39.

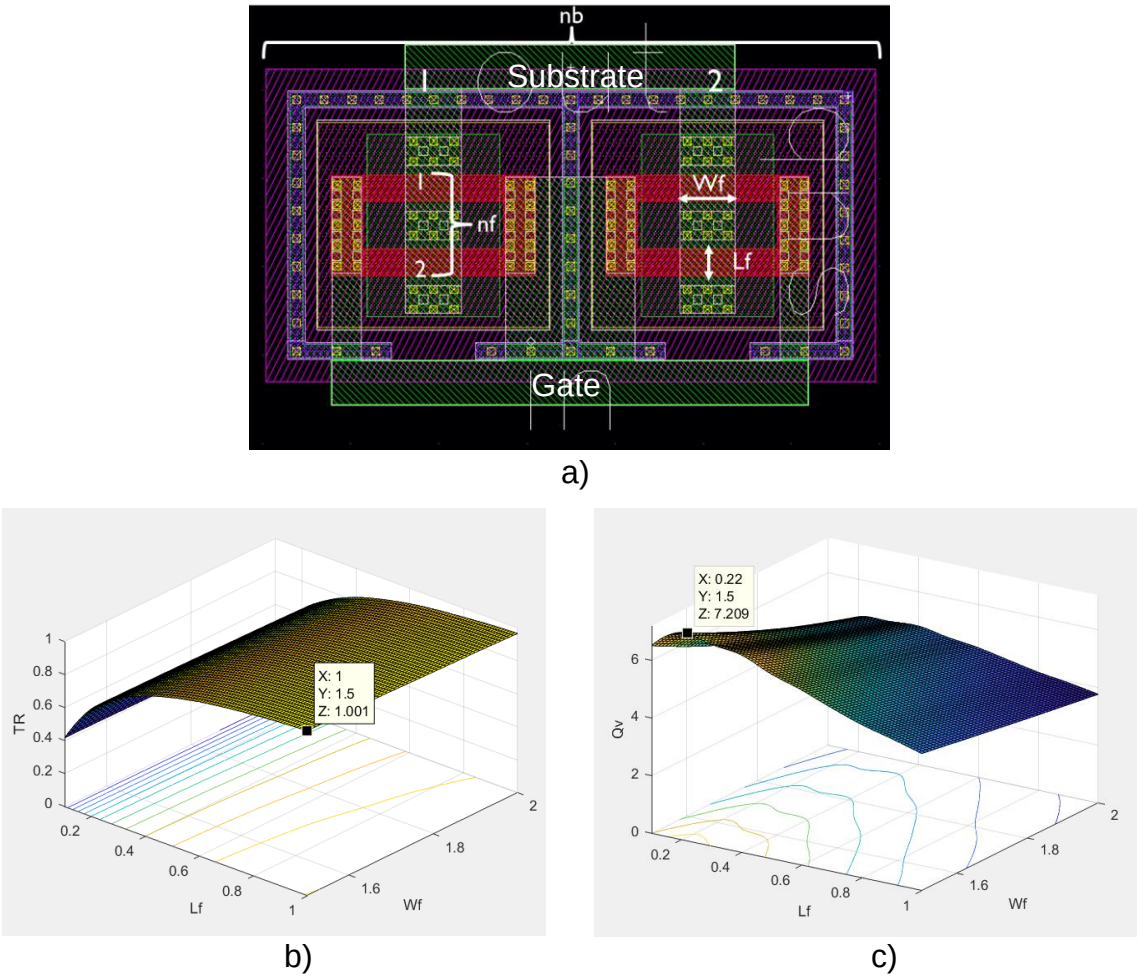


Figure 39 - a) PCell varactor layout with the design variables highlighted. b) Tuning range and c) zero-bias quality factor for thick-oxide PCell varactors for 100 nm < L_f < 1 µm and 1.5 µm < W_f < 2 µm. Source: author.

It can be seen that, indeed, the TR increases more strongly with increasing L_f, while the Q-factor is inversely proportional to W_f. For L_f, however, there is a region of higher Q-factor at around L_f = 0.22 µm.

Instead of being concentrated at the open-circuit end of the tank, the varactors can be distributed across the S-CPS inductor, connected between each strip and the floating shield underneath, as shown in Figure 40 a). This way the varactor size can be kept small, thus minimizing varactor losses, and they retain the resonance tuning ability, turning the S-CPS inductor into a loaded line phase shifter that resonates when its electrical length equals 90°. By controlling the varactors' bias, the phase velocity of the transmission line can be changed, thus changing the electrical length of the short-circuit-terminated S-CPS phase shifter. The equivalent electrical model for the varactor-loaded S-CPS is also shown in Figure 40 b).

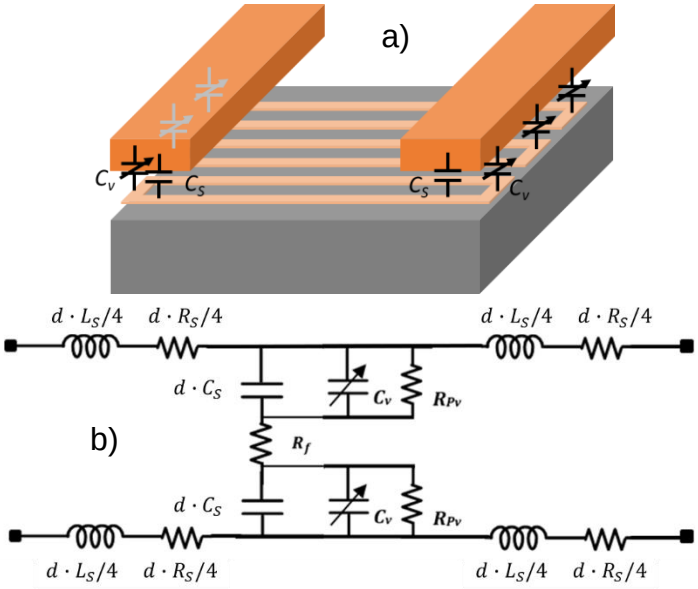


Figure 40 – a) Basic structure of the varactor-loaded S-CPS and b) its equivalent electric mode. Source: author.

The varactors, modelled by C_V and their equivalent parallel losses R_{Pv}, appear in parallel with C_S on both strips. The other passive elements, L_S, R_S, C_S and R_f, appear multiplied by a length $d = nfing * (SS + SL)$, where $nfing$ is the number of fingers that are connected to each pair of varactors. The S-CPS resonator can be modelled by cascading a number of stages equal to the total length of the resonator. The equivalent, loaded capacitance for each segment can be calculated as:

$$C_{eq} = d \cdot C_S + C_v + C_{v\_par} \quad (10)$$

where C_{v_par} is the interconnection parasitic capacitance of the varactor. The S-CPS needs to be designed having in mind the varactor loading to maximize the control of the varactor over the C_{eq}. Because of this constraint, C_S has to be made as small as possible while maintaining low losses to maximize the loaded S-CPS Q-factor.

To complete the resonator, there is still need to account for the short-circuit termination parasitics. The short-circuit serves two different purposes: the first is to supply DC power to the VCO core; the second is to guarantee a good AC ground to create the contour condition for the λ/4 resonator. To create a good DC supply, there is the need of large shunt capacitors to smooth the V_{DD} and to shunt high-frequency AC noise to ground. To create a good AC ground, the termination

itself needs to be low impedance, thus low inductance and resistance and capacitive reactance at the desired frequency. So, the idea for a layout is formed: thick, wide metal tracks connecting both S-CPS signal strips and a large capacitor bank to the DC ground to smooth out the supply voltage. Two alternatives were considered for the capacitor bank placement: one way is to put one bank close to each signal strip termination, which is called **termination 1**; another is to put it close to the central point of the short-circuit termination, which is called **termination 2**. The basic layouts of the two proposed solutions with their main components and parasitics are presented in Figure 41, as well as their equivalent models. Termination 1 would offer a better DC decoupling than termination 2, since the total C_{shunt} is higher than termination 2: but the equivalent impedance of these capacitor banks would be degraded by the L_{cap} inductance, thus limiting the ac grounding performance of termination1.

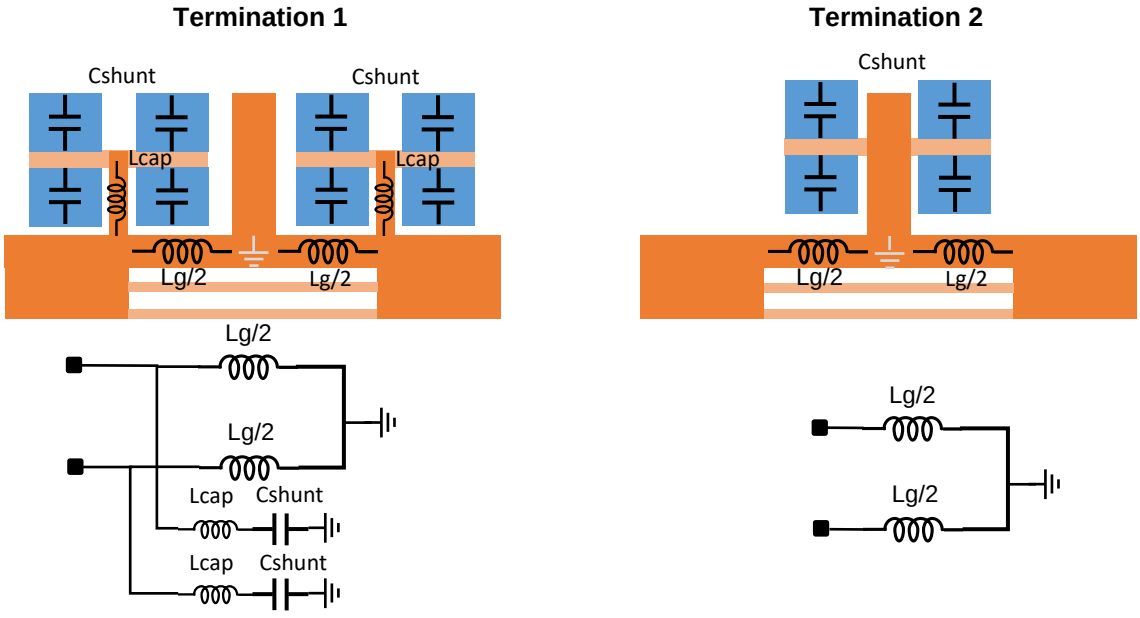


Figure 41 – Basic layout and equivalent electrical model of the two short-circuit terminations proposed for the loaded S-CPS resonator. Source: author.

The complete resonator model is shown in Figure 42. It is comprised of a number of loaded S-CPS segments, each representing a length $d = nfing * (SS + SL)$ totaling the complete length of the resonator, ended by the short-circuit termination model. This complete model permits the calculation of the resonant frequency and equivalent loss resistance of the resonator, and was used to design the VCO core.

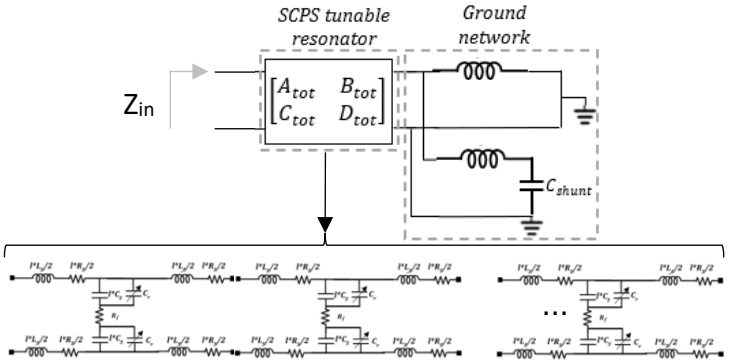


Figure 42 – Complete model of the distributed S-CPS resonator.Source: author.

3.3.2 MOSFET CROSS-COUPLED PAIR

The cross-coupled pair (CCP) is a classical, MOSFET-based negative resistance circuit that is used extensively as loss-compensation circuit in monolithic, CMOS-based VCOs because of its simplicity and ease of biasing. The basic operating principle of a CCP-based VCO is the compensation of the tank losses by the two fed-back MOSFETs, which is modelled as a negative resistance, R_{neg}, in parallel to the equivalent tank losses, modelled as a resistance, R_p, in parallel with the tank circuit. The basic schematic for a CCP and its equivalent electrical model are shown in Figure 43.

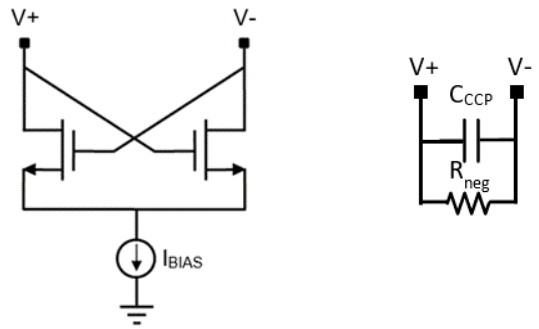


Figure 43 - Basic schematic of the Cross-Coupled Pair, showing the biasing tail current source, and its equivalent electrical model: a negative resistance in parallel with the parasitic capacitance of the devices. Source: author.

To satisfy Barkhausen's criterion, the absolute value of R_{neg} should be smaller than R_{loss} so oscillations can start. However, because of process and temperature variations, there should be some overcompensation to guarantee the startup of the oscillations in worst corner cases. So, R_{neg} needs to satisfy:

$$\left|R_{neg}\right| = |-2/g_m| \leq R_{loss}/K \tag{11}$$

where K is an empirical loss compensation factor and g_m is the individual MOSFET g_m. The g_m depends on the physical dimensions of the transistors and

on the drain current I_D following the approximation given by (12):

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \tag{12}$$

This approximation tells that larger transistors biased at higher currents produce lower $|R_{neg}|$, at the cost of higher power consumption. The CCP's MOSFETs have a parasitic capacitance (C_{ccp}), calculated as:

$$C_{ccp} = C_{GS} + C_{DB} + 4 \cdot C_{GD} \tag{13}$$

where C_{GS}, C_{DB} and C_{GD} are the capacitance between gate and source, drain and bulk and gate and drain, respectively. MOSFET parasitic capacitances are proportional to the device size to a larger degree, being dependent on drain and source junction area and perimeter, and to I_D to a smaller degree. So, larger MOSFETs result in larger C_{ccp}, which will disturb the tank operation, as C_{ccp} is comparable to the varactor's own capacitance. Thus, the optimal CCP is the one that achieves the desired R_{neg} while minimizing power dissipation and C_{ccp}, which is achieved by finding a suitable trade-off between the W/L ratio and I_{BIAS}. The design procedure can be simplified if I_D is normalized by dividing it by W. An interesting characteristic of MOSFETs is that this quantity, I_D/W, serves to characterize important characteristics of the device and it is invariant regarding technology nodes, temperature, circuit topologies and, in a given technology node, over a wide range of L and threshold voltages [43]. For any MOSFET, a current density of 0.15 mA/µm gives the lowest noise figure, a current density of 0.2 mA/µm gives maximum f_{max} and a current density of 0.3 mA/µm gives maximum f_T. However, translating to R_{neg}, the minimum absolute value of R_{neg} happens at a current density of 0.35 mA/µm. Any more drain current than that, there will actually be a drop in $|R_{neg}|$, with an increase of output power and DC power dissipation. In Figure 44, the R_{neg} and the C_{ccp} are plotted in function of the biasing current of the CCP for values of W between 10 µm and 34 µm. Naturally, $I_{BIAS} = 2 \cdot I_D$, so the current densities are doubled.

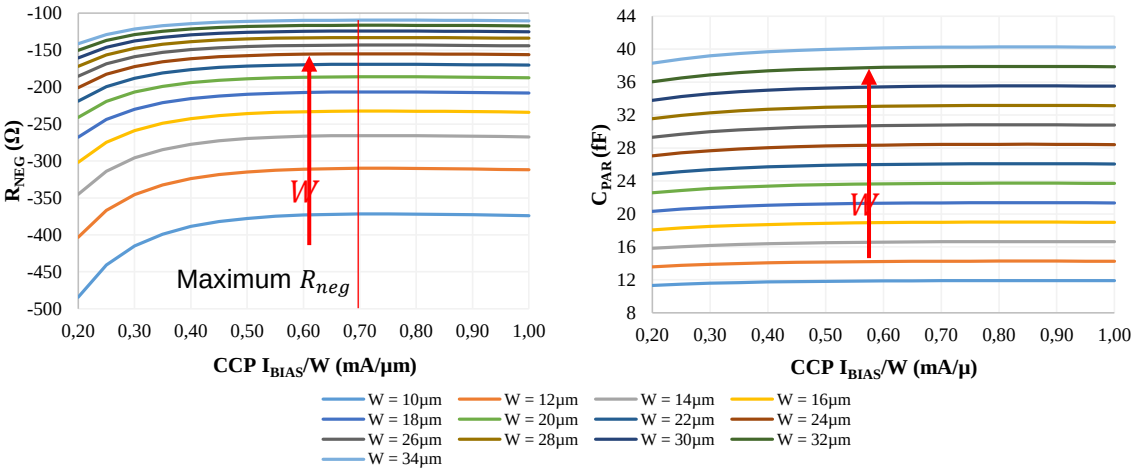


Figure 44 – Negative resistance and shunt parasitic capacitance of the MOSFET cross-coupled pair versus the tail current density. Source: author.

3.3.3 BUFFER

The output buffer isolates the VCO core from the loading by the following circuits, so that they do not disturb the VCO operation, such as disturbing the oscillation startup conditions. An ideal output buffer for a VCO would be a unitary power gain buffer, having infinite input impedance, zero input capacitance and a perfectly-matched output. In real life, however, these performance constraints lead to a scenario where fulfilling one constraint causes another to be disturbed. For example, having high input impedance would degrade the power gain because of impedance mismatch, low input capacitance would require small transistors, which would further decrease the power gain. However, good output match would benefit from a large transistor whose output impedance is already close to 50 Ω (assuming, of course, a 50-Ω system). The solution would be to implement a multi-stage buffer comprising a low input capacitance input stage, a power gain stage and an output-matching stage.

For this VCO design, this three-stage buffer was implemented as follows: a source-follower input stage, feeding a common source amplifying stage, a passive impedance matching stage and a common source output matching stage. The amplifier was designed using ADS optimization tools using the following constraints: 3 dB bandwidth of 10 % centered at 80 GHz; maximum input capacitance after layout of 5 fF; maximum insertion loss of 9 dB; maximum return loss of 10 dB inside the bandwidth. The final schematic, layout and post-layout simulations for this buffer are presented in Figure 45. All dimensions presented therein are already as in Si – that is, taking the shrink in consideration.

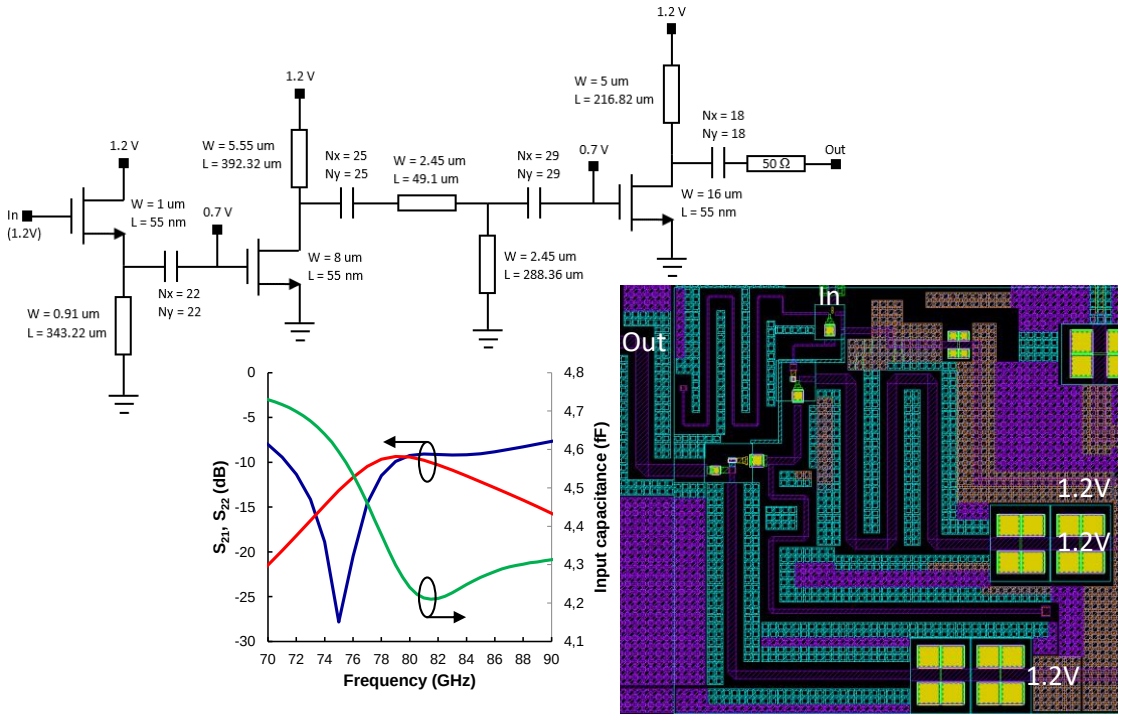


Figure 45 – Schematic, layout and post-layout simulation for the output buffer proposed for this VCO design. Source: author.

The input capacitance of the buffer is taken as 4.2 fF at 80 GHz, this value being added to the CCP C_{CCP} when designing the VCO. The output return loss is very good at 75 GHz, reaching 27 dB, however inside the rest of the band the output return loss reaches an almost flat value of 9 dB. Even though this is worse than the required 10 dB inside the band, this was the optimization result that better covered all the design requirements. Finally, each buffer consumes 6.49 mA of DC current.

3.3.4 OSCILLATOR DESIGN

Having shown all the building blocks of the VCO, the design procedure can now be explained. The goal is to arrive at a VCO with F_{OSC} = 80 GHz having the highest FTR possible. The complete model of the VCO is presented in Figure 46.

The goal of the design algorithm is to find the length (L_{en}) of the resonator, the W of the CCP and to estimate the frequency tuning range (FTR). The inputs are: the varactor (C_V, Q_V, CT, QT); the S-CPS (W_S, G, SS, SL, strips_layer, shield_layer); a table containing R_{neg} and C_{CCP} versus MOSFET W and I_{BIAS}/W; and finally, a desired F_{OSC}, called f_{des}.

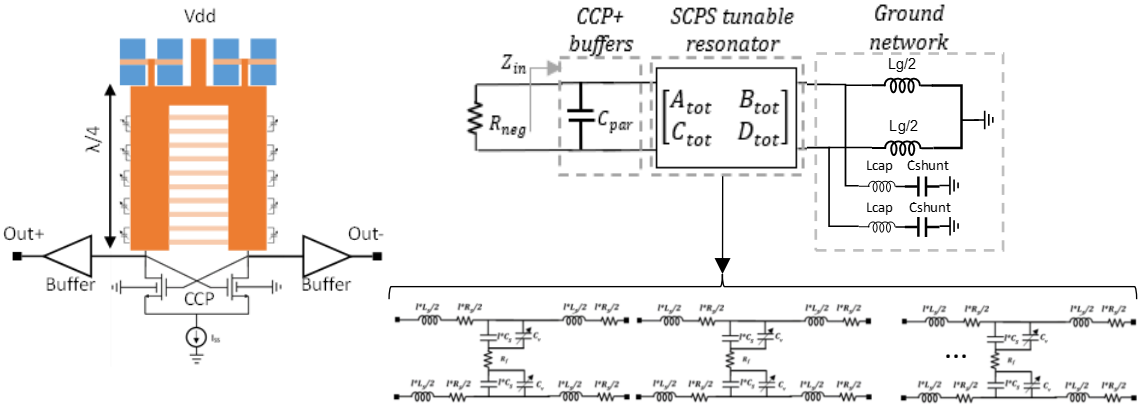


Figure 46 – Complete lumped model of the standing-wave oscillator based on the distributed S-CPS resonator. Source: author.

The calculation of the oscilation frequency of a loaded resonator of a given L_{en} involves finding:

$$(\mathcal{D}_R)_{f=F_{osc}} = 0 \tag{14}$$

where

$$\begin{bmatrix} \mathcal{A}_R & \mathcal{B}_R \\ \mathcal{C}_R & \mathcal{D}_R \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ j\omega C_{par} & 1 \end{bmatrix} \cdot \begin{bmatrix} A_{tot} & B_{tot} \\ C_{tot} & D_{tot} \end{bmatrix} \cdot \begin{bmatrix} A_G & B_G \\ C_G & D_G \end{bmatrix} \tag{15}$$

$$\begin{bmatrix} A_{tot} & B_{tot} \\ C_{tot} & D_{tot} \end{bmatrix} = \begin{bmatrix} \cosh(\gamma \cdot Len) & Z_C \cdot \sinh(\gamma \cdot Len) \\ \dfrac{\sinh(\gamma \cdot Len)}{Z_C} & \cosh(\gamma \cdot Len) \end{bmatrix} \tag{16}$$

$$\gamma = \sqrt{\frac{R_S + j\omega L_S}{R_f + \dfrac{R_p}{1 + j\omega C_v \cdot R_p}}} \tag{17}$$

$$Z_C = \sqrt{(R_S + j\omega L_S) \cdot \left(R_f + \frac{R_p}{1 + j\omega C_v \cdot R_p}\right)} \tag{18}$$

$$Len = N_{segs} \cdot d \tag{19}$$

N_{segs} being the number of d – long segments. Finding the L_{en} that gives $F_{OSC} = f_{des}$ is an iterative calculation, where L_{en} is adjusted so as $\mathcal{D}_R$ equals 0 at f_{des}. The flowchart of the design algorithm is shown in Figure 47.

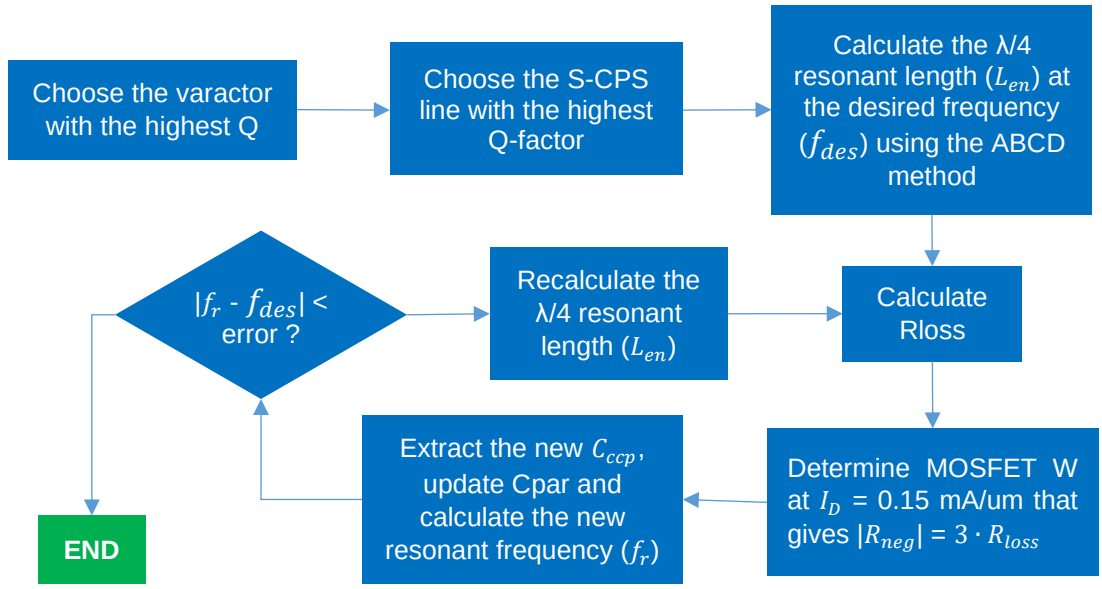


Figure 47 – Flowchart of the design algorithm of the distributed S-CPS resonator-based 80 GHz VCO. Source: author.

After L_{en} is determined, the resonator is simulated in HFSS to futher refine the accuracy and its RLRC model is built in Cadence Virtuoso. Then, the CCP is laid out to extract the actual parasitics. Finally, the oscillation frequency and phase noise are determined by post-layout harmonic balance simulation in Cadence Virtuoso ADE L tool.

3.3.4.1 Resonator optimization

The first step is to find the varactor with the best compromise between Q-factor and TR. The optimal varactor is determined by an exhaustive parametric SPICE simulation using the PCell model given by the PDK. The $nbcell$, N_f, W_f and L_f are varied and the optimal varactor is chosen as the one that has the highest average Q-factor while having a TR greater than 0.5. The $TR \geq 0.5$ constraint forces the compromise choice of a varactor with both a good capacitance tuning and good Q-factor. The chosen varactor has L_f = 0.38 µm, W_f = 1.7 µm, N_f = 1 and $nbcell$ = 2. The capacitance varies between 7.23 fF and 2.89 fF, resulting in a TR of 0.857. Q varies between 4.3 and 8.6. These values were extracted from SPICE simulations at 80 GHz.

The schematic and layout of the varactor interconnection are presented in Figure 48. R_{pol} implements a compact RF choke to isolate the varactor and shield from Vbias. The parasitics of this layout are modelled as a 1.5 fF capacitance in

parallel to the varactor. This parasitic capacitance is added to the S-CPS segment capacitance, $d \cdot C_S$, to improve the design accuracy.

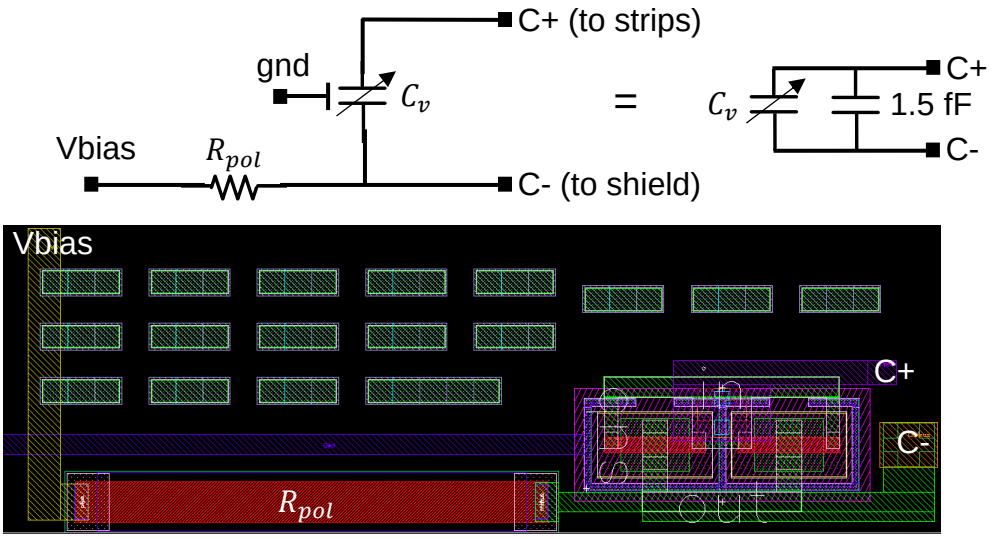


Figure 48 - Model, equivalent circuit and layout of the varactor connections to the S-CPS. Source: author.

The resonator design procedure continues with the optimization of the unloaded S-CPS to maximize the Q-factor and varactor control over C_{eq}. Drawing from the conclusions obtained from the S-CPS inductor optimization, wide strips reduce the ohmic losses of the S-CPS, but increase C_S, thus the separation between strip and floating shield needs to be increased. Also, since C_S is a function of the ratio between SS and SL, increasing SS and decreasing SL will also decrease C_S. SS and SL need to obey the constraint:

$$SS + SL \ < 2 \cdot t \tag{20}$$

to ensure low E-field leaking into the Si, increasing losses due to eddy currents. However, a more practical relation would be:

$$SS + SL \ < t \tag{21}$$

helping further minimize the substrate losses. Having this relation in mind minimize crosstalk between consecutive varactors, and to respect PCell clearance and design rules, d was fixed at 7.2 µm.

$$d = \ nfinger \cdot (SS + SL) = 7.2 \ \mu m \tag{22}$$

where $nfinger$ is the number of fingers loaded by each pair of varators. SL was kept at 0.6 µm as a compromise value between low C_S and low R_f. There is a number of possible layer combinations for the strip and the fingers metal layers, taking in consideration the BEOL stack presented in Figure 32. The lowest metal

that can be used on the S-CPS resonator is M5, because of interconnection restrictions. The topmost metal, M8, is better suited to be used by the signal strips, because of its greater thickness, which reduces ohmic losses. The viable layer combinations, given the presented constraints, are shown in Table 12, with their respective t and t_s.

Table 12 – Practical metallic layer combination for the signal strips and the floating shield of the unloaded S-CPS.

Strip layers (and t_s)	**Shielding layer (and t)**
M8 (3 µm)	M7 (1.5 µm), M6 (3 µm), M5 (4.4 µm)
M8+M7 (5.35 µm)	M6 (0.6 µm), M5 (3 µm)
M8+M7+M6 (6.8 µm)	M5 (0.6 µm)

First, the strip metal layers are optimized taking into account the metal thickness and the ohmic loss using the symmetrical S-CPS model presented in Section 3.2. Figure 49 shows $d \cdot R_S$ for three different metal combinations as a function of W_S: M8 strips, interconnected M8 and M7 stacked strips and interconnected M8, M7 and M6 stack. For all cases, G = 30 µm and shield is at M5 to create a fair basis for comparison between the different metal configurations.

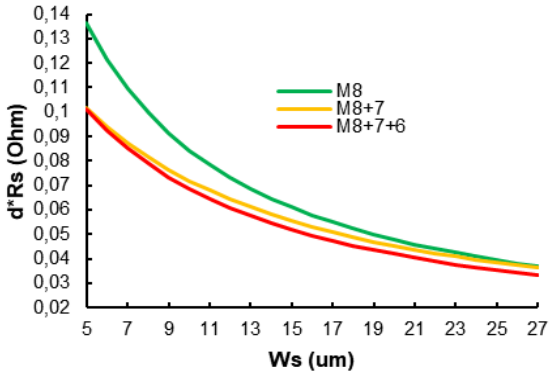


Figure 49 - Strip loss for three different signal strip metal configurations versus the strip width. Source: author.

The reduction in strip conductive losses that comes from increasing the t_S is more evident at thinner strips, as for W_S wider than 20 µm the difference in $d \cdot R_S$ becomes very small. So, the use of a thicker stack of metals would be more advantageous regarding conductive losses alone. However, because of the reduced t when using thicker metal stacks, the dramatic increase in C_S and the reduction in varactor control over C_{eq} means that thicker stacks for the signal

strips are not interesting for the distributed S-CPS resonator. Thus, the strip metal stack will consist only of M8.

Now, to determine the optimal shield layer, the Q-factor of the S-CPS for each different shield layer has to be compared, having in mind the C_S for each case. The Q-factor and $d \cdot C_S$ for the three different shield combinations are plotted in Figure 50 against W_S, with the varactor excursion shown for reference. The SS, $nfing$ and SL for each case are shown in Table 13.

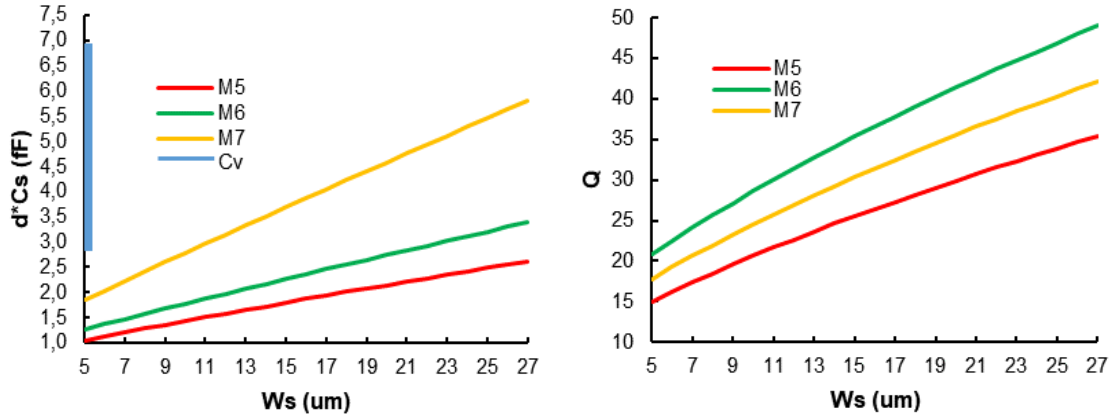


Figure 50 - Strip capacitance and quality factor of the S-CPS having M8 strips for three diferent options for the floating shield: M5, M6 and M7. The varactor excursion is shown for reference to have a sense of the control it would have on the equivalent S-CPS capacitance. Source: author.

Table 13 - Three different shield configurations for the M8-only strips, showing the finger width, pitch and number of fingers contained in the 7.2 µm segments. Source: author.

Strip layers (and t_s)	Shielding layer (and t)	M5 shield	M6 shield	M7 shield
M8 (3 µm)	M7 (1.5 µm)	SS = 1.8 µm	SS = 3 µm	SS = 1.5 µm
	M6 (3 µm)	$nfing$ = 3	$nfing$ = 2	$nfing$ = 4
	M5 (4.4 µm)		SL = 0.6 µm	

The combination that gives the highest Q-factor for every value of W_S is M8 for the strips, and M6 for the floating shield. As for the C_S, the configuration that gives the best varactor control, and thus FTR, is actually M5 for the shield. However, because of the large drop in Q-factor, and the resulting total losses of the resonator, the M5 shield was not considered for the final S-CPS structure.

Having determined the S-CPS layers, now it is necessary to determine W_S and G. Since the Q-factor increases with higher values of W_S, which can be observed from the Q-factor versus W_S curve in Figure 50, wider strips will produce higher-Q resonators. Figure 51 shows the Q-factor versus G curves for the M8/M6 S-CPS for two different values of W_S: 20 µm and 27 µm, the maximum value

permitted by the design rules.

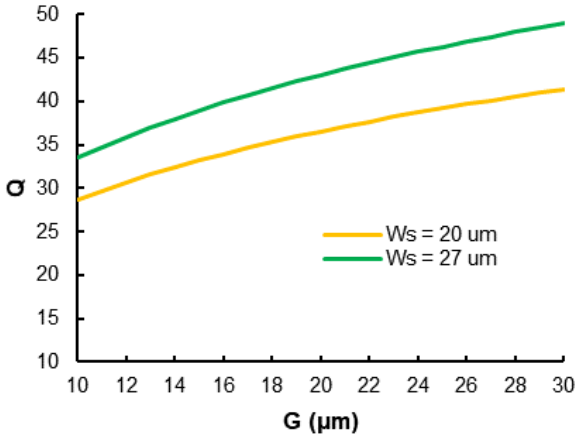


Figure 51 - Quality factor versus strip separation for two diferent values of S-CPS strip width. Source: author.

The Q-factor increases with G, so larger gap values would lead to higher Q-factor resonators. However, much larger values of G would lead to increased short-circuit inductance (L_g, see Figure 41), limiting the FTR. So, the optimal, unloaded S-CPS for the purposes of building a distributed resonator would have W_S and G = 30 µm. However, the larger value of C_S that results from a wider signal strip would degrade the varactor control over the phase velocity. This can be observed from the $d \cdot C_S$ versus W_S curves from Figure 50: for W_S = 20 µm, $d \cdot C_S$ = 2.54 fF, which is below the minimum capacitance value of the optimal varactor; however, for W_S = 27 µm, $d \cdot C_S$ = 3.4 fF, a 33% increase. This would degrade the impact of the varactor loading as C_v approaches the minimum value and, thus, limit the FTR. For this reason, W_S was fixed at 20 µm.

To test the accuracy of the model, and to maximize varactor control over the S-CPS phase velocity, two different resonators were designed, changing $nfing$ and SS: the first, called **design 1**, assumes $nfing$ = 2, minimizing substrate losses; the other, called **design 2**, assumes $nfing$ = 1 and $SS + SL = 2 \cdot t$, maximizing varactor control. The S-CPS model parameters are presented in

Table 14, as well as the chosen values for SS in each case.

Table 14 - S-CPS lumped RLRC model parameters and short-circuit termination interconnection parasitics for design 1 and design 2.

	SS = 3 µm, $nfing$ = 2	SS = 5.3 µm, $nfing$ = 1
Parameter	**Value**	
$d \cdot L_S$ **(pH)**	6.1	5.6
$d \cdot R_S$**(mΩ)**	32	27.9
$d \cdot C_S$ **(fF)**	2.4	1.85
R_f **(Ω)**	1.22	1.92

The short-circuit termination used for the two designs is the termination 1 shown in Figure 41. The capacitor bank is implemented with four PCell MOM capacitors, totaling 500 fF of total capacitance per bank. The short-circuit interconnection parasitics are presented in Table 15.

Table 15 – Parasitic components of the S-CPS short-circuit termination.

Parameter	**Value**
L_g **(pH)**	11.4
L_{cap} **(pH)**	12
C_{shunt} **(fF)**	500

3.3.4.2 CCP design and layout

The CCP R_{neg} is naturally a function of the MOSFETs W and of their biasing tail current. A way to simplify the CCP design is to fix I_D/W at minimum noise figure, 0.15 mA/µm, or 0.3 mA/µm considering I_{BIAS} for the two MOSFETs, and treat W as design variable, finding the one that gives the target overcompensation factor K = 3. After obtaining W for the desired R_{neg}, the CCP parasitic capacitance, C_{CCP}, is extracted and added to the buffer input capacitance and any interconnection parasitic capacitances to form the total parasitic capacitance C_{par}.

The layout uses a centroid topology to ensure the best possible symmetry between both halves, reducing process and temperature variations. C_{CCP} comprises the total parasitic capacitances in parallel with the negative resistance. R_{loss} and R_{neg} are calculated by:

$$R_{loss} = Re\{Z_{in}\rfloor_{f=F_{osc}}\} = Re\left\{\frac{\mathcal{B}}{\mathcal{D}}\right\} \quad (23)$$

$$|R_{neg}| = \frac{R_{loss}}{3} \quad (24)$$

The biasing of the CCP is realized by a 1:1 current mirror. A parallel design was chosen to reduce process-induced variations on performance and to keep the individual transistor W below 100 µm. The current mirror was designed to sink 10 mA with 10% of error with a headroom of 0.3 V. The MOSFET W and L were chosen as to minimize the output error while occupying the smallest possible surface, and were fixed as 25 µm and 150 nm, respectively. A capacitor bank was added to improve common-mode noise rejection. The complete layout for a CCP plus current mirror is shown in Figure 52.

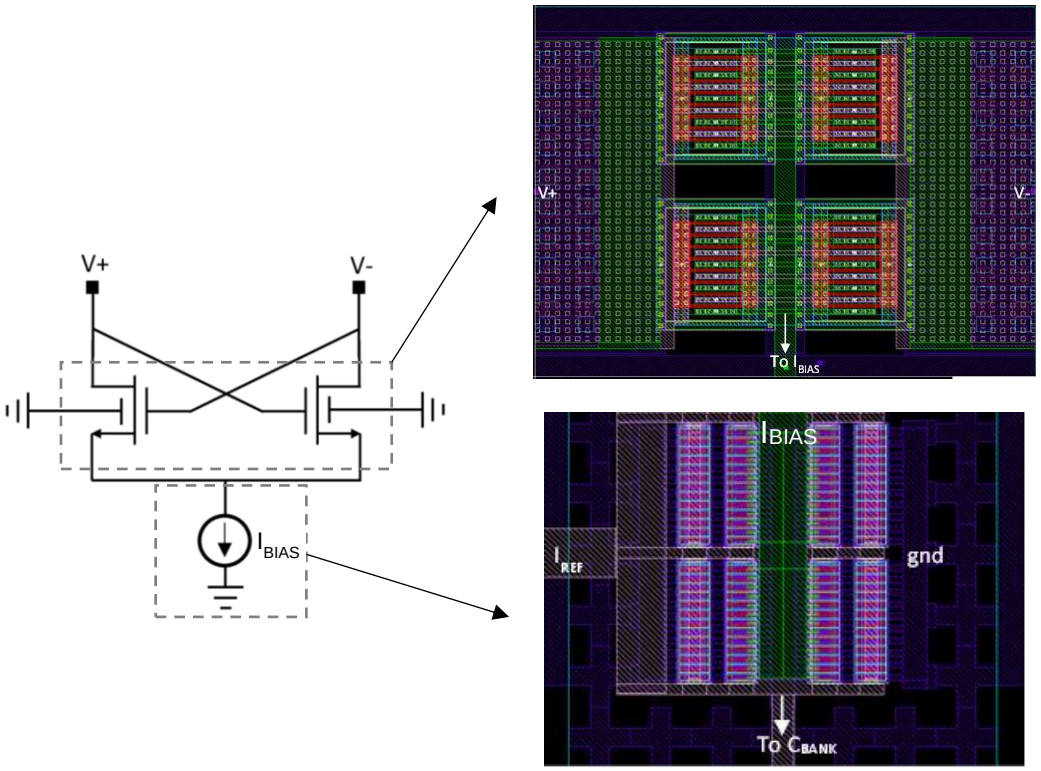


Figure 52 - Layout scheme of the cross-coupled pair, comprising the negative resistance MOSFETs and the current mirror. Source: author.

Post layout simulations reveal that the C_{CCP} for the common centroid layout presented in Figure 52 follows:

$$C_{CCP} = C_{MOS} + C_{layout} \cong 1.5 \cdot C_{MOS} \quad (25)$$

3.3.5 VCO RESULTS

After running the design algorithm for the two proposed designs, two different VCOs were designed. Table 16 contains the final length of the

resonators, CCP, W and R_{neg} for I_{BIAS} = 0.3 mA/µm for the two proposed resonator designs.

Table 16 - Final design parameters of the two proposed VCO designs after the design algorithm.

	SS = 3 µm, $nfing$ = 2 (“Design 1”)	SS = 5.3 µm, $nfing$ = 1 (“Design 2”)
Len	11*7.2 µm = **79.2 µm**	12*5.9 µm = **70.8 µm**
R_{loss}	836 Ω	792 Ω
CCP W	16 µm	16 µm
I_{BIAS}	4.8 mA	4.8 mA
I_{buffer}	12.98 mA	
R_{neg}	-258 Ω	-258 Ω
C_{par}	32.3 fF	32.3 fF

After laying out all important interconnections, the VCO core was re-simulated to assess its electrical performance. The post-layout simulations (PLS) were carried out in CADENCE Virtuoso design suite using spectre and ADE L tool and Quantus parasitic extraction (PEX) and physical verification (PVS) tools. The simulations that were carried out are harmonic balance simulations plus noise, intending to extract the output frequency, output power and phase noise of the oscillator. The PLS results for both oscilator designs are presented in Figure 53, at the same biasing conditions as shown in Table 16.

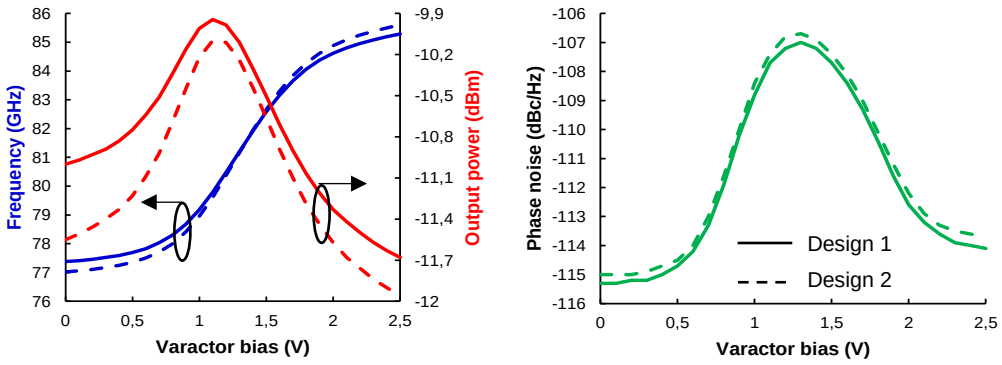


Figure 53 - Post-layout simulation results containing the output frequency (in blue), the output power (in red) and the phase noise (in green) for the two proposed tank designs. Source: author.

The F_{osc} in both cases is 81.3 GHz, with FTR approaching the 10% mark in both cases: design 1 has 7.9 GHz of output frequency excursion, translating to a FTR of 9.8 %; design 2 has a slightly wider output frequency excursion of 8.6 GHz, translating to a FTR of 10.6 %. The output power and phase noise of both designs is comparable, varying from -9.9 dBm to -12 dBm and

from -115 dBc/Hz to -106 dBc/Hz, respectively. Design 1 shows, however, slightly higher output power and phase noise performance, at the cost of slightly reduced FTR. This shows that the increase in varactor control by increasing SS translated into greater equivalent losses, and thus smaller closed-loop gain across the varactor biasing range.

Having the VCO core designed and laid out, the next step was to lay out the DC biasing network, the RF output and ground plane. Since the length difference between the two tanks design is only 8.4 µm, the placement of the buffers, pads and ground plane could be shared between both circuits. The layout for the die and the two VCO cores is presented in Figure 54.

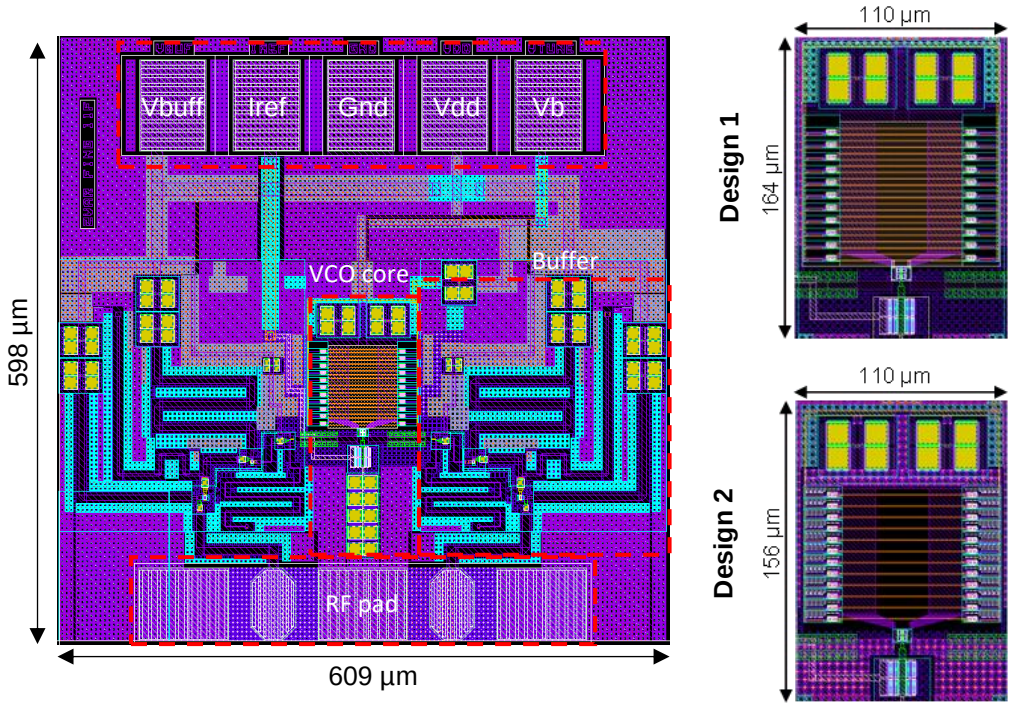


Figure 54 - Final layout for the two proposed VCO designs, showing the entire die and the two different cores. Source: author.

The complete VCO layout, including output buffers and I/O pads occupies an area of only 0.36 mm², where the VCO core itself occupies about 0.0176 mm², a mere fraction of the total area. This shows one of the advantages of the S-CPS-based resonator: reduced surface occupation thanks to the strong slow-wave effect that comes from the S-CPS when loaded by the varactors.

3.3.6 Discussions

Table 17 summarizes the performance of the two VCO designs shown in the previous section. The FOM of the two VCOs are in the vicinity of -186 dB,

showing excellent performance.

Table 17 - Post-layout results of the two proposed VCO designs.

	Design 1 (I_{REF} = 5 mA, I_{BIAS} = 4.43 mA)	**Design 2 (I_{REF} = 5 mA, I_{BIAS} = 4.43 mA)**
Central F_{osc}	81.3 GHz	81.3 GHz
FTR	7.9 GHz (9.73 %)	8.6 GHz (10.6 %)
PN @ 10 MHz (V_b = 0 V)	-115 dBc/Hz	-115 dBc/Hz
PN @ 10 MHz (V_b = 1.25 V)	-107 dBc/Hz	-106.7 dBc/Hz
PN @ 10 MHz (V_b = 2.5 V)	-114 dBc/Hz	-113 dBc/Hz
P_{out} **(V_b = 0 V)**	-11 dBm	-11.6 dBm
P_{out} **(V_b = 1.25 V)**	-10.1 dBm	-10.18 dBm
P_{out} **(V_b = 2.5 V)**	-11.7 dBm	-12.0 dBm
FOM	-186 dB	-186 dB
RF efficiency (V_b = 1.25 V, VCO plus buffers)	0.94 %	0.92 %

For the same value of R_{neg} and thus the same loading parasitics, design 2 showed wider FTR for similar values of output power and FOM. Thus, this configuration will be used in the next designs.

3.4 OPTIMIZED DESIGN ALGORITHM FOR THE STANDING-WAVE OSCILLATOR BASED ON DISTRIBUTED S-CPS RESONATOR

Drawing from the promising results obtained in the previous section, where the basics of the S-CPS-based distributed resonator and VCO were explained and designed, this section deals with the improvement of the design algorithm. The objective of this new algorithm is twofold: the first is to create a systematic way to design VCOs using the distributed S-CPS resonator, where a set of design goals would result into an optimized design; the second is to arrive at the best-performing S-CPS resonator, given a target central F_{OSC} and FTR, by optimizing the loaded S-CPS – that is, taking the varactor characteristics into the S-CPS during the optimizations instead of simply choosing the best varactor and then the best S-CPS dimensions.

The grounds for this algorithm is explained in the following subsections. The algorithm was used to design an 80 GHz VCO with a target FTR of 10 %.

3.4.1 LOADED S-CPS OPTIMIZATION

The premise behind the new design algorithm is: for a given F_{OSC} and FTR on an arbitrary S-CPS structure (W_S, G, t, t_S), there is only one varactor (W_f, L_f, $nbcells$) that will fulfill the design goals while maximizing the resonator Q-factor, taking into account all parasitic and loading from the CCP and the short-circuit interconnection.

First of all, the loaded S-CPS model needs to be addressed. The RLRC model presented in Figure 40 is quite hard to work with as it is, because of the number of components and circuit complexity, even though it describes the physical behavior of the S-CPS very well. The idea is to simplify the shunt section of the model, incorporating the varactor losses into the S-CPS components and converting everything into an equivalent telegraphist model. The telegraphist model is simpler and easier to work with, as it is very well-known and used.

The conversion involves a number of parallel-to-series conversion of RC networks. The conversion maintains the Q-factor of the RC circuit while changing the resistive and capacitive elements using the following equations:

$$C_{parallel} = \frac{C_{series}}{\left(1 + \frac{1}{Q^2}\right)} \tag{26}$$

$$R_{parallel} = R_{series} \cdot (1 + Q^2) \tag{27}$$

The Q-factor for the series and parallel networks are defined as:

$$Q_{series} = \frac{1}{\omega \cdot C_{series} \cdot R_{series}} \tag{28}$$

$$Q_{parallel} = \omega \cdot C_{parallel} \cdot R_{parallel} \tag{29}$$

Naturally, $Q_{series} = Q_{parallel} = Q$ so the two networks are electrically equivalent. Figure 55 shows the steps of the conversion of the S-CPS shunt network into a simpler parallel RC network using the method described above.

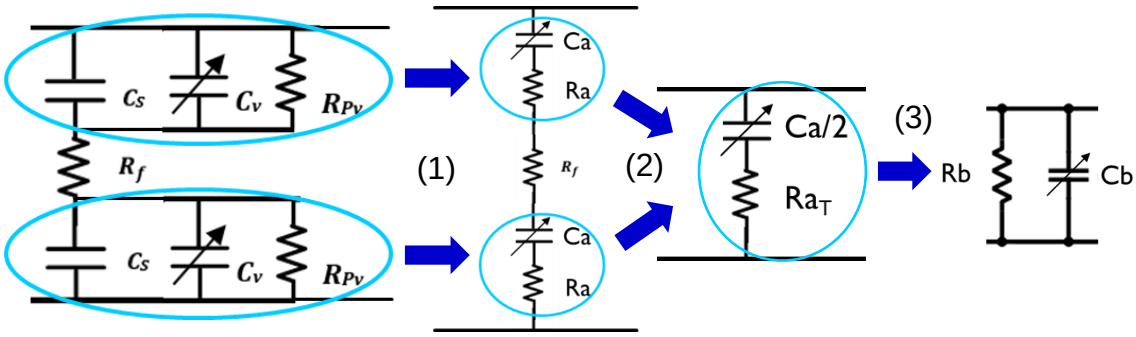


Figure 55 - Simplification steps of the capacitive shunt network of the loaded S-CPS model. Source: author.

The conversion involves three steps: in step (1) the varactor capacitance is added to the S-CPS capacitance and to the varactor interconnection parasitics, and each resulting parallel RC network is transformed into an intermediate, series RC network using the following equations:

$$C_a = (C_S + C_v)\left(1 + \frac{1}{{Q_1}^2}\right) \tag{30}$$

$$R_a = \frac{R_{Pv}}{\left(1 + {Q_1}^2\right)} \tag{31}$$

$$Q_1 = \omega \cdot (C_S + C_v) \cdot R_{Pv} \tag{32}$$

In step (2) the resulting series circuit is now simplified, preparing it to the series to parallel conversion. The new equivalent series loss resistance is calculated as:

$$R_{aT} = 2R_a + R_f \tag{33}$$

In step 3, the simplified series RC network is converted to a parallel RC network, using the following equations:

$$C_b = \frac{C_a/2}{\left(1 + \frac{1}{{Q_3}^2}\right)} \tag{34}$$

$$R_b = R_{aT} \cdot \left(1 + {Q_3}^2\right) \tag{35}$$

$$Q_3 = \frac{2}{\omega \cdot C_a \cdot R_{aT}} \tag{36}$$

By inserting the maximum, minimum and central values for a given varactor capacitance and equivalent loss resistance into equation (30), the resonator can be modelled at the extreme points of the output frequency excursion. Thus, the FTR can be evaluated and the VCO designed using the same method described

by equations (14) to (19).

Having the equivalent telegraphist model, the loaded S-CPS resonator can be optimized as a single entity. To understand how the optimum varactor can be found, the algorithm has to look at two different relations: the first is the relation between C_v and Q_v and TR; the second is the relation between the loaded S-CPS Q-factor and the varactor, for different values of FTR.

Figure 56 shows the plots of C_v versus Q_v and C_v versus TR. Drawing from the data observed in Figure 39, where it can be seen that increasing W_f causes Q_v to drop, W_f is set to the minimum possible value of 1.5 µm. Also, nf is set to 1 to keep Q_v high. The C_v is increased, then, by increasing L_f and $nbcell$.

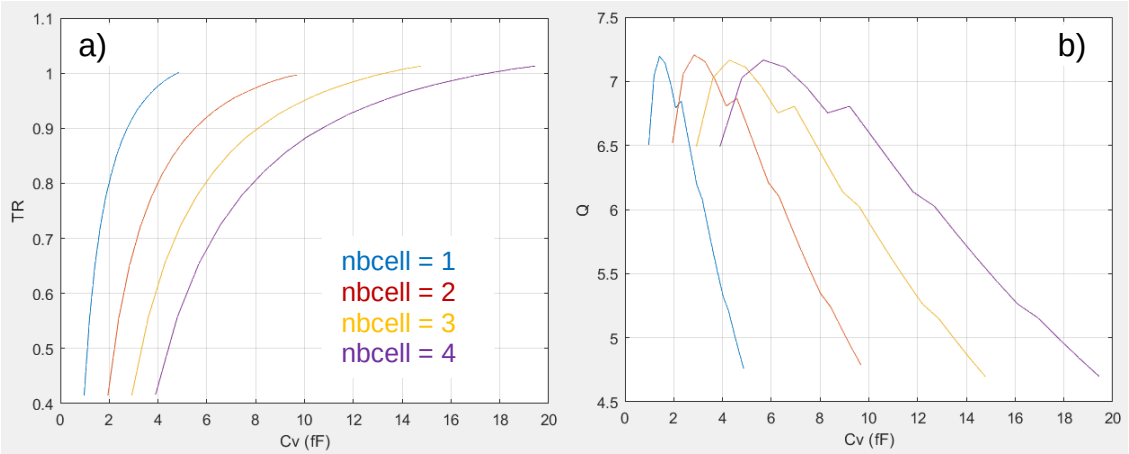


Figure 56 - Plots of varactor nominal capacitance versus the tuning range (a) and quality factor (b) for single-finger varactor whose width is 1.5 µm. Source: author.

It can be seen from the data presented above that the highest values of Q_v are found for C_v between 1 fF and 10 fF. Also, for a given value of C_v inside this range, there is a configuration that maximizes TR and another that maximizes Q_v.

Having this information in hand, the relation between the varactor and the S-CPS was investigated, as described in the following. First, the loaded S-CPS Q-factor (Q_t) is plotted for various varactors of L_f between 100 nm and 1 µm, and W_f between 1.5 µm and 2 µm, for nf = 1 and $nbcell$ = 1, for a fixed S-CPS having D = 30 µm and W_S = 27 µm. This plot, as well as its level curves, can be seen in Figure 57.

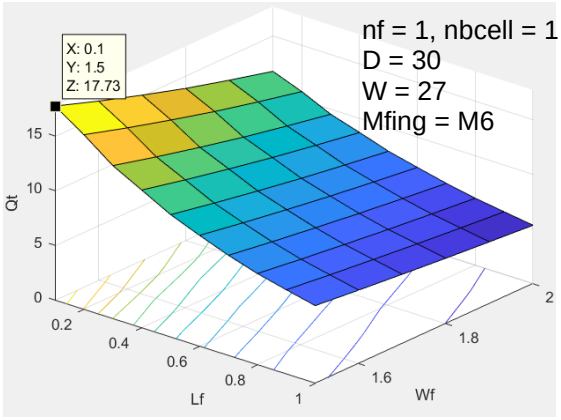


Figure 57 - Loaded S-CPS quality factor versus the loading varactor dimensions. Source: author.

From this plot it can be seen that the behavior of Q_t follows the inverse of the "intensity" of varactor control over C_{eq} from Equation (10): if C_{eq} is dominated by C_S the losses are low; however, if C_v dominates C_{eq}, the losses increase. Thus, resonators with wider FTR, which require more varactor control over C_{eq}, exhibit higher losses than resonators designed for narrower FTR. This behavior can also be observed if the curves for the different FTR are super-imposed on the Q_t level curves. This plot is shown in Figure 58 for a resonator built using the S-CPS presented in Figure 57, having an arbitrary length of 144 µm. For the purposes of this study, the effects from the short-circuit termination and from C_{par} were omitted.

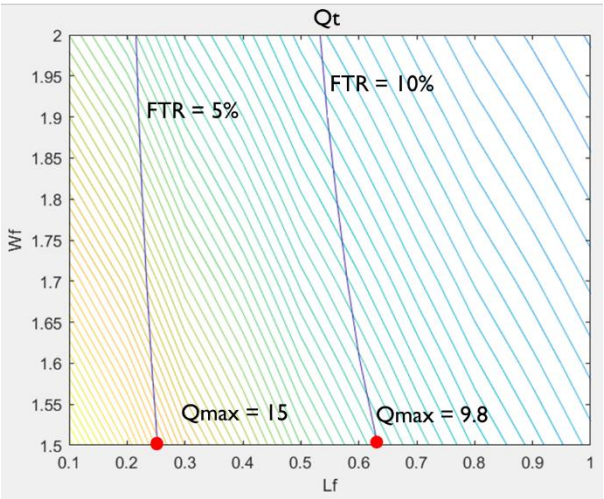


Figure 58 – The Q-factor level curves for a mock resonator, showing the *loci* of FTR = 5 % and FTR = 10% as dark blue lines. The Q-factor increases toward the lower left corner of the graph. Source: author.

The curves in dark blue show all resonators that show an FTR of either 5 % or 10 %. This plot shows that, indeed, for every S-CPS, given a target FTR,

there's a single varactor choice that maximizes the Q-factor, since it decreases with increasing W_f and L_f. This, naturally, can be extended for every viable S-CPS geometry, as can be seen in Figure 59. Here, the Q_t is plotted for the optimally-loaded, mock S-CPS resonator for different combinations of W_S and G

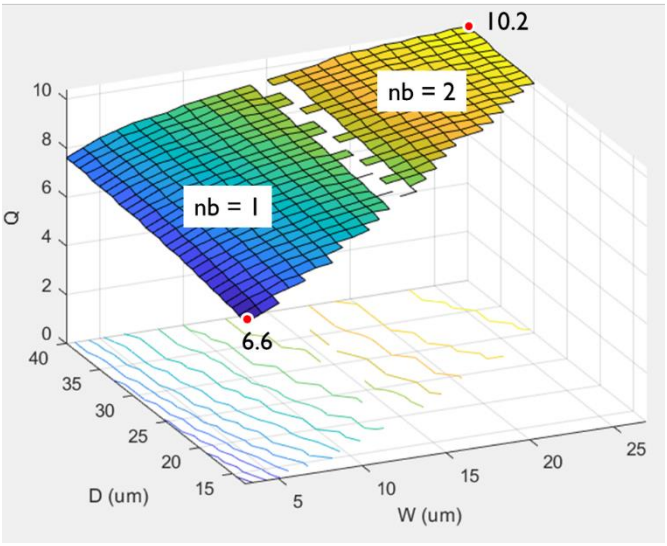


Figure 59 - Q-factor of the optimally-loaded, mock S-CPS resonator for every viable strip width and gap. Source: author.

The two distinct regions of the Q_t surface represent the difference in the value of $nbcell$ for the optimal varactor. It can be seen that the Q_t increases with W_S and D, reaching a larger value when these two variables are maximized.

In conclusion, to find the best-performing VCO, and thus the better-performing resonator, the designer has to maximize the Q-factor of the unloaded S-CPS, to then find the optimally-loaded S-CPS for a target FTR.

3.4.2 REDUCTION OF THE PARASITIC LOADS

To further improve the performance of the VCO, and thus of the loaded, distributed S-CPS resonator, there are still two important blocks that need to be improved: the short-circuit termination and the output buffer.

Starting with the short-circuit termination, the option chosen for this VCO design is the termination 2, whose basic layout and equivalent model are shown in Figure 60

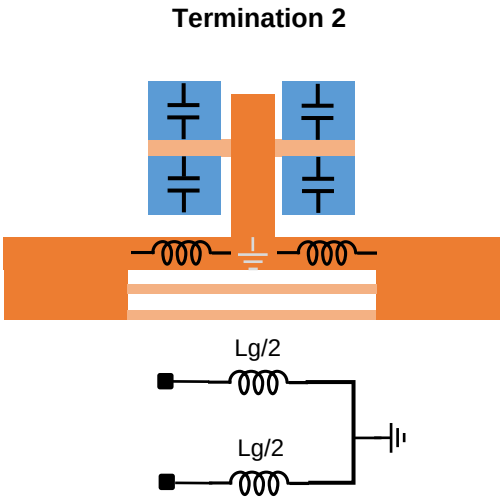


Figure 60 – Termination 2 for the short-circuit termination of the S-CPS resonator with its equivalent model. Source: author.

This option reduces the effective value of L_g, as C_{shunt} is accessed by a wide, thick metal strip, which has reduced parasitic self-inductance. The termination 1, on the other hand, has to use thinner strips because of layout constraints.

The termination 2 has another advantage: it permits the use of higher-quality C_{shunt} devices. Termination 1 employed PCell MOM capacitors, which are designed to produce high capacitance surface density. However, because of the narrow, dense and interconnected M2 to M5 mesh, the ohmic losses of these devices at mmW can be higher than a more traditional parallel-plate capacitor. The main disadvantage of parallel-plate capacitors, however, is the low capacitance density, which renders their use inviable for most monolithic devices.

The vertical parallel-plate (VPP) capacitor is a solution that unites the good electrical performance of parallel-plate capacitors with the higher surface density of MOM capacitors. It is laid out by stacking multiple parallel-plate capacitors, arranging them in a parallel fashion, to increase the surface density of the device. Another advantage of the VPP in decoupling capacitor layout is that the ground termination is part of the layout, as simply being the lowest plate of the stack. In the STM 55nm BiCMOS technology, this stack was laid out as follows: M8-M6-M4-M2 stack as the input plate and M7-M5-M3-M1 as the ground plate. The layout for the C_{shunt} cells used in both terminations is shown in Figure 61, as well as a comparison of the cross-section of these devices.

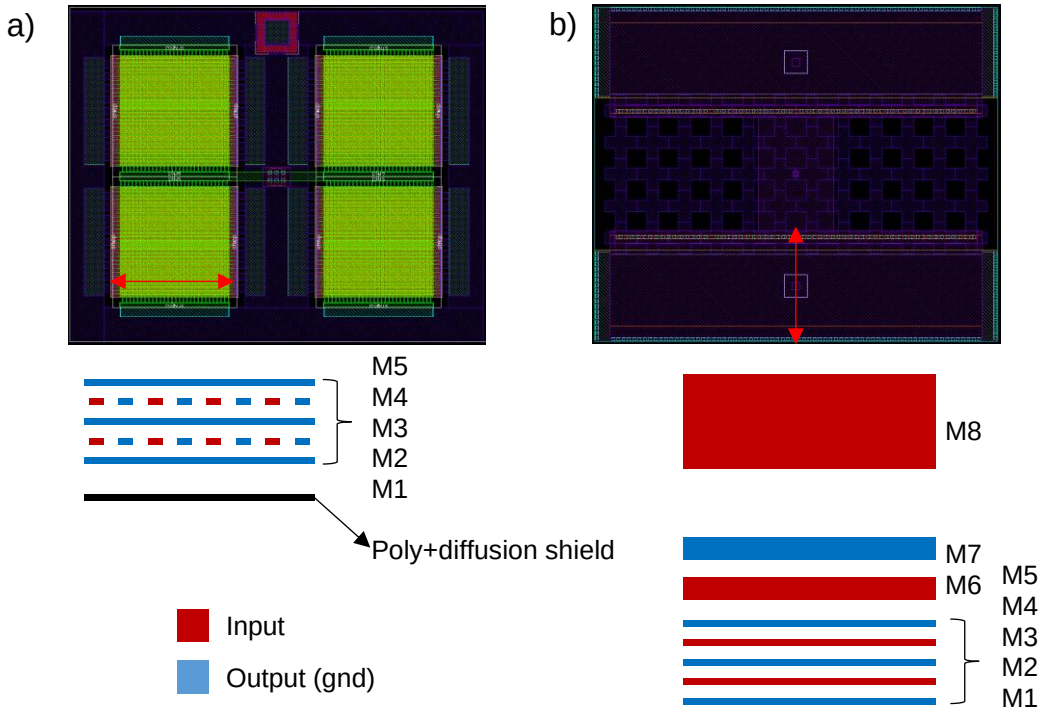


Figure 61 - Layout and cross-section comparison of a PCell MOM capacitor (a) and a custom-made VPP capacitor (b). Source: author.

The cells were designed to have a DC capacitance of around 1 pF, which translates to a reactance of 2 Ω at 80 GHz. Table 18 shows the performance parameters of the two C_{shunt} cells, considering the input and grounding parasitics. The Q-factor and self-resonating frequency (SRF) were obtained by simulating the extracted views of the two cells, thus taking into consideration all interconnection parasitics.

Table 18 - Post-layout performance parameters of the MOM and VPP C_{shunt} cells.

Parameter	MOM	VPP
DC C_{shunt} (pF)	1.19	0.747
Surface (μm²)	1858	2338
SRF (GHz)	57	155
Q-factor @ 80 GHz	---	10

The VPP capacitor shows an improved SRF and Q-factor when compared to the standard MOM capacitor, especially taking in consideration the access parasitics. The cost to be paid, of course, is a smaller capacitance density, which results in a larger surface occupation for a given capacitance value.

Now, for the short-circuit termination itself. Considering G = 30 μm as the total length of the short-circuit termination, which is routed on M8 with a width of

10 µm, the L_g of Termination 2, shown in Figure 41, was found to be 11.4 pH. This value was extracted using Ansys' Q3D parasitics extractor and compared against the PDK parasitics extractor, which was found to be in very good agreement.

The output buffer was also optimized to achieve two goals: the first was to reduce the input capacitance to a minimum possible to reduce the loading on the tank; the second was to increase the bandwidth and flatness of the power gain inside the passband. To this end, the input stage was re-worked to implement a differential pair, retaining the same topology on the two following stages, that is: a middle stage to deliver power gain and an output stage to match the load impedance. The differential input stage greatly reduces the actual capacitive load on the tank because of the differential nature of the circuit, being the half of an equivalent common-source stage. The final layout of the new output buffer and the schematic of each half are shown in Figure 62. The PLS results are shown in Table 19.

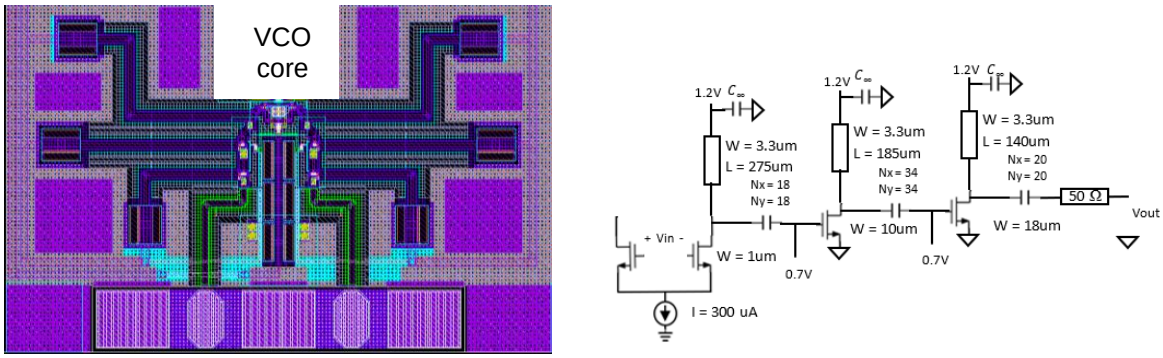


Figure 62 - Final layout, schematic and post-layout performance of the improved buffer. Source: author.

Table 19 - PLS results of the improved buffer.

Parameter	Value
Max. S_{21}	-8.5 dB @ 80 GHz
-1 dB bandwidth	75.5 GHz to 84.5 GHz
-3 dB bandwidth	74 GHz to 87 GHz
-10 dB bandwidth (output match)	72 GHz to 88 GHz
Total input capacitance	2.5 fF
I_{DC} (total)	14.1 mA

3.4.3 OPTIMIZED VCO DESIGN

Considering all that has been said in this chapter regarding the relationship between the varactors and the S-CPS, as well as the parasitics reduction and layout improvements of the short-circuit termination, the new design algorithm

can now be presented.

The goal of the design algorithm is to find L_{en} of the resonator, the W of the CCP and to estimate the FTR. The inputs are: a table containing C_v, Q_v, TR and QT, as well as their minimum and maximum values, of all varactors having W_f = 1.5 µm and N_f = 1; an optimized S-CPS; a table containing R_{neg} and C_{CCP} versus MOSFET W and I_{BIAS}/W; and finally, f_{des}. The flowchart of the algorithm is presented in Figure 63.

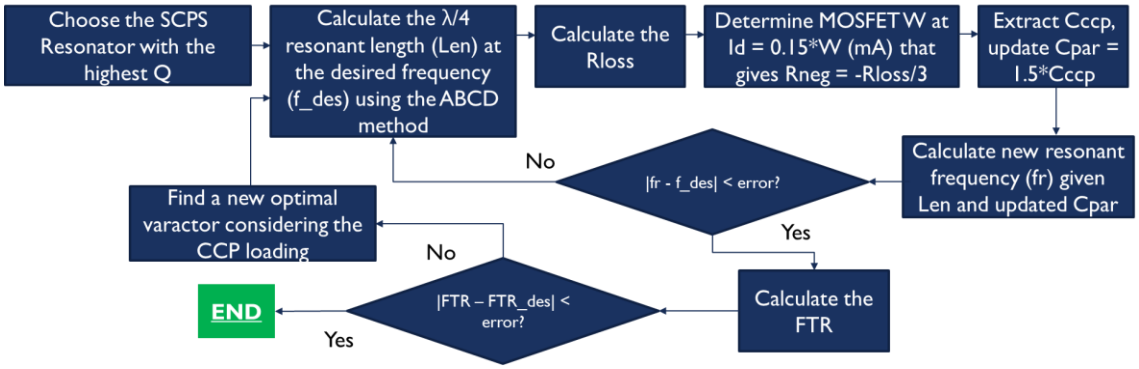


Figure 63 - Improved VCO design algorithm that tackles the simultaneous optimization of the S-CPS and varactor. Source: author.

After L_{en} is determined, the resonator is simulated in HFSS to futher refine the accuracy and its RLRC model is build in Cadence Virtuoso. Then, the CCP is laid out to extract the actual parasitics. Finally, the oscillation frequency and phase noise are determined by post-layout harmonic balance simulation in Spectre ADE L tool. The ABCD method uses Equation (14) to Equation (19), as the previous algorithm. The basic VCO schematic and equivalent model are shown in Figure 64.

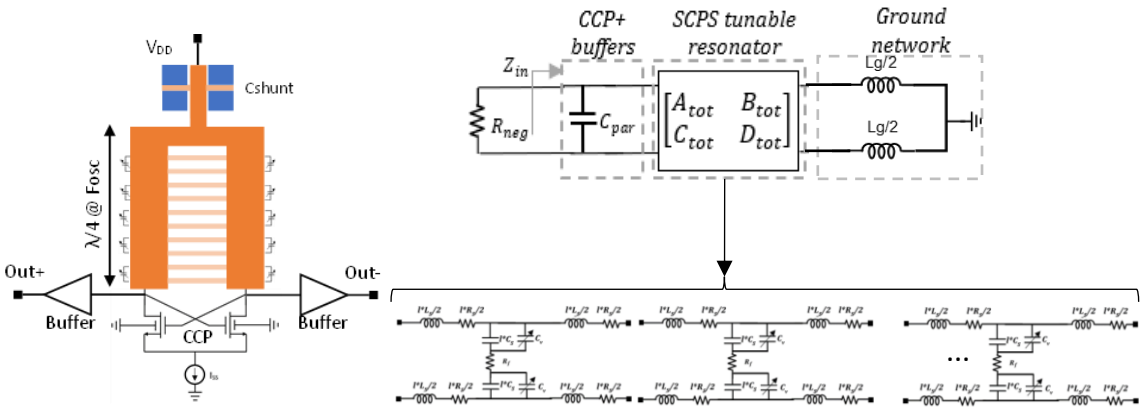


Figure 64 - Optimized VCO basic schematic and equivalent model. Source: author.

3.4.4 VCO RESULTS

Table 20 contains the final length of the resonator, CCP W and R_{neg} for I_{BIAS}/W = 0.3 mA/µm for the optimized VCO design.

Table 20 - Final design parameters of the optimized VCO after running the improved design algorithm.

Parameter	Value
Len	9*7.2 µm = **64.8 µm**
W_f	1.535 µm
L_f	0.395 µm
nb_cell	3
R_{loss}	594 Ω
CCP W	21 µm
I_{BIAS}	6.3 mA
R_{neg}	-197 Ω
C_{par}	39.1 fF

After laying out all important interconnections, the VCO core was re-simulated to assess is electrical performance. The PLS were carried out in CADENCE Virtuoso design suite using spectre and ADE L tool and Quantus PEX and PVS tools. The simulations that were carried out are harmonic balance simulations plus noise, intending to extract the output frequency, output power and phase noise of the oscillator. The PLS results for the optimized oscilator design are presented in Figure 53.

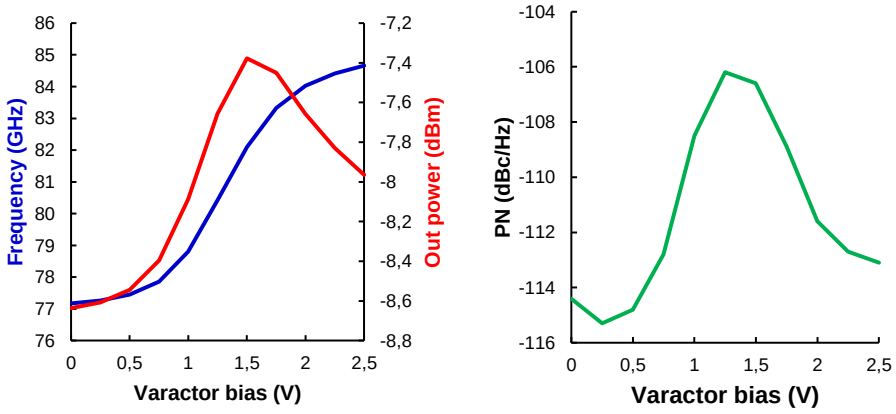


Figure 65 - Post-layout simulation results containing the output frequency (in blue), the output power (in red) and the phase noise (in green) for the two proposed tank designs. Source: author.

The observed F_{osc} is 80.3 GHz, and the output frequency excursion falls

between 76.34 GHz and 84.37 GHz, translating to a FTR of 8.03 GHz, or 10 %. The output power and phase noise of this design are from -7.4 dBm to -8.6 dBm and from -115 dBc/Hz to -106 dBc/Hz at 1 MHz, respectively.

Having the VCO core designed and laid out, the next step was to lay out the DC biasing network, the RF output and ground plane. The layout for the die is presented in Figure 66.

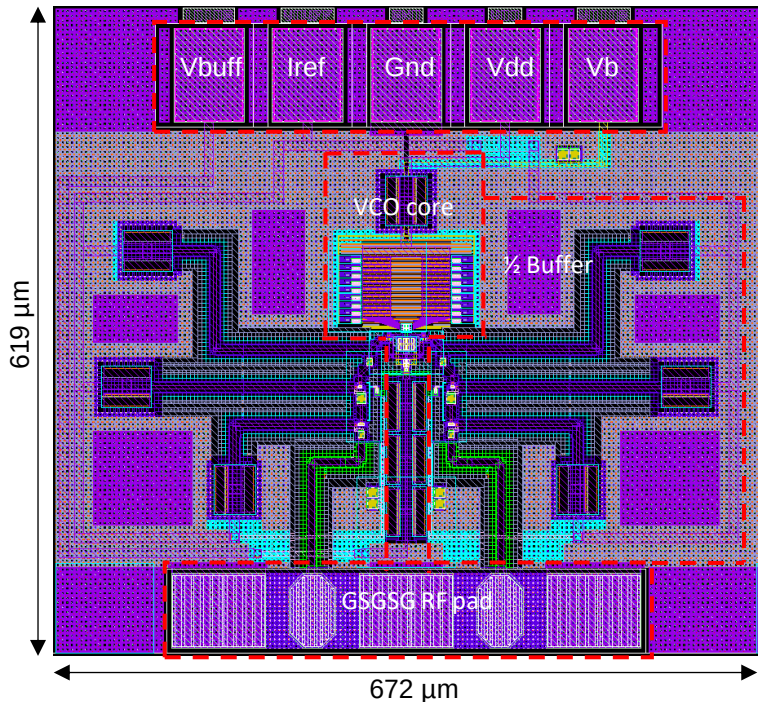


Figure 66 - Final layout for the optimized VCO at 80 GHz. Source: author.

The complete VCO layout, including output buffers and I/O pads occupies an area of only 0.416 mm², where the VCO core itself occupies about 0.017 mm², a mere fraction of the total area. The die area increased because of the larger size of the improved buffer, but the VCO core itself remained about the same size.

3.4.5 DISCUSSIONS

The R_{loss} of this new tank is lower than of the previous iteration (594 Ω compared to 792 Ω). The reason for this difference is an update of the varactor model that modified its equivalent losses to better represent the results the foundry was having from on-Si characterization. This update resulted in a twofold reduction of the varactor Q_v, which, in turn, increased the resonator losses. Table 21 shows the comparison between the resonator parameters of the optimal result and of the design 2 resonator of section 3.3 in two conditions: re-simulation using

the new varactor model and re-design using the improved design algorithm presented in section 3.4.

Table 21 – Comparison of the design and performance parameters of the two resonator topologies presented so far: the design 2 of section 3.3 and the new, optimized resonator.

Parameter	Section 3.3 Design 2 (re-simulated)	Section 3.3 Design 2 (re-designed)	Section 3.4 (optimized design)
Len	11*7.2 µm = **64.8 µm**	7*7.2 µm = **50.4 µm**	9*7.2 µm = **64.8 µm**
W_f	1.7	1.505	1.535
L_f	0.38	0.625	0.395
nb_cell	2	3	3
R_{loss}	792 Ω	485 Ω	594 Ω
CCP W	16 µm	26 µm	21 µm
I_{BIAS}	4.8 mA	7.8 mA	6.3 mA
R_{neg}	-258 Ω	-159 Ω	-197 Ω
C_{par}	32.3 fF	47.5 fF	39.1 fF
FTR	7.6 %	9.8 %	10 %

It can be seen that, even though the new model caused an increase of the resonator losses, or degradation of the FTR performance, the algorithm was able to find the optimal solution for both S-CPS configurations, further demonstrating the good performance and flexibility of the new, improved design algorithm.

Table 22 summarizes the performance of the optimized VCO design shown in the previous section. Compared to the two designs presented in section 3.3, the FOM did reduce about 2 dB, which would indicate a slightly poorer design. However, since the equivalent losses did increase, the fact that the new FOM is in the vicinity shows again the performance and flexibility of the new proposed design algorithm.

Table 22 - Post-layout results of the new, optimized VCO design.

	Optimized design (I_{BIAS} = 6.3 mA)
Central F_{osc}	80.3 GHz
FTR	8.03 GHz (10 %)
PN @ 10 MHz (V_b = 0 V)	-114.4 dBc/Hz
PN @ 10 MHz (V_b = 1.25 V)	-106.3 dBc/Hz
PN @ 10 MHz (V_b = 2.5 V)	-113.1 dBc/Hz
P_{out} **(V_b = 0 V)**	-8.6 dBm
P_{out} **(V_b = 1.25 V)**	-7.6 dBm
P_{out} **(V_b = 2.5 V)**	-7.9 dBm
FOM	-184.6 dB

RF efficiency (V_b = 1.25 V, VCO plus buffers)	0.7 %

3.5 STANDING-WAVE OSCILLATOR BASED ON DISTRIBUTED S-CPS RESONATOR WITH DISTRIBUTED NEGATIVE RESISTANCE

Moving on with the improvement of VCOs based on the distributed, loaded S-CPS resonator, the next step to be tackled is the reduction of the parasitic capacitance of the CCP by distributing it across the resonator. The goal is to decrease the loading capacitance close to the open-circuit termination of the resonator, as it is the point most sensitive to parasitic, shunt capacitances while keeping the same loss compensation of the classical approach of using a single CCP at the open-circuit termination.

This section presents the modelling of the S-CPS resonator with the distributed CCP, as well as a qualitative comparison between different R_{neg} distribution techniques. The distributed designs are compared against a reference case of a classical single CCP at the open-circuit end of the resonator.

3.5.1 WORKING PRINCIPLE

Being a short-circuit terminated λ/4 resonator, the current and voltage at the resonant frequency form a stationary wave across the resonator, and they follow a half sinusoidal distribution, being in antiphase between themselves. That is, on the short-circuit terminated end the current is at its maximum value and the voltage is zero. On the other end, at the open-circuit end, the voltage is at its maximum value and the current is zero. Thus, the impedance seen across the resonator at its resonant frequency changes depending on the distance to the short-circuit end. Ideally, the impedance at the open-circuit end should be infinite, and the impedance at the short-circuit end should ideally be zero. Figure 67 shows the resonating normalized voltage and current across a resonator of unitary length, zero being the open-circuit end and 1 the short-circuit end, as well as the equivalent impedance of this ideal resonator at each point across its length.

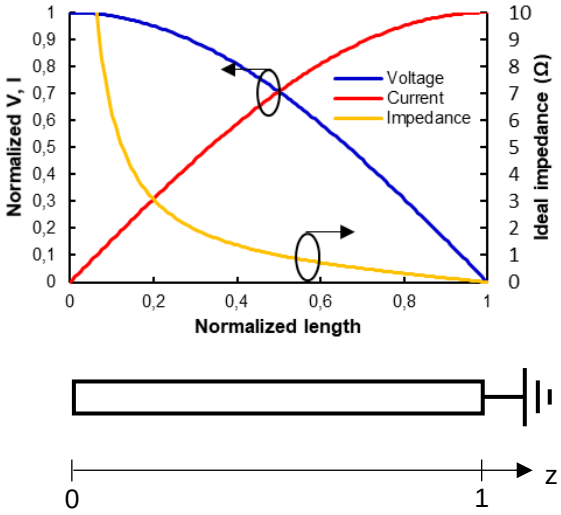


Figure 67 - Normalized current and voltage of a mock resonator of unitary length, where 0 is the open-circuit end and 1 is the short-circuit end. The impedance of this resonator is also shown. Source: author.

This “impedance” is merely an indicator of the “stiffness” of the resonator, and not an actual output impedance, as it doesn’t take into consideration propagation effects or loading by parasitic elements. This stiffness, however, indicates the sensitivity of the resonator towards shunt loads: since less current is present closer to the open-circuit end, the resonator is disturbed the most by shunt conductances, such as capacitive parasitics. However, it is also at this region that the loss compensation is most power-efficient, as less g_m is required to achieve the required R_{neg}.

Thus, since the CCP has parasitic capacitance, there is an inherent trade-off between the efficiency of the loss compensation and the loading it will cause, as the shunt capacitance lowers the FTR of the VCO.

3.5.2 EQUIVALENT MODEL OF THE RESONATOR

As explained in the two previous sections, the distributed S-CPS resonator is modelled by N 7.2 µm-long segments connected in series to form the total length of the resonator, L_{en}. The CCP, modelled as a parallel RC circuit, is inserted at one end, and the short-circuit termination, at the other end. Likewise, if the CCP is to be placed in a position other than the end, its model can be placed between two segments. Figure 68 shows an example of a distributed CCP where the CCP has been divided into three cells distributed across the resonator. Each block is modelled by the series connection of a number of 7.2-µm-long segments equal to the physical length of the block. The CCP’s C_{CCP} now considers the

interconnection parasitics to the resonator.

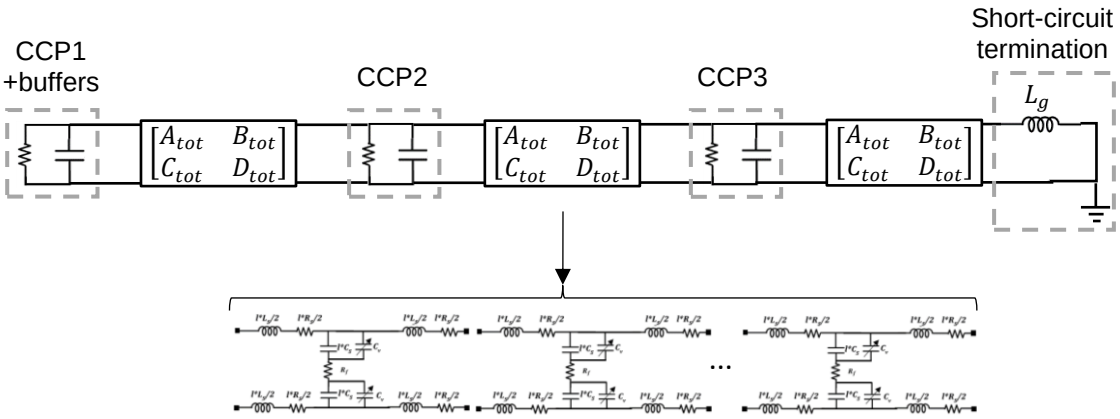


Figure 68 - Equivalent model of the distributed S-CPS resonator, having the CCP distributed as well across the resonator's length. Source: author.

The R_{neg} is determined just like the case of a single CCP, that is, by using Equation (23). The loss overcompensation factor, K, has to be determined in another way, as the placement of the CCP inside the tank will disturb the voltage and current distribution inside the resonator. K, thus, is determined practically by the following relation:

$$K = \frac{|Z_{in\_cl}|}{Z_{in\_ol}} \tag{37}$$

where Z_{in_cl} is the input impedance of the tank in closed-loop, that is, by taking the compensation from the CCPs in parallel with the tank's losses. Z_{in_ol}, on the other hand, is the open-loop losses, that is, the real, and positive R_{loss}. By taking the definition of K like so, it is possible to compare different CCP configurations, that is, lumped or distributed.

The resonant frequency for the VCO compensated by the distributed CCPs is calculated in a similar fashion as the method presented by Equation (14) to Equation (24). However, the model cannot be directly converted into an equivalent ABCD matrix anymore. The resonator is now modelled as a chain of *segments,* each loaded by a CCP. To find an equation that enables the designer to find the resonant frequency of this resonator, each CCP-loaded segment is transformed into an intermediate, equivalent ABCD matrix, which is obtained by:

$$\begin{bmatrix} A_{seg} & B_{seg} \\ C_{seg} & D_{seg} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ j\omega C_{ccp} & 1 \end{bmatrix} \cdot \begin{bmatrix} \cosh(l_{seg} \cdot \gamma) & Z_C \cdot \cosh(l_{seg} \cdot \gamma) \\ \cosh(l_{seg} \cdot \gamma)/Z_C & \cosh(l_{seg} \cdot \gamma) \end{bmatrix} \tag{38}$$

This segment ABCD matrix is then converted into a scattering transmission

matrix, or T-parameter matrix, for the resonant frequency calculation. By converting this ABCD matrix into a T-parameter matrix, the segments can be multiplied in series to model the complete resonator. This total T-parameter matrix can then be converted back into total ABCD matrix, so the open-circuit and short-circuit parasitic elements can be incorporated into the model, and the resonant frequency can, then, be calculated by Equation (14).

3.5.3 THE DIFFERENT METHODS OF DISTRIBUTING THE CCP g_m

There are three ways of achieving the goal of distributing the CCP, lessening the shunt capacitive loading on the open-circuit termination of the S-CPS resonator: the first is by moving the CCP towards the short-circuit termination, trying to maintain the same K; the second is dividing the total, lumped CCP g_m in more than one CCP that are distributed, equally-spaced, across the S-CPS resonator; finally, the third combines the two approaches, that is, divide the CCP into n smaller cells and move them all towards the short-circuit termination, so that the open-circuit termination is loaded only by the buffer.

3.5.3.1 Moving a single CCP towards the short-circuit termination

By moving the CCP away from the open-circuit termination, the S-CPS resonator gets less disturbed by the CCP parasitic capacitance. However, the CCP's own ability to compensate the resonator's R_{loss} gets further impaired the closer it is from the short-circuit termination. This phenomenon can be justified by two different methods, both arriving at the same result.

The first explanation is heuristic, and is based on the resonator "stiffness" depicted at Figure 67. It gets more difficult to influence the resonator behavior the further one is from its free termination: since more current is present at a given point, the CCP needs to source and sink larger drain current to compensate the same amount of R_{loss}, thus needing to have more g_m.

The second explanation takes into consideration the transmission line equations and the equivalent impedance seen by the CCP in an intermediate point between the open-circuit and short-circuit terminations. If the CCP is placed at a distance l_1 from the open-circuit termination, it will see the parallel combination of two S-CPS stubs: the first, of length l_1 ended by the buffer input capacitance plus parasitics; the second, of length $l_2 = Nsegs \cdot 7.2\,\mu m - l_1$,

ended by the short-circuit termination parasitics. This setup is illustrated in Figure 69.

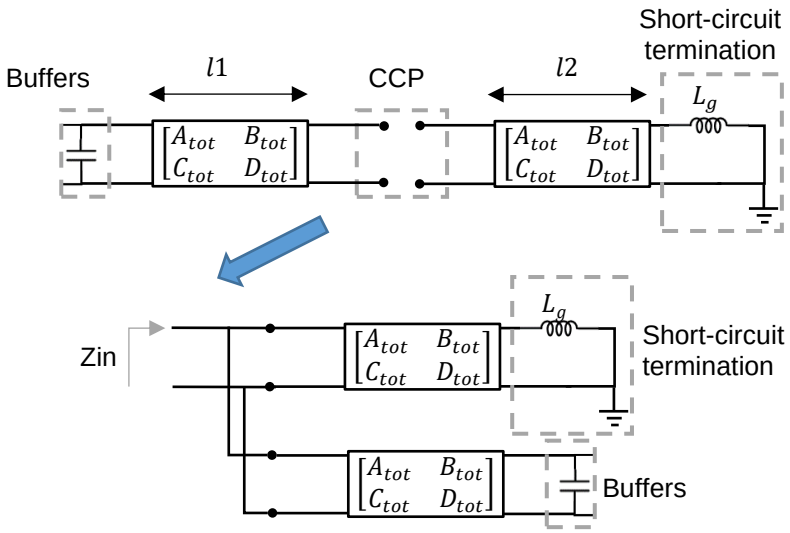


Figure 69 – Modelling the equivalent impedance seen by a CCP placed in an intermediate point l1 units of length away from the open-circuit point of the S-CPS resonator. Source: author.

If $l_1 = 0$, the system falls back to the classical, single CCP at the open-circuit termination. If $l_1 = Nsegs \cdot 7.2\,\mu m$, the CCP is placed at the short-circuit termination and the impedance it sees is dominated by the short-circuit parasitics, which shorts out the resonator. Thus, it can be seen that the CCP ability to compensate the losses do follow the same tendency. This parallel configuration can be used to calculate the R_{neg} seen by the CCP, and thus to determine the required g_m to achieve a target K.

There is an inherent trade-off between moving the CCP across the resonator. The more g_m is needed, the larger C_{ccp} the CCP will have, which will increase the capacitive load, but at a point of reduced sensitivity.

3.5.3.2 Distributing the CCP across the resonator

Instead of placing a single CCP at a certain point on the resonator, the CCP can be divided into n smaller sub-cells that are equally-spaced across the resonator. The equivalent model for the S-CPS resonator plus distributed CCP was already presented in Figure 68, and it can be looked at in two ways. First, if the CCP is divided into enough cells so that the electrical length between two adjacent CCPs is very small, the lumped model elements from the CCP can be

taken into the S-CPS model, as if the transmission line itself had more shunt capacitance and “negative losses”, i.e., negative shunt conductance. Second, if the spacing is larger, the resonator can be looked at a λ/4-long resonator that is loaded by lumped RC networks across its length. Because of the strong slow-wave effect that comes from the S-CPS loaded by varactors, the area occupied by the CCP, plus its biasing circuits, is significant when compared to the resonator’s own length. Thus, the “negative loss” transmission line approximation is not valid anymore.

The distribution of the negative resistance can be done in two ways: either the CCP g_m is distributed equally across the n CCP cells, a homogeneous distribution; or the g_m is unequally distributed, where some form of tapering is employed so that the CCPs closest to one of the resonator terminations has more g_m, a tapered distribution. The goal of the distribution is to reduce the size of the CCP at the open-circuit termination, thus reducing the capacitive load at that point. The goal of tapering the g_m across the resonator is to improve the energy efficiency of this configuration.

The sizing of the CCPs is done in an empirical way, since the placement of a CCP sub-cell changes the equivalent impedance seen by the other cells. Thus, the design for the distributed CCP is done running parametric sweeps inside a S-parameter simulation. The design stops when the Z_{in_cl} reaches the same values observed in the reference case.

3.5.3.3 Moving the distributed the CCP across the resonator

Now, if the distributed CCPs are moved towards the short-circuit termination, the capacitive loading at the open-circuit termination is minimized. The cost to be paid, of course, is that the total required g_m increases, decreasing the energy efficiency of the VCO.

The comparison between these different approaches is done as follows. First, a classical, single-CCP VCO is designed, but this time, the overcompensation factor K is set to 2, as the parasitics involved in the VCO layout are already well known, thus enabling a design with a wider FTR. This VCO is called the reference case.

Second, the single, shifted CCP VCO is designed. The goal is to find the CCP offset, that is, the distance between the CCP and the open-circuit termination that gives the best FTR, while maintaining the MOSFET W under 50 µm. The PLS result for this VCO is noted for later comparison.

Third, the distributed CCP VCO is designed. A single design is chosen depending on the FTR and DC-RF efficiency, and for this, the uniform and tapered distributions are compared in schematic simulation, and the best-performing option is laid out. The PLS results of this best option is noted for later comparison.

At last, the best distributed option is sent through the process of shifting the whole CCP set. To simplify the design, the CCPs was shifted by the same n*7.2 µm gap towards the short-circuit termination. That is, if the CCPs are spaced by 14.4 µm, the CCPs is shifted by this length towards the short-circuit termination.

To keep the comparison easier to do and more comprehensive, the three CCP variations are designed using the exact same S-CPS resonator used by the control case VCO.

3.5.4 REFERENCE CASE VCO

The classical-reference VCO uses the exact same design method presented at Section 3.4.3. The F_{osc} is still set at 80 GHz, however the K is now set at 2 and the FTR at 15%. The nominal drain current density of each MOSFET was set to 0.2 mA/µm, instead of 0.15 mA/µm, to further reduce the parasitic capacitance. The S-CPS geometry is still W_S = 27 µm and G = 30 µm, SS = 3 µm and SL = 0.6 µm. The VCO core results are presented in Table 23.

Table 23 - VCO core obtained from the optimized design algorithm for the reference case.

Parameter	Value
Len	8*7.2 µm = **57.6 µm**
W_f	1.5
L_f	0.6
nb_cell	4
R_{loss}	341 Ω
CCP W	24 µm
I_{bias}	12 mA
R_{neg}	-161 Ω
C_{par} **(plus buffer)**	44.56 fF

The VCO was then laid out to have its parasitic elements extracted. The final layout and the tank are presented in Figure 70. The die dimensions are 747 µm x 647 µm, resulting in an area of 0.438 mm^2. The ground plane, buffer layout and pads were re-used by the other VCOs, as the resonators is largely the same, thus simplifying the layout. The PLS results for the reference case VCO are presented in Figure 71, and summarized in Table 24.

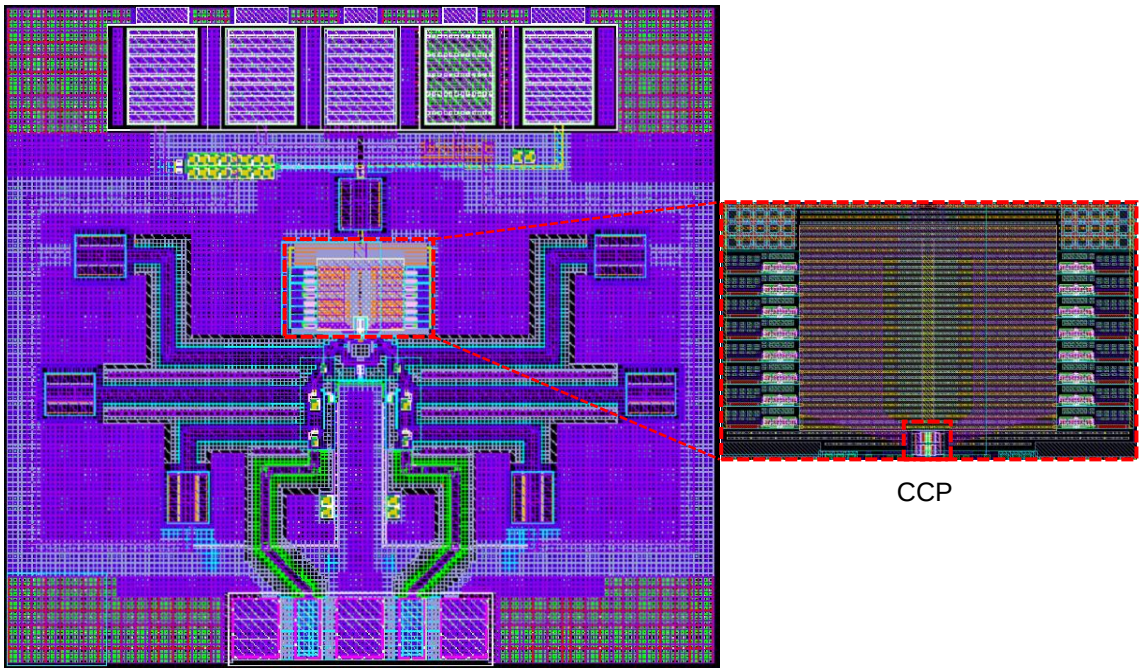


Figure 70 - Reference case VCO layout plus the tank in detail. Source: author.

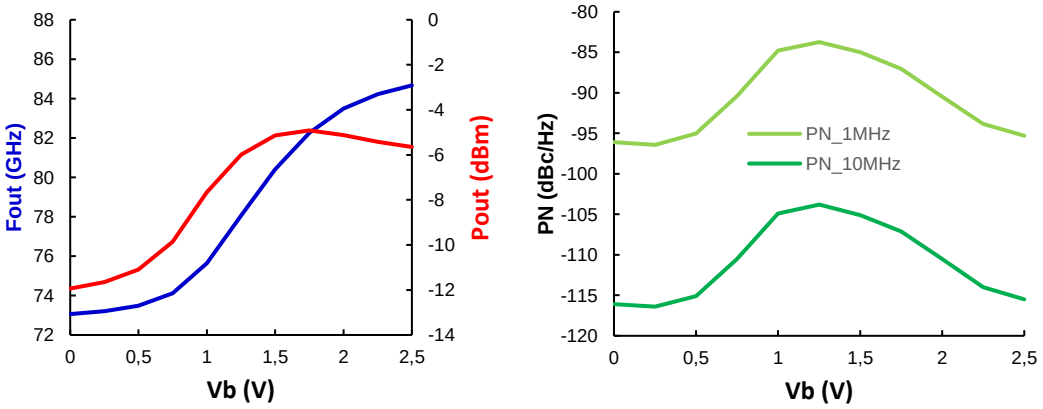


Figure 71 – Post layout simulation for the reference case VCO, showing the oscillation frequency (in blue), output power (in red) and phase noise at 1 MHz offset (light green) and 10 MHz offset (dark green). Source: author.

Table 24 – Summary of the post-layout simuation results of the reference case VCO.

	Final design (I_{BIAS} = 12 mA)
Central F_{osc}	78.9 GHz

$\boldsymbol{FTR}$	11.6 GHz (14.7 %)
PN @ 10 MHz (V_b = 0 V)	-116.1 dBc/Hz
PN @ 10 MHz (V_b = 1.25 V)	-103.8 dBc/Hz
PN @ 10 MHz (V_b = 2.5 V)	-115.5 dBc/Hz
$\boldsymbol{P_{out}}$ **(V_b = 0 V)**	-11.94 dBm
$\boldsymbol{P_{out}}$ **(V_b = 1.25 V)**	-6.0 dBm
$\boldsymbol{P_{out}}$ **(V_b = 2.5 V)**	-5.7 dBm
FOM	-182 dB
RF efficiency (V_b = 1.25 V, VCO plus buffers)	1 %

3.5.5 SHIFTED CCP VCO

The design of the shifted CCP VCO starts with determining the distance between the CCP and the open-circuit termination. This is done to avoid a recursive definition of the design, since the R_{neg} is a function of this offset, and the offset dictates the needed R_{neg}. Because of the modular nature of the S-CPS resonator, and of its modelling, the offset is given in number of 7.2 µm-long segments. This variable was called N_{off}.

The S-CPS resonator naturally forms a standing-wave resonator, which resonates at frequencies where its electrical length is equal to $(2\mathrm{n}+1)\cdot\lambda/4$, where n is the resonating mode. If, then, a shunt capacitance is placed at an intermediate point of a standing-wave resonator, degenerate higher-order modes can be created, which might create intermodulation interference with the desired, fundamental mode. To avoid this, the CCP was placed at the center of the resonator.

The design method for this VCO uses a modified version of the algorithm presented in Section 3.4.3. The modification happens at the computation of the required R_{neg}, where the CCP is sized based on the Z_{in} shown in Figure 69 instead of the equivalent losses of the resonator. Also, since the goal is to create a fair comparison between the different methods of distributing the CCP, the resonator won't be changed, so the optimization step is skipped.

The output half of the CCP's current mirror was laid out inside the S-CPS resonator, as well as the CCP MOSFETs. The diode-connected MOSFET, which is the other half of the current mirror, was laid out closer to the DC pad. Even if this would impair the matching between the two halves, this layout choice

facilitated the design and freed the much-limited area inside the S-CPS resonator. Even though the presence of low-conductivity Si (the MOSFET's active areas and P wells) should in theory increase the substrate losses, the shielding provided by the floating metal ribbons of the S-CPS mitigates most deleterious effects. Thus, the only extra parasitic elements considered for the CCP design were the extra shunt capacitance between the M8 interconnections and the M6 shielding ribbons. This extra capacitance was extracted in Ansys' Q3D parasitic extractor, was found to be equal to 1.6 fF, and was added to C_{CCP} for the design procedure.

Table 25 contains the parameters for the S-CPS resonator and for the shifted CCP. The W has increased to 38 µm, compared to 24 µm for the reference case, which results in an increase of DC power consumption (15.2 mA versus 9.6 mA for the reference case). The equivalent losses seen by the CCP have decreased to 153.8 Ω, which is a two-fold increase if compared to the 341 Ω of the reference case. The C_{CCP} increased as well, however it is now placed in the middle of the resonator.

Table 25 - Resonator core of the shifted CCP VCO.

Parameter	Value
Len	8*7.2 µm = **57.6 µm**
W_f	1.5
L_f	0.6
nb_cell	4
N_{off}	4*7.2 µm = **28.8 µm**
$Re\{Z_{in}\}$	153.8 Ω
CCP W	38 µm
I_{BIAS}	15.2 mA
R_{neg}	-75 Ω
C_{CCP}	68.1 fF

The VCO was then laid out to have its parasitic elements extracted. The final layout and the tank are presented in Figure 72. The die dimensions are exactly the same as the reference case VCO, 747 µm x 647 µm, as the ground plane and biasing pads were re-used. The PLS results for the shifted CCP VCO are presented in Figure 73, and summarized in Table 26.

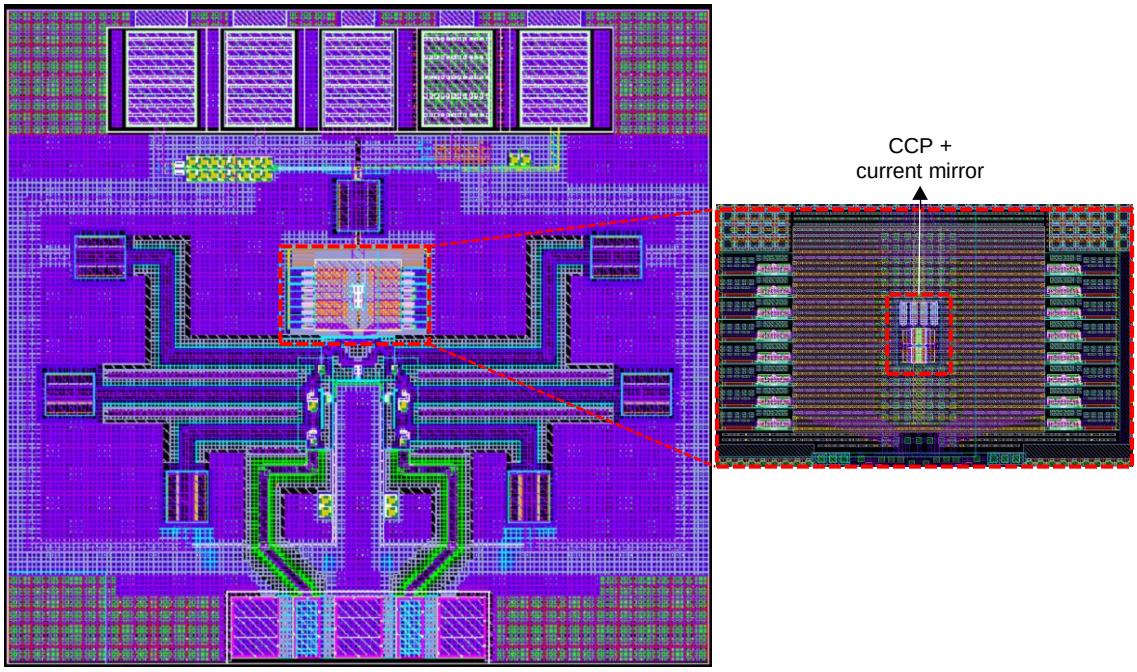


Figure 72 – Shifted CCP VCO layout plus the tank in detail. Source: author.

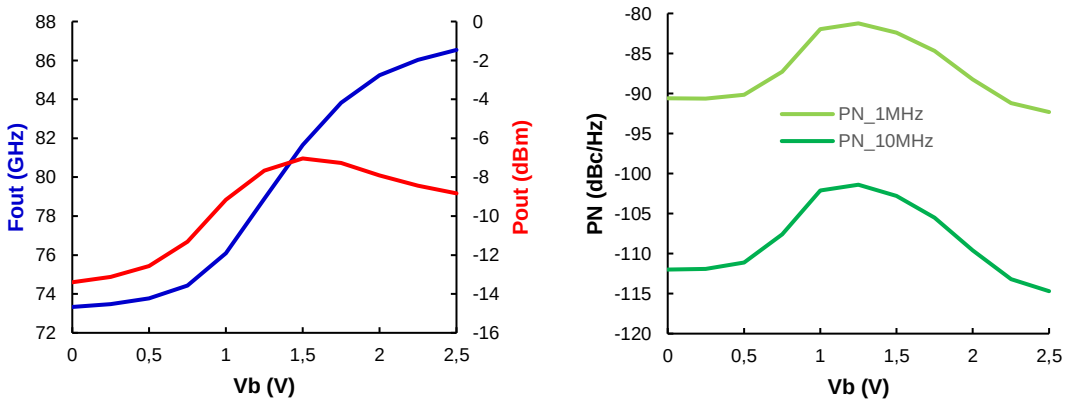


Figure 73 - Post-layout simulation results of the shifted CCP VCO, showing the output frequency (blue) and power (red), as well as the phase noise at 1 MHz offset (light green) and at 10 MHz (dark green). Source: author.

Table 26 - Post-layout results summary for the shifted CCP VCO.

	Final design (I_{BIAS} = 19 mA)
Central F_{osc}	80 GHz
FTR	13.1 GHz (16.3 %)
PN @ 10 MHz (V_b = 0 V)	-116.1 dBc/Hz
PN @ 10 MHz (V_b = 1.25 V)	-103.8 dBc/Hz
PN @ 10 MHz (V_b = 2.5 V)	-115.5 dBc/Hz
P_{out} (V_b = 0 V)	-13.4 dBm
P_{out} (V_b = 1.25 V)	-7.7 dBm
P_{out} (V_b = 2.5 V)	-8.8 dBm
FOM	-178 dB
RF efficiency (V_b = 1.25 V,	0.46 %

3.5.6 DISTRIBUTED CCP VCO

The design of the distributed CCP VCO starts by defining the method of distribution: homogeneous or tapered.

For the homogeneous distribution, the lumped CCP R_{neg} is divided equally across the resonator, so each sub-cell has R_{neg}/n. The CCP W, thus, is determined by finding the W that gives the required R_{neg}/n. If the Z_{in_cl} is smaller for any reason, the CCPs are equally adjusted until the Z_{in_cl} reaches the same values seen on the reference case VCO.

For the tapered distribution, the design procedure is empiric, as the adjustment of a CCP changes the equivalent losses seen by the other CCPs, thus leading to a recursive problem. To avoid this, the design of the tapered, distributed CCP VCO was done by conducting a parametric sweep of a number of combinations of the CCP Ws and choosing the combination that results in the widest FTR while maintaining the same Z_{in_ol} as the reference case VCO.

Because of area constraints, only one distributed CCP VCO prototype could be submitted to the tape-out, so a preliminary comparison had to be made. To decide which method would be laid out, a schematic-level comparison between the two distribution methods was carried out. The 8-segment long S-CPS resonator was loaded with 4 CCP cells in each case, each CCP cell spaced by 2 segments (14.4 µm) from each other. Intermediate results showed that the CCP closest to the short-circuit termination has little to no effect on the loss compensation, and was thus removed. The final placement configuration is shown in Figure 74. After running a set of exhaustive parametric sweeps in both uniform and tapered distributions, the best-performing designs were found. The central F_{osc}, FTR, IDC and Ws of the individual CCPs are displayed in Table 27.

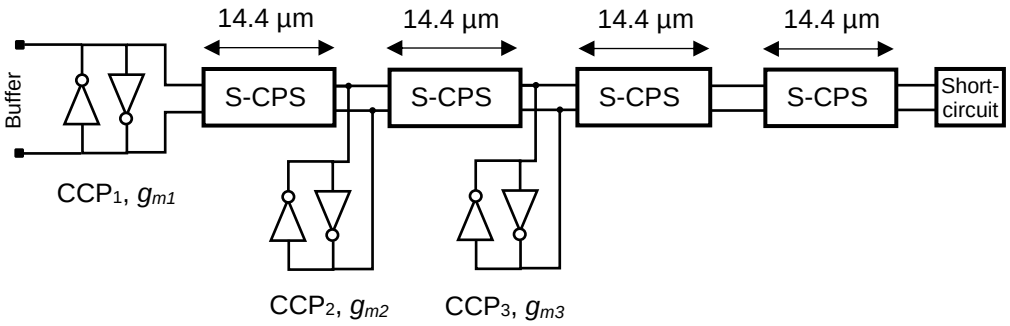


Figure 74 - Schematic representation of the distributed CCP VCO. Source: author

Table 27 - Design and performance parameters of the VCO core using the uniform and tapered distributed CCPs. Source: author.

	Uniform	**Tapered**
CCP pitch	2*7.2 µm = **14.4 µm**	
Central F_{osc}	78.45 GHz	79.25 GHz
CCP W_1+ W_2+ W_3	11+11+11	16+10+4
I_{DC}	13.2 mA	12 mA
FTR **(%, GHz)**	16.89 %, 13.25 GHz	17.54 %, 13.9 GHz

The tapered distribution displays lesser capacitive loading overall, which is inferred by the higher central F_{osc} and wider FTR. Also, it requires less DC current (I_{DC}) to result in the same amount of loss compensation. Thus, it was chosen as the best candidate to implement the CCP distribution.

The VCO was then laid out to have its parasitics extracted. The final layout and the tank are presented in Figure 75. The die dimensions are exactly the same as the reference case VCO, i.e. 747 µm x 647 µm, as the ground plane and biasing pads were re-used. The PLS results for the distributed CCP VCO are presented in Figure 73, and summarized in Table 28.

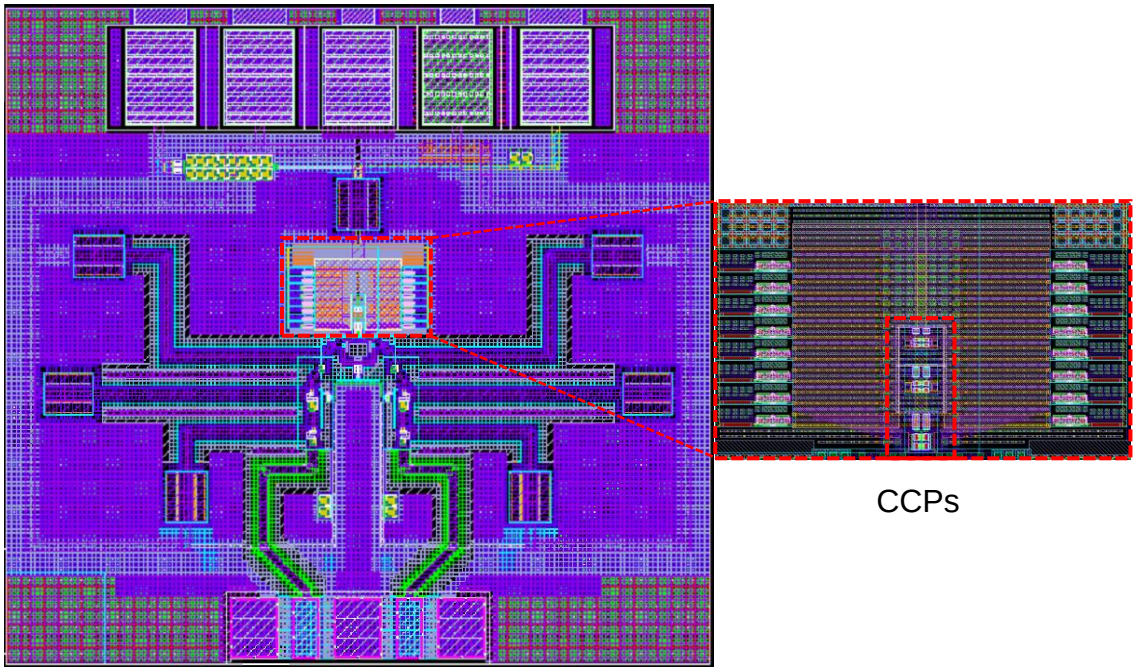


Figure 75 - Distributed CCP VCO layout plus the tank in detail. Source: author.

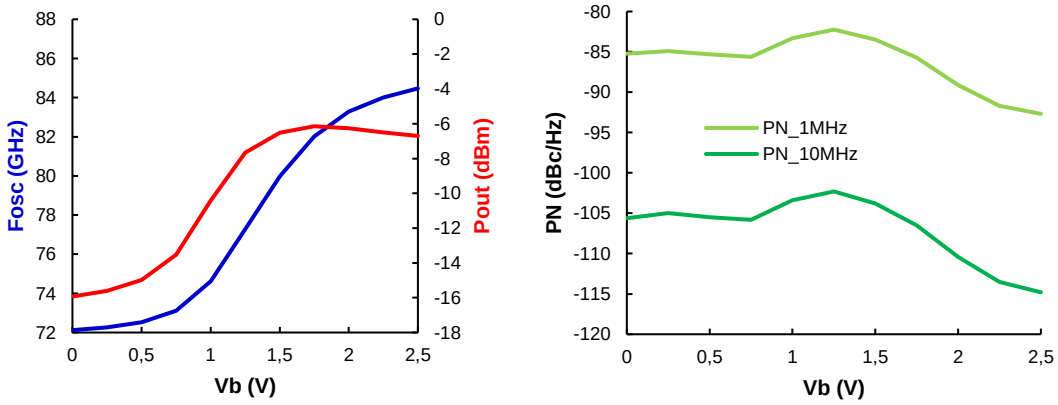


Figure 76 - Post-layout simulation results of the distributed, tapered CCP VCO, showing the output frequency (blue) and power (red), as well as the phase noise at 1 MHz offset (light green) and at 10 MHz (dark green). Source: author.

Table 28 - Summary of the post-layout simuation results of the ditributed, tapered CCP VCO.

	Final design (I_{BIAS} = 15 mA)
Central F_{osc}	78.3 GHz
FTR	12.4 GHz (15.8 %)
PN @ 10 MHz (V_b = 0 V)	-105.6 dBc/Hz
PN @ 10 MHz (V_b = 1.25 V)	-102.3 dBc/Hz
PN @ 10 MHz (V_b = 2.5 V)	-114.8 dBc/Hz
P_{out} (V_b = 0 V)	-15.93 dBm
P_{out} (V_b = 1.25 V)	-7.7 dBm
P_{out} (V_b = 2.5 V)	-6.7 dBm
FOM	-181 dB
RF efficiency (V_b = 1.25 V,	0.72 %

3.5.7 SHIFTED, DISTRIBUTED CCP VCO

The design of the shifted, distributed CCP VCO is very similar to the design of the distributed CCP VCO presented in subsection 3.5.6. The design method starts with determining the offset from the open-circuit termination and the distance between each CCP. Then, the W of each CCP is determined by running an exhaustive parametric sweep of the individual CCP W in Virtuoso ADE L, and the combination of Ws that produce the widest FTR are chosen.

The final placement configuration is shown in Figure 77. After running a set of exhaustive parametric sweeps using the tapered distribution, the best-performing design was found. The central F_{OSC}, FTR, I_{DC} and Ws of the individual CCPs are displayed in Table 29.

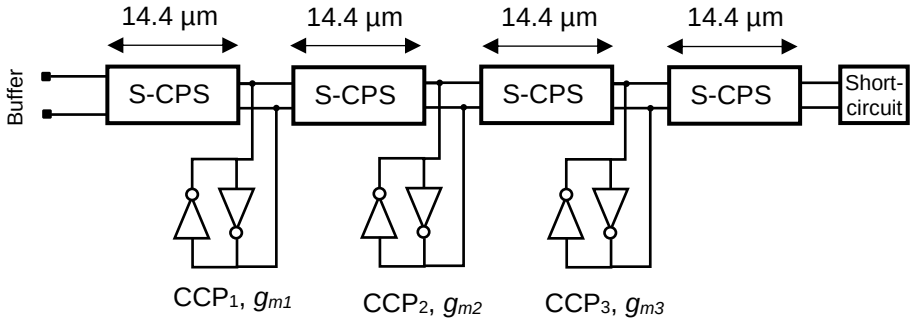


Figure 77 - Schematic representation of the shifted, distributed CCP VCO. Source: author.

Table 29 - Resonator core of the shifted, distributed CCP VCO.

	Shifted, tapered CCP
CCP pitch	2*7.2 µm = **14.4 µm**
Central F_{osc}	78.45 GHz
CCP W_1+ W_2+ W_3 (µm)	18+16+4
I_{DC}	19 mA

The VCO was then laid out to have its parasitics extracted. The final layout and the tank are presented in Figure 78. The die dimensions are exactly the same as the reference case VCO, i.e. 747 µm x 647 µm, as the ground plane and biasing pads were re-used. The PLS results for the distributed CCP VCO are presented in Figure 79, and summarized in Table 28.

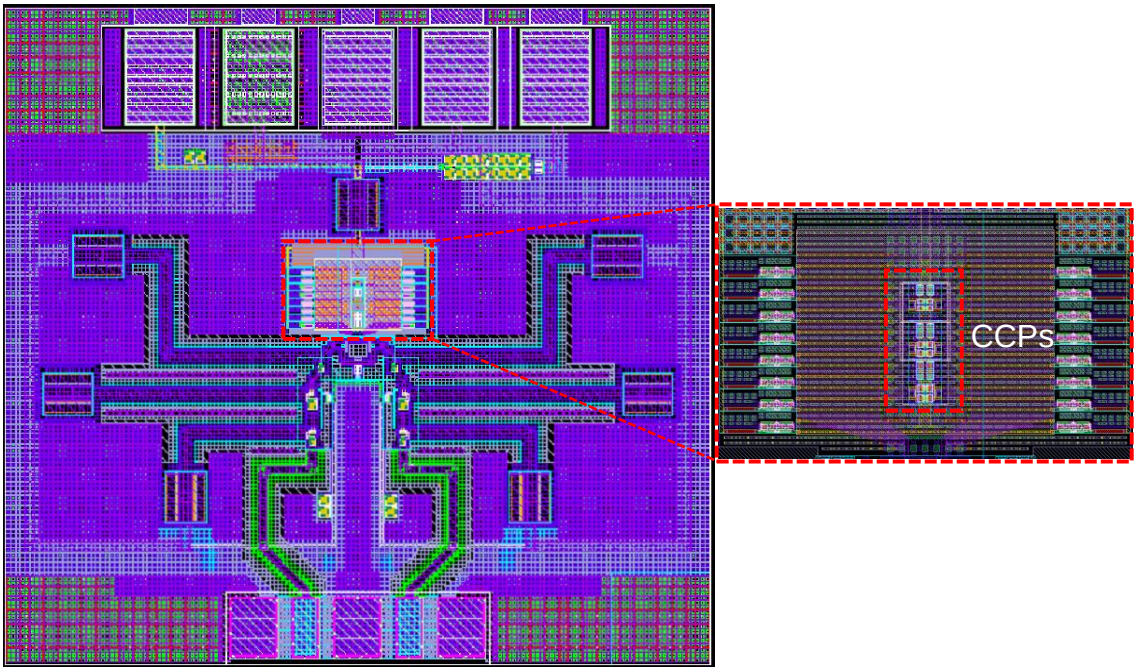


Figure 78 – Shifted, distributed CCP VCO layout plus the tank in detail. Source: author.

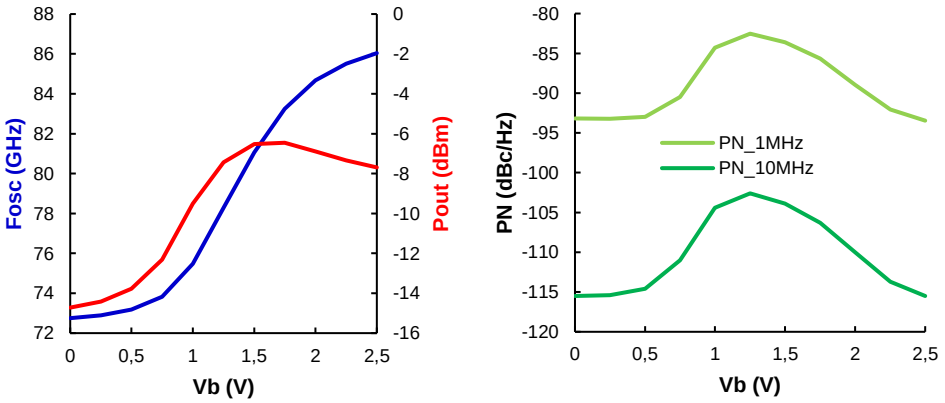


Figure 79 - Post-layout simulation results of the shifted and distributed, tapered CCP VCO, showing the output frequency (blue) and power (red), as well as the phase noise at 1 MHz offset (light green) and at 10 MHz (dark green). Source: author.

Table 30 - Summary of the post-layout simuation results of the shifted, ditributed CCP VCO.

	Final design (I_{BIAS} = 19 mA)
Central F_{osc}	79.4 GHz
FTR	13.3 GHz (16.7 %)
PN @ 10 MHz (V_b = 0 V)	-115.5 dBc/Hz
PN @ 10 MHz (V_b = 1.25 V)	-102.6 dBc/Hz
PN @ 10 MHz (V_b = 2.5 V)	-115.5 dBc/Hz
P_{out} (V_b = 0 V)	-14.7 dBm
P_{out} (V_b = 1.25 V)	-7.4 dBm
P_{out} (V_b = 2.5 V)	-7.7 dBm
FOM	-180 dB
RF efficiency (V_b = 1.25 V,	0.55 %

3.5.8 COMPARISON OF THE DESIGNED VCOS

Having designed, laid out and simulated all four variations, their performance are now compared to assess the strengths and weaknesses of each approach. The central F_{OSC}, FTR, DC current consumption from the VCO core, best-case phase-noise, FOM and DC to RF efficiency are summarized in Table 31.

Table 31 - Performance summary of the each VCO designed for the CCP distribution study.

	Reference case	**Shifted CCP**	**Distributed CCP**	**Dist. Shifted CCP**
Central F_{osc}	78.9 GHz	80 GHz	78.3 GHz	79.4 GHz
FTR	11.6 GHz (14.7 %)	13.1 GHz (16.3 %)	12.4 GHz (15.8 %)	13.3 GHz (16.7 %)
I_{DC}	12 mA	19 mA	15 mA	19 mA
PN @ 10 MHz (Best case)	-116.1 dBc/Hz	-116.1 dBc/Hz	-114.8 dBc/Hz	-115.5 dBc/Hz
FOM (Eq. (2)	-182 dB	-178 dB	-181 dB	-180 dB
RF eff. (Eq. (3))	1 %	0.46 %	0.72 %	0.55 %

The FOM of each oscillator did not depart far from the -180 dB mark, which shows that every design is an excellent-performance VCO. However, the reference case displays the best FOM, at -182 dB.

The VCOs that displayed the best FTRs are the ones where the CCP was shifted in some way, this shows that indeed removing the loading C_{CCP} from the open-circuit termination does improve the tuning performance of the VCO, at the cost of increased DC power consumption. The design that has the best FTR, the shifted and distributed CCP, also displays the highest DC power consumption.

Distributing the CCP does improve the FTR, also at the cost of increased DC power consumption: for the same level of compensation, the reference case VCO has a FTR of 14.7 % at a DC bias of 12 mA, the distributed CCP, on the other hand, has a FTR of 15.8 % at a DC bias of 15 mA.

Shifting and distributing the CCP appears to bring the best characteristics of both methods in a single design, giving back some DC to RF efficiency to the shifted CCP while actually improving the FTR of the purely distributed CCP.

3.5.9 DISCUSSIONS

Shifting and distributing the CCP across the distributed S-CPS resonator has potential to be the best way to improve the performance of the classical, single CCP VCO. It increases the FTR of the VCO at the cost of greater DC power consumption when compared to the reference case VCO. However, it displays better DC to RF power efficiency than the shifted, lumped CCP and better FTR than the distributed CCP.

The design method for these VCOs, however, is still very basic, as no global optimization procedure could be employed. Thus, no guarantee can be made regarding the optimization of the VCO as a whole. The placement of each CCP, the offset calculation and tapering method still need to be equated and introduced into a proper, automated design algorithm. This, indeed, is left as a suggestion for future works that may derive from this thesis.

3.6 BUFFERLESS VOLTAGE CONTROLLED OSCILLATOR

Having dealt with the optimization of the resonator, and having acquired enough understanding of its functioning and modelling, the attention falls now to the output buffers. Specifically, the question is “would it be possible to extract power directly from the tank”, thus removing the effects on the VCO that may happen because of this. This section present the concept, modelling and design algorithm for this novel, bufferless S-CPS VCO, as well as a comparison to the already discussed buffered VCOs.

3.6.1 WORKING PRINCIPLE

The working principle of the bufferless VCO derives directly from the discussion of the voltage and current distribution across a λ/4 resonator presented at section 3.5.1. Each point across the standing-wave resonator has an intrinsic impedance, and placing a load connected directly on it affects these distributions. The immediate effect is, of course, the disturbance of the equivalent losses seen by the CCP. The VCO model with inclusion of an external load is shown in Figure 80

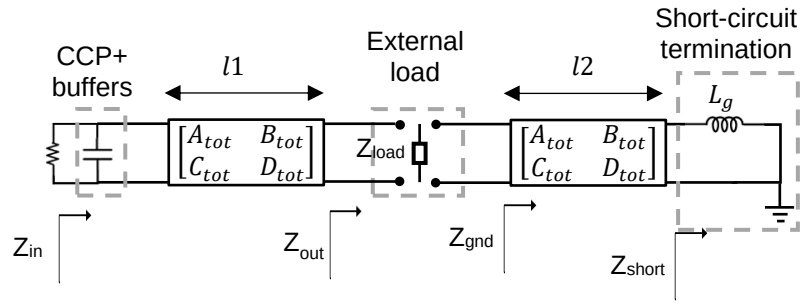


Figure 80 – Bufferless resonator model, which is based on the shifted CCP model presented in Figure 69. Source: author.

Z_{in}, the impedance at the open-circuit termination, seen by the CCP, is given by:

$$Z_{in} = Z_C \cdot \frac{Z_{out} + Z_C \cdot \tanh(\gamma \cdot l_1)}{Z_C + Z_{out} \cdot \tanh(\gamma \cdot l_1)} \tag{39}$$

where:

$$Z_{out} = \frac{(2 \cdot Z_L) \cdot Z_{gnd}}{(2 \cdot Z_L) + Z_{gnd}} \tag{40}$$

$$Z_{gnd} = Z_C \cdot \frac{Z_{Short} + Z_C \cdot \tanh(\gamma \cdot l_2)}{Z_C + Z_{Short} \cdot \tanh(\gamma \cdot l_2)} \tag{41}$$

$$Z_{Short} = \omega L_g \tag{42}$$

Z_C and γ are the varactor-loaded S-CPS characteristic impedance and propagation constant, respectively. Z_{load} can be complex and depends on the circuit that the VCO couples to. The output impedance of the tank has a negative real part in closed-loop, because of the negative resistance given by the CCP. The position, however, can in theory be designed to match the tank output impedance in open-loop, maximizing the power transfer.

3.6.2 BUFFERLESS VCO DESIGN

Should the CCP be implemented as a single, lumped CCP, the design of the bufferless VCO uses the same optimized design presented at Section 3.4.3, where the resonator losses calculation uses the correction given by Equation (*39*). The goal of the design algorithm is to find L_{en} of the resonator, the W of the CCP and to estimate the FTR. The inputs are: a table containing C_v and Q_v, as well as their minimum and maximum values, of all varactors having W_f = 1.5 µm and N_f = 1; an optimized S-CPS; a table containing R_{neg} and C_{CCP} versus MOSFET W and I_{BIAS}; the distance between the output and the open-circuit termination L_{off}; and finally, a f_{des}.

After L_{en} is determined, the bufferless resonator is simulated in HFSS to

futher refine the accuracy and its RLRC model is build in Cadence Virtuoso. Then, the CCP is laid out to extract the actual parasitics. Finally, the oscillation frequency and phase noise are determined by post-layout harmonic balance simulation in Spectre ADE L tool. The basic bufferless VCO schematic is shown in Figure 81.

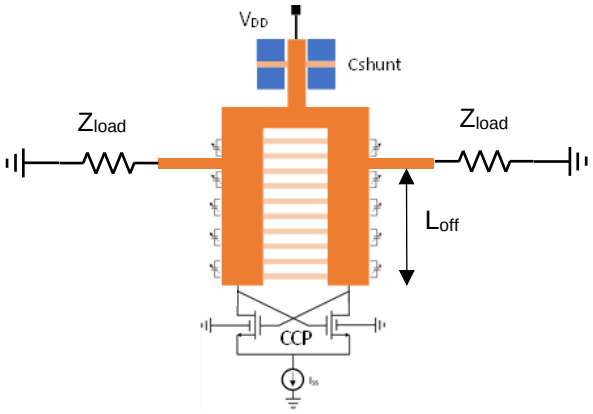


Figure 81 - Basic bufferless VCO schematic showing the CCP, the biasing current source, the loaded S-CPS resonator and the load impedance on each half of the resonator. Source: author.

3.6.3 VCO RESULTS

Three designs were proposed to verify the modelling and the accuracy of the design method. The first design is exploratory, it uses the same results from the optimal, lumped CCP presented in section 3.4.4, where L_{off} is changed to find an optimal power match to the spectrum analyzer load. The second design uses the tapered CCP configuration presented in section 3.5.6 to implement the loss compensation in order to maximize the FTR. The third design is a variation of the second, where the output is taken directly at the short-circuit network, thus maximizing L_{off}, in order to minimize the loading on the tank. Starting with the first bufferless design, Table 32 shows the parameters of the resonator and CCP.

Table 32 – Final design parameters of the first bufferless VCO, including the S-CPS resonator and CCP data.

Parameter	Value
Len	9*7.2 µm = **64.8 µm**
L_{off}	7*7.2 µm = **50.4 µm**
W_f	1.535 µm
L_f	0.395 µm
nb_cell	3
CCP W	21 µm
I_{BIAS}	6.3 mA

R_{neg}	-197 Ω
C_{par}	36.6 fF

They are essentially the same as shown in Table 20, only with the addition of L_{off}, which was found by running a load-pull simulation across the S-CPS resonator to find the point where the oscillations start. The L_{off} was then chosen 7.2 µm larger than the point where the oscillations started. After laying out all important interconnections, the VCO core was re-simulated to assess its electrical performance. The PLS was carried out in CADENCE Virtuoso design suite using spectre and ADE L tool and Quantus PEX and PVS tools. The simulations that were carried out are harmonic balance simulations plus noise, intending to extract the output frequency, output power and phase noise of the oscillator. The PLS results for the first bufferless VCO are presented in Figure 86.

The observed F_{osc} is 80 GHz, and the output frequency excursion falls between 76.1 GHz and 83.8 GHz, translating to a FTR of 7.7 GHz, or 9.6 %. The output power and phase noise of this design are from -9.4 dBm to -5.3 dBm and from -111 dBc/Hz to -103.8 dBc/Hz, respectively.

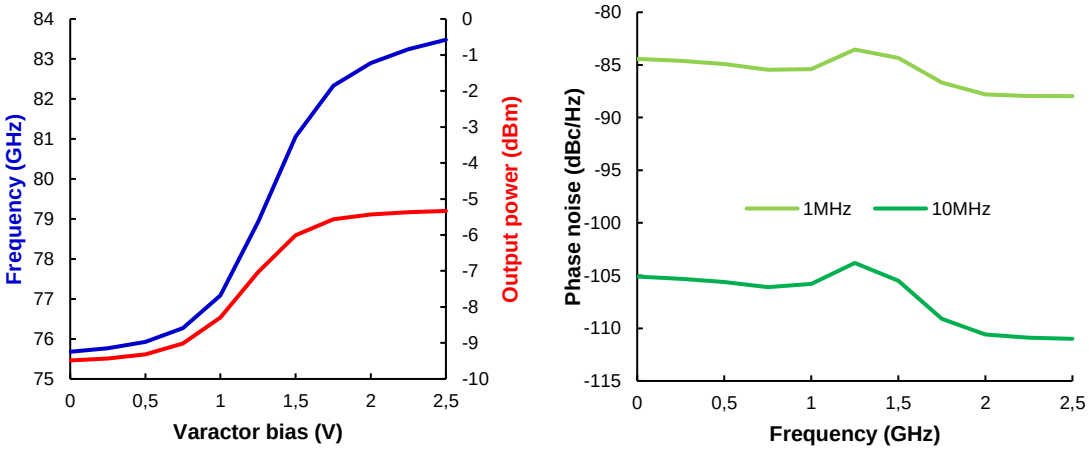


Figure 82 – Post-layout simulation results of the first bufferless VCO, showing the output frequency (blue) and power (red), as well as the phase noise at 1 MHz offset (light green) and at 10 MHz (dark green). Source: author.

Having the VCO core designed and laid out, the next step was to lay out the DC biasing network, the RF output and ground plane. The layout for the die is presented in Figure 83. The total die area, accounting the DC and RF pads, is 0,227 mm^2, 486 µm x 468 µm.

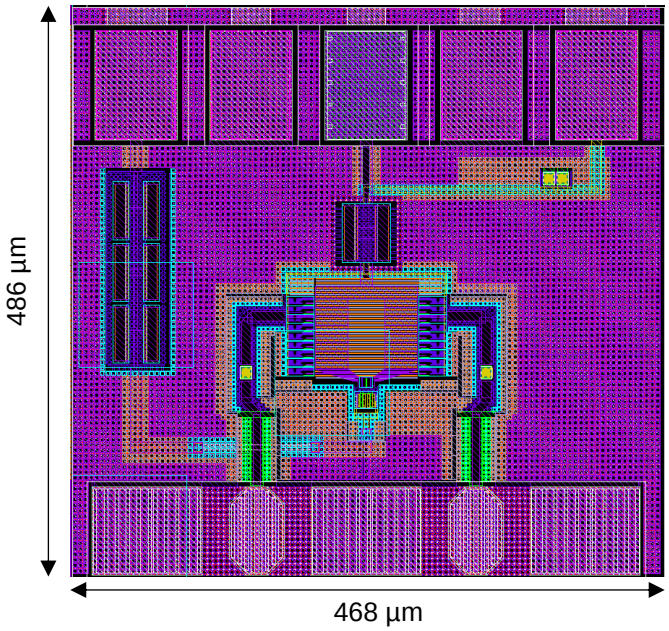


Figure 83 – First bufferless VCO layout, containing the RF pads, DC pads and the VCO core. Source: author.

The two following designs were carried out to maximize the FTR of the VCO. Following the encouraging results presented at section 3.5.6, a target FTR of 15% was used to design the base S-CPS resonator, assuming the load of a single CCP at the open-circuit termination. This resonator was shared between the two designs to facilitate the performance comparison. Then, the loss compensation was designed using the distributed and tapered CCP configuration. This design was carried out using the same procedure presented in section 3.5.6, with the addition of the loading corrections presented in section 3.6.2.

The difference in these two designs is the value of L_{off}. In the second design, L_{off} is one of the design variables to be swept with the CCPs W, the design being chosen as the one that fulfills the target FTR and a DC biasing current below 20 mA. In the third design, L_{off} was fixed as L_{off} = L_{en} and the loss compensation was designed with that constraint. For all designs, a biasing current density of 0.2 mA/µm and K = 2 was considered: this alleviates the capacitive loading on the tank, enabling a higher maximum FTR. Table 33 shows the parameters of the resonator core and CCPs for the two final designs.

Table 33 – Final design parameters of the second and third bufferless VCO designs.

Parameter	Second design	Third design
Len	6*7.2 µm = **64.8 µm**	6*7.2 µm = **64.8 µm**
L_{off}	5*7.2 µm = **50.4 µm**	6*7.2 µm = **64.8 µm**

W_f	1.5 µm	
L_f	0.9 µm	
nb_cell	4	
CCP W	26 µm + 19 µm	26 µm + 14 µm
I_{BIAS}	18 mA	16 mA

After laying out all important interconnections, the VCO core was re-simulated to assess is electrical performance. The PLS were carried out in CADENCE Virtuoso design suite using spectre and ADE L tool and Quantus PEX and PVS tools. The simulations that were carried out are harmonic balance simulations plus noise, intending to extract the output frequency, output power and phase noise of the oscillator. The PLS results for the two bufferless VCOs are presented in Figure 84. Both circuits are biased at 0.25 mA/µm, translating to 22.5 mA for design 2 and 20 mA for design 3.

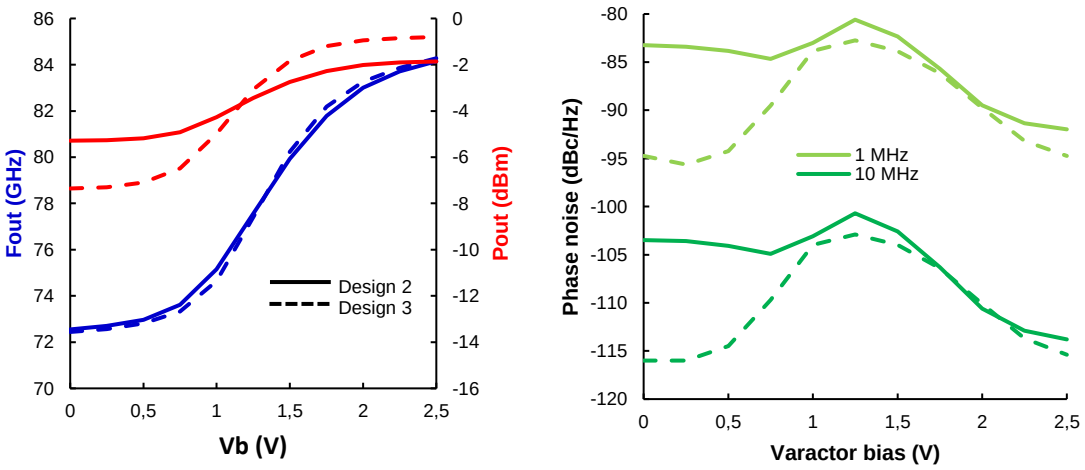


Figure 84 – Post-layout simulation results of the second (solid line) and third (dashed line) bufferless VCO designs, showing the output frequency (blue) and power (red), as well as the phase noise at 1 MHz offset (light green) and at 10 MHz (dark green). Source: author

The observed F_{osc} for both VCOs is 78.4 GHz. The output frequency excursion is very similar for both designs, falling between 72 GHz to 84 GHz, translating to an approximate FTR of 12 GHz, or 15 %. The output power for design 2 varies between -7.4 dBm and -0.8 dBm, and between -5.3 dBm and -1.9 dBm for design 3. The phase noise of design 2 is falls between -100.7 dB and -113.8 dB, while for design 3 it falls between -102.9 dB and -116 dB.

Having the VCO core designed and laid out, the next step was to lay out the

DC biasing network, the RF output and ground plane. The layout for the dies is presented in Figure 85. The total die area of each VCO, accounting the DC and RF pads, is 0,214 mm^2, 486 µm x 441 µm.

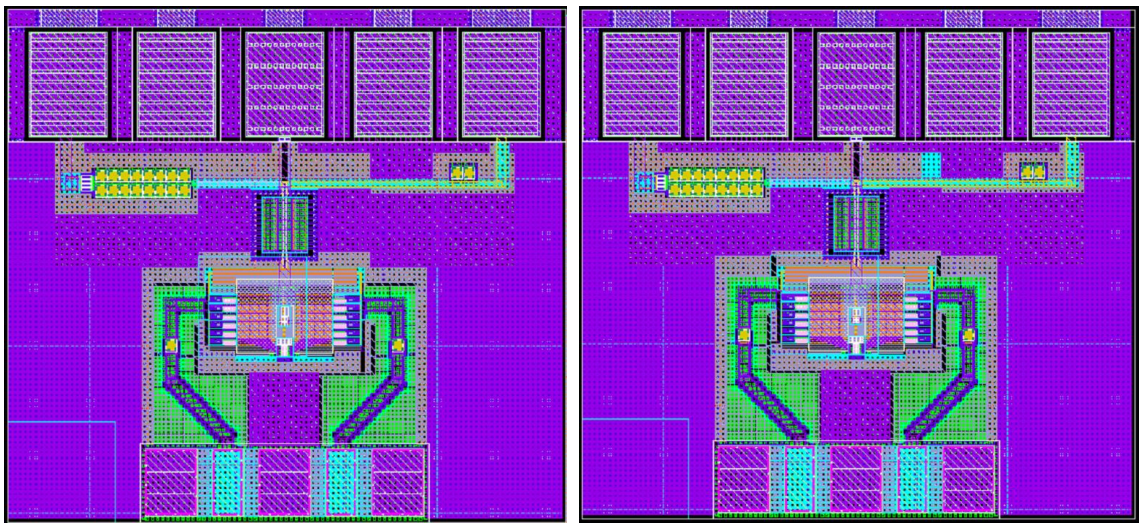


Figure 85 – Second (left) and third (right) bufferless VCO layouts, containing the RF pads, DC pads and the VCO core. Source: author.

3.6.4 DISCUSSIONS

Omitting the output buffer from the VCO core has a global effect of increasing the DC-to-RF efficiency. Even though the necessary g_m to cancel the R_{loss} increases because of the load, the increase is less than the current consumed by the buffers. This effect can be seen in Table 34, which summarizes the performance of a buffered and a bufferless version of the same resonator. The efficiency gain of the VCO has a price of worsened phase noise, because of the larger equivalent losses of the resonator, but the output power level is increased. Also, the area occupied by the bufferless VCO is about half of that occupied by the buffered version: 0.416 mm^2 for the buffered VCO versus 0,227 mm^2 for the bufferless, including the same RF and DC pads.

Table 34 – Performance summary of the first bufferless VCO design and its buffered counterpart.

	Buffered design	**Bufferless**
Central F_{osc}	80.3 GHz	80 GHz
FTR	8.0 GHz (10 %)	7.7 GHz (9.6 %)
PN @ 10 MHz (V_b = 0 V)	-114.4 dBc/Hz	-105 dBc/Hz
PN @ 10 MHz (V_b = 1.25 V)	-106.3 dBc/Hz	-103.8 dBc/Hz
PN @ 10 MHz (V_b = 2.5 V)	-113.1 dBc/Hz	-111 dBc/Hz

P_{out} (V_b = 0 V)	-8.6 dBm	-9.4 dBm
P_{out} (V_b = 1.25 V)	-7.6 dBm	-7.0 dBm
P_{out} (V_b = 2.5 V)	-7.9 dBm	-5.3 dBm
FOM	-184.6 dB	-182.5 dB
RF efficiency (V_b = 1.25 V, VCO plus buffers)	0.7 %	3.9 %

The position of the load affects the equivalent losses seen by the CCP, as shown in section 3.6.2. Thus, increasing L_{off} would result in increasingly smaller W, and I_{BIAS}, but also in smaller available output power. This is seen in Table 35, which summarizes the performance parameters of the two bufferless VCOs with different L_{off}.

Table 35 – Performance summary of the second and third bufferless VCO designs.

	Design 2	**Design 3**
Central F_{osc}	78.4 GHz	78.4 GHz
FTR	11.8 GHz (15.1 %)	11.6 GHz (14.8 %)
PN @ 10 MHz (V_b = 0 V)	-103.5 dBc/Hz	-116 dBc/Hz
PN @ 10 MHz (V_b = 1.25 V)	-100.7 dBc/Hz	-102.9 dBc/Hz
PN @ 10 MHz (V_b = 2.5 V)	-113.8 dBc/Hz	-115.4 dBc/Hz
P_{out} (V_b = 0 V)	-7.4 dBm	-5.3 dBm
P_{out} (V_b = 1.25 V)	-3.1 dBm	-3.4 dBm
P_{out} (V_b = 2.5 V)	-0.8 dBm	-1.9 dBm
FOM	-177.4 dB	-180.1 dB
RF efficiency (V_b = 1.25 V, VCO plus buffers)	3.1 %	2.7 %

The FTR of both VCOs is very similar, even though the phase noise profile and power output change: the design 2 VCO has higher equivalent R_{loss} than the design 3, which is seen in the higher phase noise at minimum output frequency, and by the decreased FOM. However, setting the output directly on the short-circuit termination decreases the DC-to-RF efficiency of the VCO, because of the smaller power available to source the load. The efficiency would indeed increase if the output of the S-CPS resonator matched the 50 Ω load, but the equivalent R_{loss} in this case might result in an impossible design, since the required CCP would be too large, the capacitive loading would shorten the resonator and heavily impact the FTR.

Nevertheless, the concept of taking the power directly from the S-CPS

resonator has been successfully demonstrated, along with its virtues and shortcomings. To summarize: the bufferless VCO has improved power efficiency and requires smaller die surface at the cost of phase noise and FTR performance.

3.7 BAND-SWITCHING, COUPLED-RESONATOR STANDING-WAVE OSCILLATOR BASED ON TUNABLE S-CPS TRANSFORMER

The last design proposal on the distributed S-CPS resonator is a multi-band VCO, whose resonator is a S-CPS tunable transformer. The primary, a varactor-loaded S-CPS, controls the F_{OSC} in a continuous way, just like the previous designs. The secondary, a variable S-CPS inductor controlled by switches, controls the oscillation band in a coarse, binary way. By adding the two control methods, a broadband VCO can be obtained.

This section presents the design of the resonator, explaining in detail the design of the tunable S-CPS transformer and switches, as well as the proposed electrical model for them, and the design of the VCO core, including the CCP. Then, the final layout and PLS results are presented.

3.7.1 WORKING PRINCIPLE

The resonators presented so far were based on a λ/4 resonator built around a tunable S-CPS, whose electrical length is changed by the distributed varactors that load the S-CPS. This structure, although flexible, is limited in FTR by the large losses that big varactors introduce in the R_{loss}. The larger R_{loss} results in larger CCPs, which loads the S-CPS resonator more heavily, thus limiting the FTR. Thus, the designer has to resort to other methods if the goal is to design a broader-band VCO.

The idea of a transformer-based resonator is not novel, and a number of VCOs do utilize this method to realize multi-band oscillators. The band-switching methods include capacitor bank switching [66] or variable secondary inductance, that is controlled by switches [67]. Since the varactor control takes care of the capacitance tuning with great efficiency, the band-switching method chosen for the S-CPS implementation is the variable inductor. The novelty of this design is the implementation of the transformer, which is based on slow-wave transmission

lines, and the switch itself that uses monolithic PIN diodes instead of MOSFETs for improved performance.

3.7.2 TUNABLE S-CPS TRANSFORMER MODEL

The tunable S-CPS transformer is a multi-layer device, divided into four different regions of interest. Each region was modelled separately. The first region of interest, called **region 1**, is the portion of primary (M8 resonator) that does not couple into the secondary. The second region, called **region 2**, is the portion of the secondary (Alucap resonator) that is not affected by the EM coupling to the primary. The third region, called **region 3**, is the region where primary and secondary are stacked on each other, where the intended EM coupling happens. The final and fourth region, called **region 4**, models the parasitic, fringing field coupling between primary and secondary, which happens at the short-circuit terminations of both primary and secondary. The basic layout for the transformer and the equivalent model for regions 1 to 3 are presented in Figure 86.

Regions 1 and 2 are modeled after the equivalent lumped RLRC model for the S-CPS transmission line, which are presented in section 3.2 (the unloaded S-CPS line) and section 3.3.1 (the varactor-loaded S-CPS line). The model parameters are simply renamed to express the exact layer that the signal and ground lines are routed. For example, R_{S_M8} is the series resistance of the primary, routed using M8, as R_{S_AP} is the same series resistance at the secondary, routed using Alucap (AP). The coupled section of the tunable S-CPS transformer, region 3, is realized by the vertical coupling between the M8 primary and the AP secondary. The coupling between these two different conductive layers happens, thus, via the inter-strip capacitance and the mutual inductance between them, which are introduced into the model by the mutual inductance M_{M8_AP} and by the distributed interstrip capacitance C_{S_M8AP}. The equivalent model of these three regions covers a length of $Nseg * (SS + SL) = 7.2\ \mu m$, which is the length that is controlled by each pair of varactors.

The model for region 4, however, has to take into consideration the other regions because it reflects the exact interaction between them, and the parasitic elements and EM coupling between them. These parasitic couplings are: the magnetic coupling between the short-circuit terminations of both primary and

secondary (M_{F_SC}), the fringe coupling between primary and secondary (M_{F_APM8}) and between secondary and primary (M_{F_M8AP}). The capacitive coupling between primary and secondary (C_{C_APM8}) and between secondary and primary (C_{C_M8AP}) are also included. The short-circuit terminations self-inductances (L_{SC_M8} and L_{SC_AP}) and the excess inductance between regions 4 and 2 (L_{CONN}) are also included. This model is presented in Figure 87.

The determination of the values for the S-CPS parameters follow the same methods described at section 3.2. The determination of the mutual inductances, however, depends on the exact configuration of the secondary inductance, since the resonator implements a switched secondary to create a variable inductor.

The design variables of the tunable S-CPS transformer resonator are: the number of segments of the primary and secondary ($Nsegs_{M8}$ and $Msegs_{AP}$, respectively) and the offset between primary and secondary (Y_C). There is also the W_S, G, SS and SL of the secondary, but, for simplicity, they were kept the same as the primary's. Figure 88 shows the transformer design variables on the basic structure to facilitate the understanding.

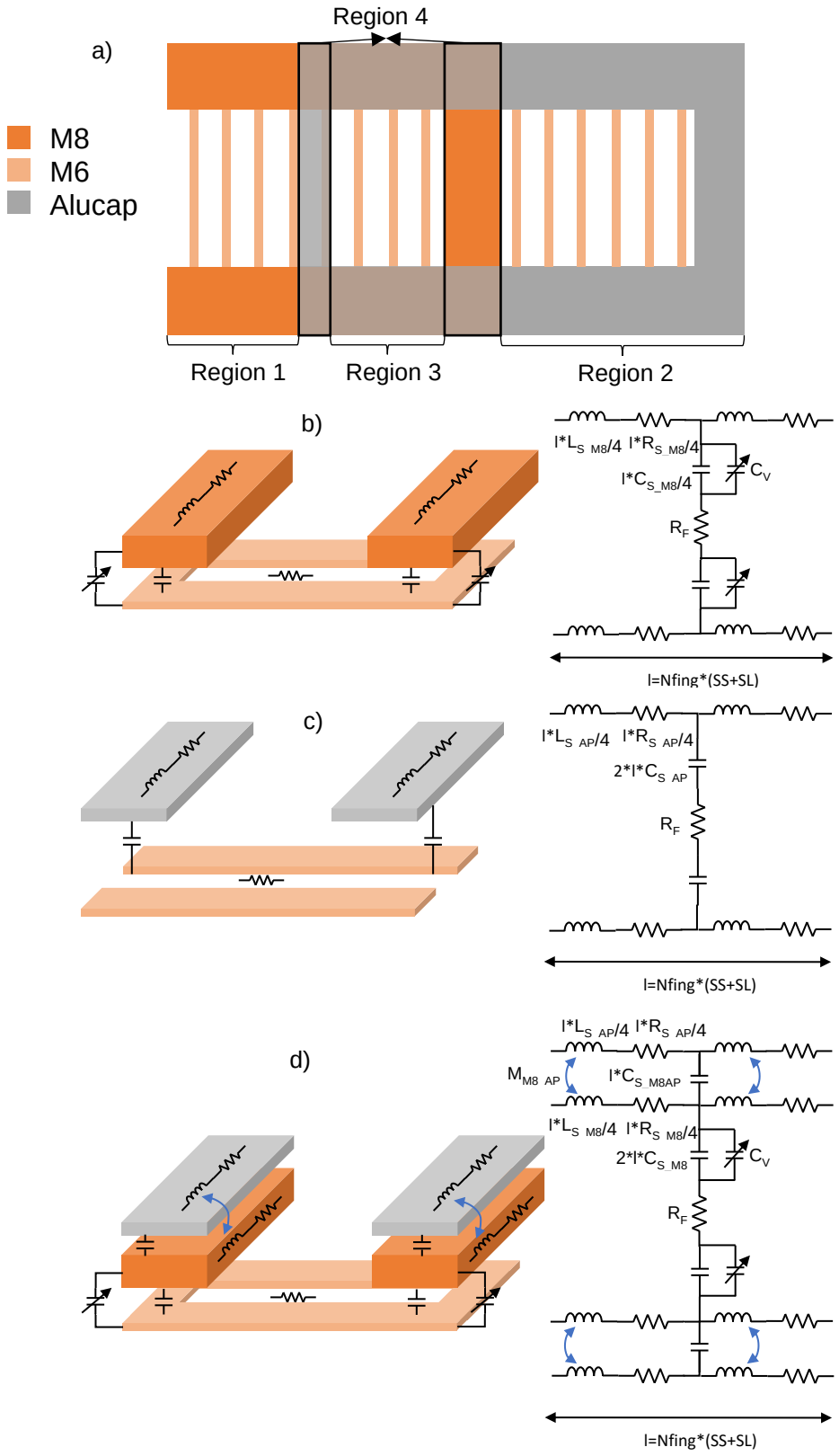


Figure 86 - a) Basic top view of the tunable S-CPS transformer resonator showing the different regions of interest for the equivalent model. b) Cross-section and equivalent model of region 1, the varactor-laden primary that's uncoupled to the secondary. c) Cross-section and equivalent model of region 2, the secondary that's uncoupled to the primary. d) Cross-section and equivalent model of region 3, the overlapping between primary and secondary. Source: author.

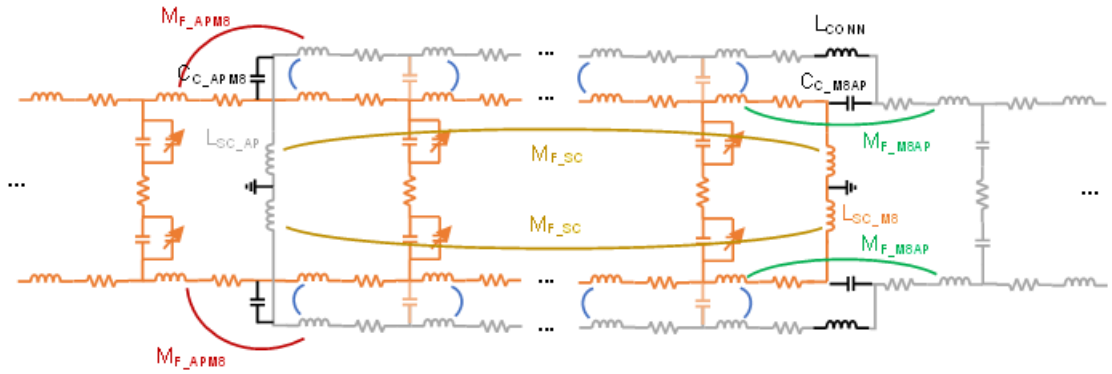


Figure 87 – Equivalent model of region 4, which shows the parasitic electromagnetic couplings between primary (in orange) and secondary (in light grey) as well as interconnection parasitics and the short-circuit terminations of both primary and secondary. Source: author.

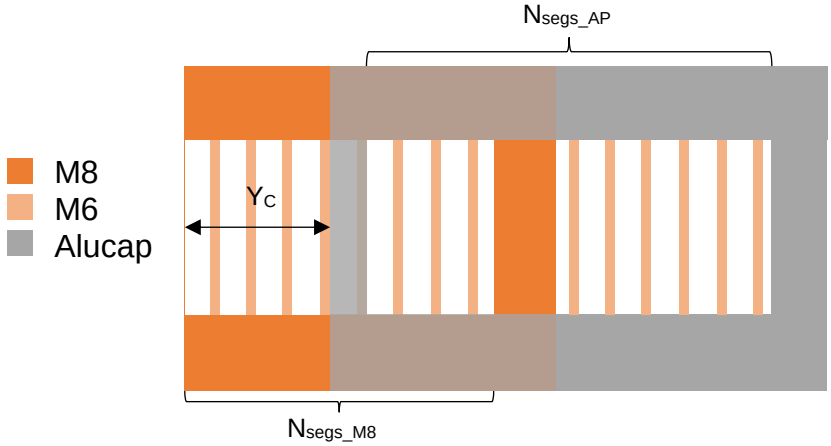


Figure 88 - Tunable S-CPS transformer resonator design variables. Source: author.

3.7.3 CHOICE AND DESIGN OF RF SWITCH

Monolithic switches can be implemented using two families of switches: MEMS electrostatic switches or active switches, such as transistors or diodes.

MEMS switches require specific fabrication processes to enable the realization of air cavities inside the BEOL and/or the etching of the wafer, as well as being high-voltage capable, because of the high activation voltage of these devices, which are in the order of tens of volts up to 100 V. These switches, however, do offer the best RF performance: their on-resistance (R_{on}) is limited by the contact resistance between two different metallic layers, and their off-capacitance (C_{off}) is a function of the separation between the switch terminals. Since the STM 55nm BiCMOS does not offer MEMS fabrication capabilities, they could not be included in the final decision.

Active switches in mainstream CMOS processes rely on n-channel MOSFETs to realize the switching element. On BiCMOS processes, there is also the possibility of employing bipolar transistors, BJTs or HBTs, as switches. The

HBT-based switch profits from the improved RF characteristics of these devices to deliver better-performing switches than their MOSFET-based counterparts: in order to have low R_{on}, a MOSFET has to have a large W, which leads to large parasitic capacitances, increasing C_{off}; bipolar devices have lower conduction resistance because of their intrinsic conduction mechanism, leading to smaller devices which leads smaller C_{off}. Even though the STM 55nm BiCMOS technology does offer both n-channel RF MOSFETs and npn HBTs, only the MOSFETs were considered, the reason being the intrinsic device source-drain symmetry, which simplifies switch design.

In microwave circuits, the device of choice to realize RF switches is the PIN diode, because of their better RF performance when acting as switches. PIN diodes are PN junction diodes where the P and N semiconductors are separated by an intrinsic semiconductor layer. This intrinsic layer introduces a transit time for the charge carriers, and thus a transit cut-off frequency: below this frequency, the PIN diode acts like a normal rectifier diode; above this frequency, the PIN diode acts like a current-controlled resistor. Thus, if the PIN diode is strongly forward-biased, it has very low R_{on}. And because of the larger separation between P and N regions introduced by the intrinsic layer, the C_{off} is small.

The STM 55nm BiCMOS technology offers native PIN diodes[68] in an experimental state, thus these devices were included into the final decision.

The FOM for RF switches is defined as:

$$FOM = \frac{1}{2 \cdot \pi \cdot R_{on} \cdot C_{off}} \tag{43}$$

which is the switch maximum frequency of operation, where the on-state and off-state impedance equals each other.

Since the tunable S-CPS transformer secondary is a low-resistance loop, the switch has to rely on an isolated control signal, otherwise the secondary would simply short out the signal, thus rendering the switch unusable. Using MOSFETs, this problem is trivially solved because of the natural isolation between source/drain and the gate, thanks to the gate oxide. However, since the control signal for the PIN diodes is their anode current, a back-to-back configuration has to be employed. The MOSFET and PIN diode configuration are presented in Figure 89 with the required components for DC biasing.

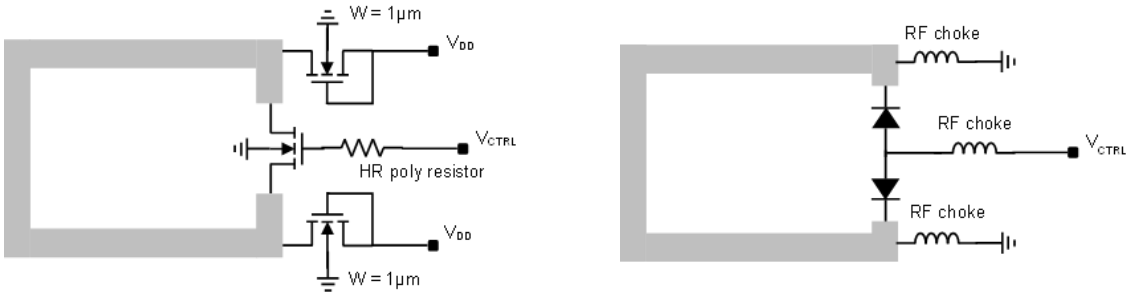


Figure 89 - a) MOSFET-based switch showing the tunable S-CPS transformer secondary and DC biasing components. b) PIN diode-based switch showing the RF chokes used for biasing. Source: author.

In order to choose the best-performing option, the two switches were designed to find the best FOM in either case. The PIN diode layouts and equivalent R_{on}/C_{off} were given by ST Microelectronics based on wafer measurements of their test structures, and from these two different diodes were chosen. Their electrical parameters are shown in Table 36, together with the biasing anode to cathode current (I_{ak}) for the on-state and the anode to cathode voltage (V_{ak}) for the off-state.

Table 36 - On-state resistance, off-state capacitance and the figure of merit of the two PIN diodes chosen to make the RF switches. The biasing conditions of each state are shown as well.

Device\Parameter	$\boldsymbol{R_{on}}$ ($\boldsymbol{I_{ak}}$ = 12 mA)	$\boldsymbol{C_{off}}$ ($\boldsymbol{V_{ak}}$ = 0V)	FOM (fs)
Diode 1	3.5 Ω	15 fF	90
Diode 2	2.5 Ω	25 fF	100

The MOSFET models are included in the PDK and the best-performing W was chosen after an exhaustive parametric sweep. Figure 90 shows the plot of FOM at 80 GHz versus W, considering L = 150 nm, and Table 37 shows the performance data of the best MOSFET.

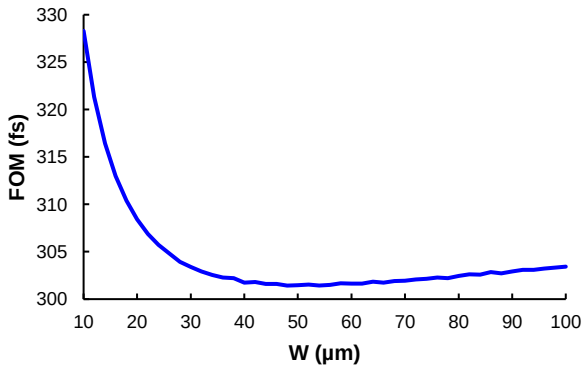


Figure 90 - Figure of merit at 80 GHz of MOSFETs for channel widths between 10 µm and 100 µm. Source: author.

Table 37 - On-state resistance, off-state capacitance and the figure of merit of the best-performing MOSFET. The biasing conditions of each state are shown as well.

Device\Parameter	$\boldsymbol{R_{on}}$ ($\boldsymbol{V_{gs}}$ = 1.2 V)	$\boldsymbol{C_{off}}$ ($\boldsymbol{V_{gs}}$ = 0 V)	FOM (fs)
MOSFET (W = 48 µm)	22 Ω	13.7 fF	301

Even though the MOSFET show lower C_{off} than the PIN diodes, the R_{on} of the latter components is much lower, which is reflected in the FOM of the devices: the best-case for a MOSFET is 301 fs, which is three times higher than the worst FOM for the PIN diodes, 100 fs. Thus, the PIN diode will be the device of choice to implement the RF switch to realize the variable inductor.

To finish the design of the switch, the RF chokes need to be designed. The STM 55 nm BiCMOS technology offers two ways to do so: either using planar inductors or a microstrip stub. The planar inductor solution would render a more compact design, however the close proximity between the inductors and the S-CPS resonator would imply in unwanted magnetic coupling between them, further complicating the design. So, under the argument of simplicity, the RF chokes were designed using microstrip stubs.

3.7.4 VCO CORE DESIGN

The design starts with the design of the RF switches, as their parasitic capacitance, as well as C_{off} and R_{on}, are a part of the resonator. Then, starts the design of the tunable S-CPS transformer, starting with the design of the primary, responsible for the continuous tuning. The primary is designed having a target central F_{OSC} of 90 GHz and a FTR of 15 %. This design uses the optimized design algorithm presented in section 3.4.3, and the goal is to have a trustworthy estimation of $Nsegs_{M8}$, as well as the loading varactors.

This primary configuration is then used as a base to design the secondary using the HFSS EM solver: the $Nsegs_{AP}$ and Y_C are swept to find a combination that gives three distinct resonant bands. Having found this combination, the next step is to design the CCP: given the complexity of this resonator, the CCP W was determined by an exhaustive parametric sweep to find the value, or values in case of multiple CCPs, of W that gives the desired FTR performance.

The goal of this design is to arrive at a multiband VCO that covers the

71 GHz – 86 GHz band continuously. This translates into a 19.1 % FTR with a central F_{OSC} of 78.5 GHz. The results shown in Section 3.5 lead to the conclusion that a single, continuous band covering 15 GHz wouldn't be practical, as the tank would require such a large CCP that it would swamp the resonator's ability to change the resonant frequency. Thus, band-switching could be the answer, provided that the different bands have some overlapping. Three different, overlapping bands, each having a continuous FTR of under 10 % would suffice to guarantee that no gaps are present in the output frequency values.

There are two switches on the tunable S-CPS transformer secondary to realize three different oscillating bands: one switch is located at the far-end of the secondary, which controls the low and middle bands; and the other as close to the primary as possible, which controls the high oscillating band. The switches were optimized to lessen the impact on each point: the switch closer to the primary was designed around diode 2, as it has a smaller R_{on}; the switch at the far end of the secondary uses diode 1, to lessen the impact of C_{off}. The CCP is distributed and tapered across the transformer primary, as it lessens the capacitive loading on the primary, as was shown in section 3.5.6, further widening the continuous FTR. The output buffer is the same as the one presented inn Figure 62. The design of this VCO happens as follows the flowchart contained in Figure 91.

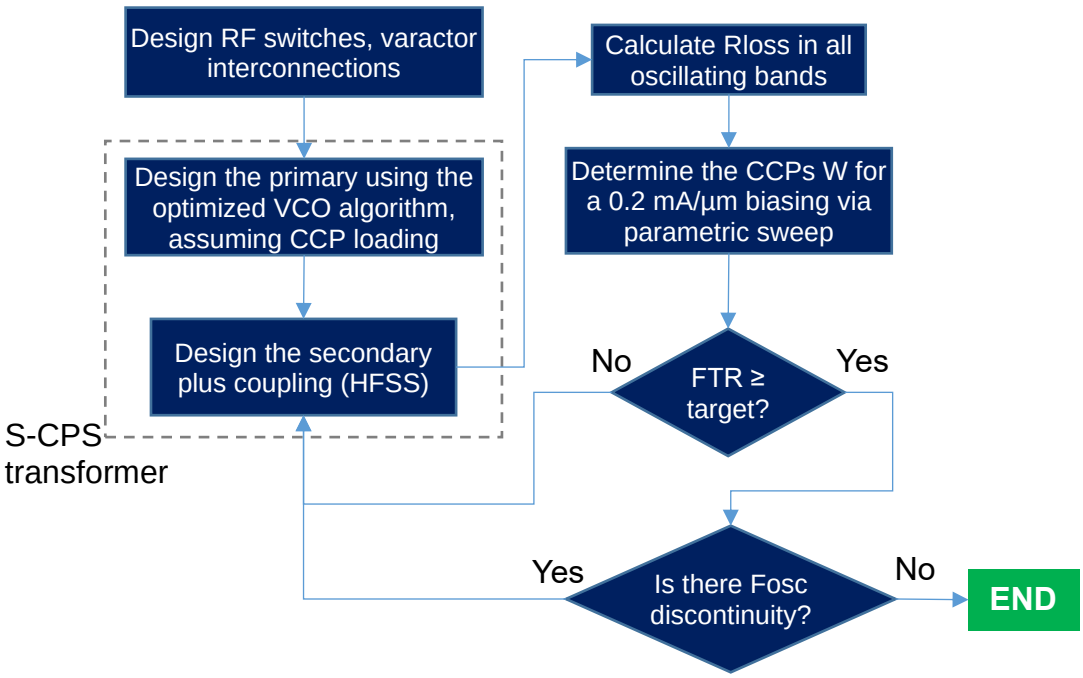


Figure 91 – Design flow of the band-switching, coupled resonator, standing-wave oscillator. Source: author.

3.7.5 VCO RESULTS

First, the design of the switches are presented. The schematic representation for the PIN diode switches is presented in Figure 92 a), showing its complete biasing networks plus the necessary variables. The layout of the diode 2 connections is presented in Figure 92 b).

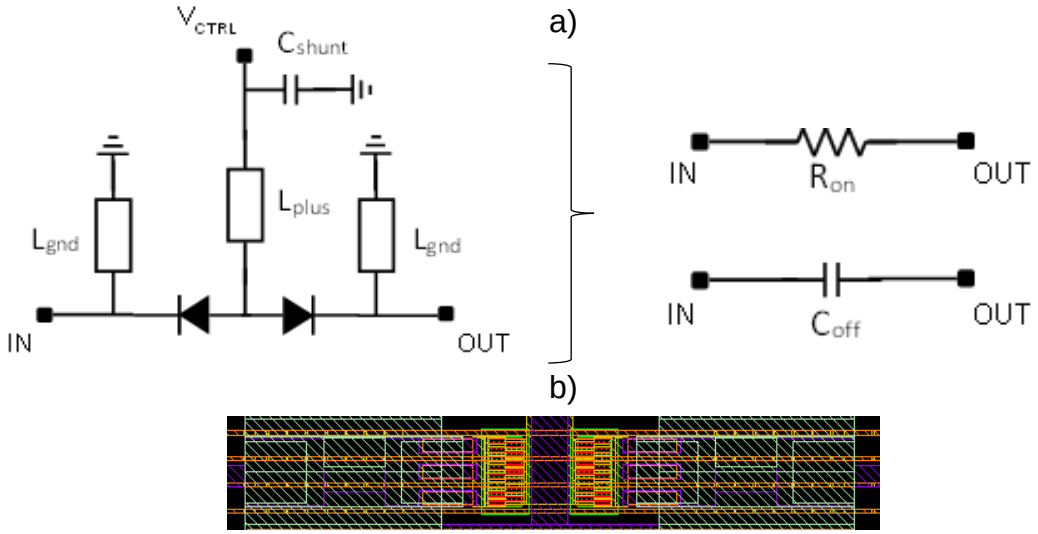


Figure 92 – a) Equivalent PIN diode - based switch schematic and simplified electrical model for the on and off states. b) The layout of the switch employing diode 2. Source: author.

The W of all microstrip lines is fixed at 3 µm to reduce the losses due to skin effect on the conductor. The lengths L_{gnd} and L_{plus} were determined by optimizing the insertion loss and off-state isolation in each switch. The final values for the microstrip stubs and the PLS values of R_{on} and C_{off} are shown in Table 38. The PLS insertion loss and isolation of each switch are shown in Figure 93.

Table 38 – PIN diode switches post-layout performance parameters.

Switch\Parameter	L_{gnd}	L_{plus}	**PLS R_{on} (I_{ak} = 12 mA)**	**PLS C_{off} (V_{ak} = 0V)**
Diode 1	350 µm	550 µm	7.2 Ω	7.6 fF
Diode 2	350 µm	475 µm	5.3 Ω	12.1 fF

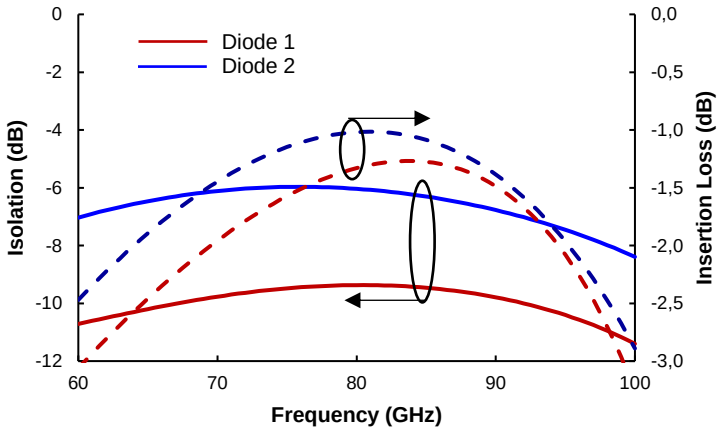


Figure 93 – Post-layout simulation results of the isolation (solid line) and insertion loss (dashed line) of the switch employing diode 1 and diode 2. Source: author.

Having the PLS data of the switches, now the rest of the VCO can be designed. Table 39 contains the final length of the resonators, CCP W and I_{BIAS} consdering a drain current density of 0.25 mA/µm for each MOSFET. Table 40 contains the values for the elements of the proposed Tunable S-CPS transformer model.

After laying out all important interconnections, the VCO core was re-simulated to assess is electrical performance. The PLS were carried out in CADENCE Virtuoso design suite using spectre and ADE L tool and Quantus PEX and PVS tools. The simulations that were carried out are harmonic balance simulations plus noise, intending to extract the output frequency, output power and phase noise of the oscillator. The PLS results for this multiband VCO are presented in Figure 94.

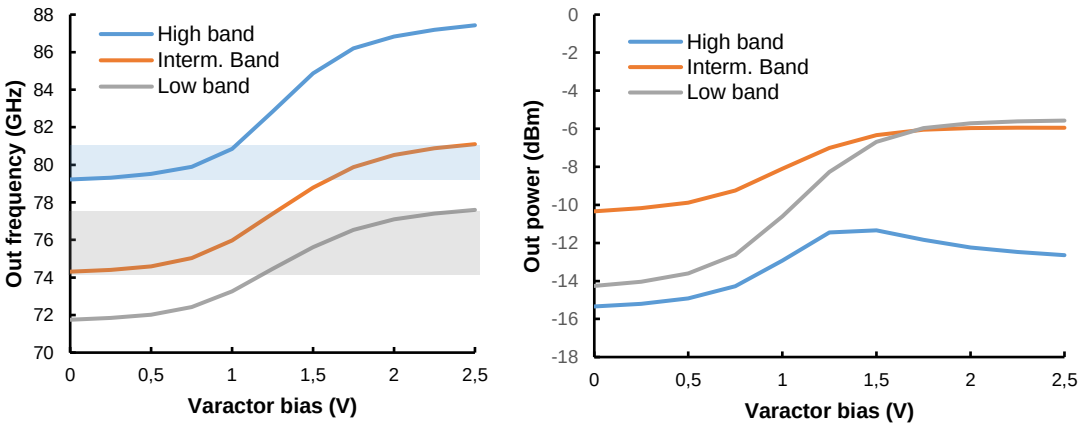
Table 39 – Multiband VCO parameters, including data from the resonator and distributed, tapered CCP.

Parameter	Value
N_{SEGS_M8}	6*7.2 µm = **43.2 µm**
N_{SEGS_AP}	20*7.2 µm = **84 µm**
Y_C	28 µm
W_f	1.5
W_f	0.6
nb_cell	3
CCP W	32 µm + 20 µm
I_{BIAS}	26 mA

Table 40 – Lumped model parameters of the tunable S-CPS transformer-based resonator presented in Figure 86 and Figure 87.

Parameter	Value	Parameter	Switch states (Diode 2 / Diode 1)		
L_{S_M8}	5.82 pH		Off/Off	Off/On	On/On
R_{S_M8}	28.9 mΩ	M_M8AP	1	-1	-1
C_{S_M8}	1.49 fF	MF_M8AP	-0.7	-1	0.2
L_{S_AP}	5.99 pH	MF_APM8	1	-0.4	1
R_{S_AP}	36.11 mΩ	MF_SC	0	1	0.25
C_{S_AP}	0.83 fF				
C_{S_M8AP}	11.52 fF				
L_{SC_M8}	5.7 pH				
L_{SC_AP}	6.1 pH				
L_{conn}	13.5 pH				
C_{C_M8AP}	1 fF				
C_{C_APM8}	20 fF				

The three oscillating bands are clearly distinguishable. The bands overlap to ensure a continuous frequency output. The overlap between bands is: 3.3 GHz between the low and intermediate bands; 1.9 GHz between the intermediate band and the high band. The minimum frequency value is 71.8 GHz and the maximum, 87.4 GHz, translating into a “continuous” FTR of 19.6% and a central F_{OSC} of 79.6 GHz. The phase noise changes between bands, reflecting the different amounts of loss compensation that happens in each band: the worst case happens at the high band, the lighter case at the low band.



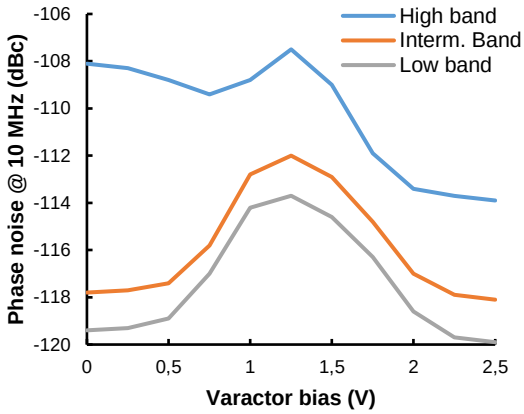


Figure 94 – Post-layout simulation results for the multiband VCO, including the output frequency, plus regions of overlap (top left), output power (top right) and phase noise at a 10 MHz offset from the carrier frequency. Source: author.

Having the VCO core designed and laid out, the next step was to lay out the DC biasing network, the RF output and ground plane. The layout for the die is presented in Figure 95.

The complete VCO layout, including output buffers and I/O pads occupies an area of 0.722 mm², where the VCO core itself occupies about 0.021 mm², a mere fraction of the total area. The die area is dominated by the microstrip stubs for the RF chokes, necessary for the PIN diode biasing, and the buffers.

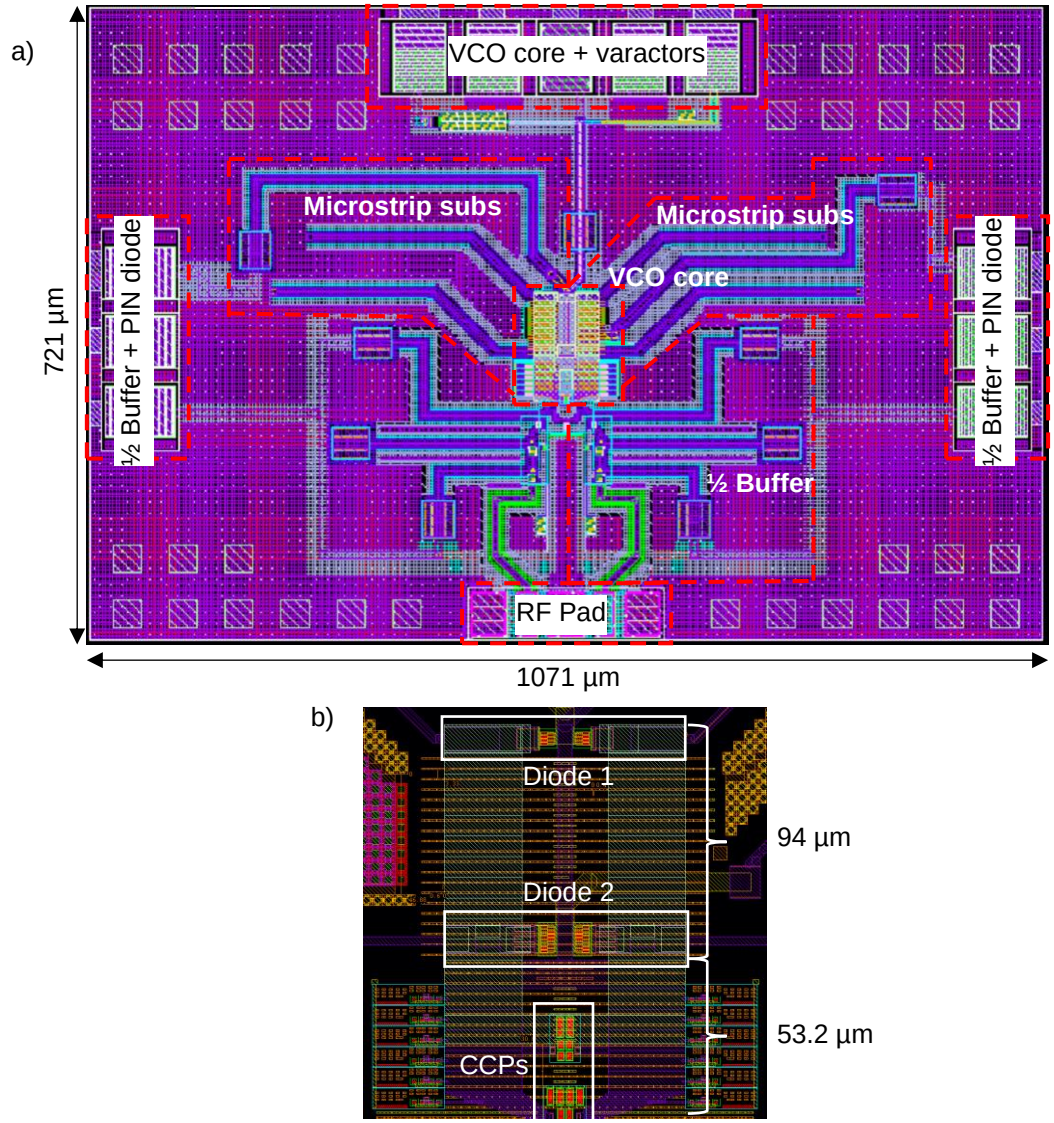


Figure 95 – a) Final layout of the multiband VCO, including the RF chokes for the two RF switches, the output buffers, the DC biasing pads and the RF pads. The die dimensions are also shown. b) The tunable S-CPS transformer-based resonator is shown in detail, with the primary and secondary lengths. Source: author.

3.7.6 DISCUSSIONS

This VCO has the most complex structure designed in this thesis, having a slow-wave, distributed, varactor-loaded primary, which is EM-coupled to a slow-wave secondary that's switched in two different points along its length to create a variable inductor. And, naturally, a design so complex is difficult to optimize properly: rather, this was an exploratory design, in which a proof-of-concept was designed and tested for its potential.

This VCO shows the importance of doing design in a mm-wave-oriented technology, which is having low-loss metallic layers and interconnections allied

with a wide selection of components that are optimized for mm-wave applications. Three elements were instrumental to the success of this design: the first is the large thickness of M8, which enables the creation of a high Qfactor primary; the second is close vertical proximity between M8 and Alucap, which enabled a good coupling between the M8 primary and the Alucap secondary; the third, and perhaps most important, was the availability of PIN diodes to create the RF switches. Without the diodes, the losses introduced by the switch would have rendered this VCO useless as the equivalent losses would be too large to be compensated by a CCP of reasonable size. The PLS results for this VCO are summarized in Table 41.

Table 41 – Performance summary of the multiband VCO presented in this section.

	Multiband VCO (I_{BIAS} = 26 mA)
Central F_{OSC}	79.6 GHz
FTR	15.6 GHz (19.6 %)
PN @ 10 MHz (V_b = 2.5 V), low band	-119.9 dBc/Hz
PN @ 10 MHz (V_b = 2.5 V), mid band	-118 dBc/Hz
PN @ 10 MHz (V_b = 2.5 V), high band	-113.4 dBc/Hz
P_{out}, low band (Best case)	-5.7 dBm
P_{out}, mid band (Best case)	-5.9 dBm
P_{out}, high band (Best case)	-11.3 dBm
FOM (Eq. (2))	-182.97

This VCO has the lowest FOM presented in this chapter, -170.3 dB, and the highest overall DC power consumption, especially considering the 15 mA consumed by the output buffers and the 24 mA consumed by the two PIN diode switches when turned on. It shows again that there is an inherent trade-off between having a continuously-tunable, wide-band VCO and DC power consumption: the tuning mechanisms either introduce extra losses to the resonator or they reduce the Q-factor of the resonator, increasing the amount of DC power required for the loss compensation circuit.

3.8 CONCLUSIONS

In this chapter, the concept of a distributed VCO resonator, based on a quarter-wavelength-long, periodically-loaded S-CPS, was presented. The novel concept was formulated and incrementally optimized. First the S-CPS layout was

optimized, by finding a combination of BEOL layers that yielded the highest Q-factor for the S-CPS while maximizing the varactor control over the phase velocity of the transmission line. Second, the design algorithm for the VCO was optimized to show that, given a technology, it is possible to design the best-performing VCO given a target central F_{osc} and an FTR. This was possible because there is a best-performing varactor-loaded S-CPS for each design.

After running the optimization, the concept was further explored and pushed to its limits. A study on concentrated versus distributed loss compensation was conducted, which showed the advantages and disadvantages of a number of different CCP configurations. The study showed that the best-performing CCP configuration employed a tapered, distributed layout: the CCPs closer to the open-circuit termination are larger than those closer to the short-circuit termination, but smaller than a single CCP at the open-circuit termination. This alleviates the capacitive loading on the S-CPS resonator, increasing the FTR at the cost of increased DC consumption. The position of the CCP was also investigated, and moving the CCP to a central point of the resonator showed similar results. By combining both effects, it is possible to arrive at a better-performing configuration, when the available space and design rules allow.

Then, the bufferless VCO concept was presented. It is an innovative concept that takes advantage of the distributed nature of the S-CPS resonator to derive power directly from the resonator, no buffering required. The main advantages of this approach are reduced surface requirements and higher overall DC-to-RF efficiency, at the cost of poorer phase-noise and FTR performance for the same resonator.

Finally, the S-CPS resonator was used to implement a multi-band VCO that used a band-switching mechanism based on an S-CPS-based transformer with a variable inductance secondary. This variable inductance was implemented with a closed secondary loop switched by PIN diode switches. The switches and Tunable S-CPS transformer were modelled, designed and the final VCO was shown to have a continuous FTR of more than 19%.

To compare the performance of the VCOs, their results will be placed against those of the state-of-the-art presented in Table 2. This comparison is presented in Table 42.

Table 42 – Comparison of the VCOs designed in this thesis against the state-of-the art. The

results in bold are those designed in this thesis.

Ref.	Tech.	F_{OSC} (GHz)	*Cont. FTR* (%)	P_{DC}[#] (mW)	*PN*@ 10 MHz (dBc/Hz)	FOM@ 10 MHz (dBc/Hz)	P_{out}[##] (dBm)
[25]	65-nm CMOS	76.5	6.27	14.3	-109	175.1	-1.5
[31]	65-nm CMOS	73.8	N/A	8.4	-112.2	-180	-17
[32]	65-nm CMOS	81.5	14	33	-97.3*	-179.7*	N/A
[33]	90-nm CMOS	56.7	16	8.7	−118.7	−184.3	-3.6
[34]	130-nm CMOS	91	0.5	46	-86.2*	-169.6*	+4.5
[35]	65-nm CMOS	70.2	N/A	7.7	-112	-180.4	N/A
[36]-1	65-nm CMOS	75.9	N/A	12	-109.4	-176.2	N/A
[36]-2	65-nm CMOS	89.4	N/A	11	-108.3	-176.9	N/A
[37]	65-nm CMOS	64	7	5	-113.7	-182.8	-17
[38]	40-nm CMOS	86.2	5.8	28.4	-118.8	-183.2	N/A
[39]	65-nm CMOS	105	9.5	54	-92.8*	-175.5*	+4.5
[40]	65-nm CMOS	62.8	N/A	21.5	-114.95	-177.6	-10
[41]	65-nm CMOS	59	5.4	16.5	-112	-175.5	-0.9
[42]	55-nm CMOS	77.3	3.25	15.1	-115.1	-181	-1.12
[53]	55-nm CMOS	77.1	4.79	5.69	−115	−185	-4.5
3.3 Design 1	**55-nm CMOS**	**81.3**	**9.7**	**6**	**-115**	**-186**	**-10.1**
3.3 Design 2	**55-nm CMOS**	**81.3**	**10.3**	**6**	**-115**	**-186**	**-10.18**
3.4	**55-nm CMOS**	**80.3**	**10**	**7.6**	**-114**	**-184.6**	**-7.6**
3.5 Reference case	**55-nm CMOS**	**78.9**	**14.7**	**14.4**	**-116**	**-182**	**-5.7**
3.5 Shifted CCP	**55-nm CMOS**	**80**	**16.3**	**22.8**	**-116**	**-178**	**-7.7**
3.5 Distributed CCP	**55-nm CMOS**	**78.3**	**15.8**	**18**	**-114.8**	**-181**	**-6.7**
3.5 Distr. Shifted CCP	**55-nm CMOS**	**79.4**	**16.7**	**22.8**	**-115.5**	**-180**	**-7.4**
3.6 Design 1	**55-nm CMOS**	**80**	**9.6**	**7.56**	**-111**	**-182.5**	**-5.3**
3.6 Design 2	**55-nm CMOS**	**78.4**	**15.1**	**21.6**	**-113.8**	**-177.4**	**-0.8**
3.6 Design 3	**55-nm CMOS**	**78.4**	**14.3**	**19.2**	**-116**	**-181**	**-1.9**
3.7	**55-nm CMOS**	**79.6**	**19.6**	**31.2**	**-113.7**	**-182.97**	**-5.7**

This comparison shows that the designed VCOs have a large FTR (above 10 %) while maintaining a high FOM (below -170 dB). This indicates that the varactor-loaded S-CPS resonator do represent a performance improvement over the lumped inductor-capacitor tank and also on other forms of resonance control. In conclusion, the S-CPS resonator is a very flexible and powerful resonator topology that permits the design of very high-performance, compact and innovative VCOs at mmW.

4 CONCLUSION

This thesis briefly explained the context of mmW wireless communication, presenting the basic architecture of a beam-steering front-end, followed by the analysis and design of two important building blocks of a beam-steering front-end: the phase shifter and the VCO.

The phase shifter presented in this work uses many innovative concepts. It is based around a novel suspended microstrip line built around the slow-wave microstrip lines available on the MnM technology platform. It uses liquid crystal to achieve continuous tuning and to facilitate electrostatic switching, which is known to generate huge amounts of phase variation with a high figure of merit. Also, the phase shift created by electrostatic switching with liquid crystal was shown to improve the performance of the phase shifter, which performed better than either case alone: the combined effects registered a best-case figure of merit of 108 °/dB at 60 GHz. However, the anchoring structure of the phase shifter creates Bragg resonance that must be optimized for a target operating frequency. Nevertheless, the LC-MnM phase shifter shows a lot of potential.

The VCOs presented at this work, designed on a RF-oriented BiCMOS technology, implemented a distributed resonator built around a S-CPS, which is periodically loaded with varactors. This was shown not only to improve the Q-factor of the resonator but also to enable a higher degree of control of the varactors over the phase velocity of the transmission line, thus on the output frequency. This concept was incrementally optimized: first, an optimal geometry was found; then, a global optimization algorithm was proposed that would result in the best-performing VCO given the technological parameters, a target central oscillating frequency and a target tuning range. Then, the concept of distributed loss compensation was analyzed, which showed that distributing the negative resistance across the resonator improved the tuning range of the VCO by reducing the capacitive loading on the open-circuit termination of the resonator, at the cost of increased DC consumption. The concept of designing a bufferless VCO was also shown, which includes a more detailed model that includes the loading effect of an external load on the tank and an improved equivalent loss calculation. The bufferless concept improved the global DC to RF efficiency at the cost of reduced tuning range when compared to a buffered VCO. Finally, a

multi-band VCO was designed using a variable inductor realized with a tunable S-CPS transformer whose secondary coil has two PIN diode-based switches for improved performance. The resulting VCO showed a continuous tuning range from 71.8 GHz up to 87.4 GHz, or 19.6 % with a figure-of-merit of -170 dBc/Hz. This work showed the great potential and flexibility that the S-CPS has to implement compact and high-performance VCOs at mmW.

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