ARTHUR LOMBARDI CAMPOS

Design of a low-power 10-bit 12-MS/s asynchronous SAR ADC

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Dissertation presented to the University of São Paulo at São Carlos School of Engineering in partial fulfillment of the requirements for obtaining the degree of Master of Science in Electrical Engineering.

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Projeto de um SAR ADC assíncrono de 10 bits a 12MS/s para baixo consumo

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To my parents and brothers, with love and gratitude.

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Abstract

CAMPOS, A. L. Design of a low-power 10-bit 12-MS/s asynchronous SAR ADC. 2020. 134p. Dissertation (masters) – São Carlos School of Engineering, University of São Paulo, São Carlos, 2020

This work presents the design of a low-power 10-bit 12-MS/s Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) in 65-nm technology, suitable for IEEE 802.15.4g standard frontend receivers (low data rate and power consumption smart utility networks). By using the differential implementation with a pair of bootstrapped switches, the input signal is sampled with low distortion. The asynchronous implementation of the SAR circuit leads to an increased system flexibility because only a single clock source is required. To support the merged capacitor switching scheme (MCS), a three-level switch circuit was designed for the capacitor array. The simulated circuit achieved a 9.65 ENOB with 151.4 µW of power consumption at 12 MS/s, leading to a FOM of 15.8 fJ/Conversion-step. Simulations have also shown that the ADC is efficient for sampling frequencies ranging from 10 kS/s up to 12 MS/s, extending its usability to low sampling frequency circuits.

Keywords: Integrated Circuits. Analog-to-Digital Converter. Low power consumption. Receivers. Asynchronous SAR ADC, Internet of Things.

Resumo

CAMPOS, A. L. Projeto de um SAR ADC assíncrono de 10 bits a 12MS/s para baixo consumo. 2020. 134p. Dissertação (mestrado) – Escola de Engenharia de São Carlos, Universidade de São Paulo, São Carlos, 2020

Este trabalho apresenta o projeto de um Conversor Analógico-Digital (ADC) de 10 bits a 12 MS/s, de baixo consumo, do tipo Registrador de Aproximações Sucessivas (SAR) assíncrono. O circuito foi projetado em tecnologia de 65 nm e visa atender receptores desenvolvidos para o padrão IEEE 802.15.4g (redes inteligentes de baixo consumo e baixa taxa de transmissão de dados). Para reduzir a distorção durante amostragem de sinais, foi utilizado uma implementação diferencial com um par de chaves *bootstrap*. A implementação assíncrona do circuito SAR aumenta a flexibilidade do sistema porque apenas um sinal de relógio é necessário para seu funcionamento. Para suportar o esquema de chaveamento mesclado (MCS), uma chave de três níveis foi desenvolvida para a matriz de capacitores. Em simulações, o circuito atingiu um ENOB de 9.65 e um consumo de 151.4 µW, a 12 MS/s, resultando em uma figura de mérito de 15.8 fJ/Conversion-step. Simulações também indicaram que o ADC é eficiente em frequências de amostragem variando de 10 kS/s a 12 MS/s, estendendo sua usabilidade para circuitos de baixa taxa de amostragem.

Palavras-chave: Circuitos Integrados. Conversor Analógico-Digital. Baixo consumo de energia. Receptores. SAR ADC assíncrono, Internet das coisas.

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List of abbreviations and acronyms

ADC	Analog-to-Digital Converter
BER	Bit Error Rate
CER	Conversion Error Rate
CMOS	Complementary Metal-Oxide-Semiconductor
DAC	Digital-to-Analog Converter
DC	Direct Current
DFT	Discrete Fourier Transform
DNL	Differential Nonlinearity
DTFT	Discrete-Time Fourier Transform
ENOB	Effective Number of Bits
ESR	Equivalent Series Resistance
FOM	Figure of Merit
FS	Full Scale
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate Frequency
INL	Integral Nonlinearity
IoT	Internet of Things
LSB	Least Significant Bit
LTI	Linear Time-Invariant
MCS	Merged Capacitor Switching
MIM	Metal-Insulator-Metal

MOS	Metal-Oxide-Silicon
MSB	Most Significant Bit
NMOS	N-type Metal-Oxide-Silicon Field-Effect Transistor
PHY	Physical Layer
PMOS	P-type Metal-Oxide-Silicon Field-Effect Transistor
PSD	Power Spectral Density
PVT	Process-Voltage-Temperature
RF	Radio Frequency
RMS	Root-Mean-Square
SAR	Successive Approximation Register
SFDR	Spurious-Free Dynamic Range
SINAD	Signal-to-Noise-and-Distortion
SNR	Signal-to-Noise Ratio
SR	Slew-Rate
THD	Total Harmonic Distortion
TSMC	Taiwan Semiconductor Manufacturing Company Limited

List of symbols

b_o	bit o at the output of the ADC
dBc	Decibels relative to the carrier
$dBFS$	Decibels relative to full scale
f_{in}	Fundamental frequency of the input signal
f_{sample}	Sampling frequency of the ADC
g_m	Transconductance of a MOS transistor
i	Iteration number
k	Boltzman constant
t_{fix}	Fixed time delay
t_{margin}	Time margin
t_p	Propagation time
t_{pL}	Latch propagation time
t_{reg}	Regeneration time of the comparator
$t_{reg,hard}$	Regeneration time of the comparator for the hardest decision
t_{track}	Time interval in which the ADC is sampling the input signal
v_N	Voltage at the negative input of the comparator
v_P	Voltage at the positive input of the comparator
ζ	Damping ratio
μ_n	N-type charge-carrier effective mobility
$\sigma(\Delta C/C)$	Standard deviation of the difference of two identical capacitors, normalized to their absolute value, C
σ_u	Standard deviation of the mean capacitance value of C_U

$\sigma_{DNL,MAX}$	Worst-case standard deviation of DNL
τ_c	Time constant of the pole
τ_L	Latch time constant
ω_c	Pole position
A_C	Capacitor area
$A_V(0)$	DC gain
$A_V(s)$	Transfer function in the s-plane
C_{bridge}	Bridge capacitor
C_f	Voltage scaling capacitor
C_{hld}	The hold capacitor
C_{ox}	Gate-oxide capacitance of a MOS transistor
C_p	Parasitic capacitance
C_u	Capacitance value of C_U
C_{GD}	Gate-drain capacitance of a MOS transistor
C_{GS}	Gate-source capacitance of a MOS transistor
C_{OV}	Gate-drain/source overlap capacitance of a MOS transistor
C_U	The unity capacitor
Cn	Capacitor at the n-side of the DAC
Cp	Capacitor at the p-side of the DAC
$E_{gain(ADC)}$	Gain error of the ADC
$E_{off(ADC)}$	Offset error of the ADC
$E(D)_{DNL}$	DNL error of the ADC, at the output code D
$E(D)_{INL}$	INL error of the ADC, at the output code D
$H(f)$	Transfer function
J	Number of binary-weighted capacitors in the sub DAC
K_C	Capacitor density
K_σ	Capacitor matching coefficient

L	Channel length of a MOS transistor
L_{OV}	Gate-drain/source overlap length of a MOS transistor
M	Number of binary-weighted capacitors in the main DAC
N	ADC resolution
N_{record}	Number of samples stored for DFT computation
N_{window}	Number of cycles within the sampling window for DFT computation
P_{meta}	Probability of a metastability event to occur
$P_{noise,out}$	Total noise power in the output
Q_{ch}	Channel charge of a MOS transistor
Q_{TOP}	Total charge on the top plate of the capacitors
R_{ON}	On-resistance of a MOS transistor
$S_{in}(f)$	Power spectral density of the input signal
$S_{out}(f)$	Power spectral density of the output signal
$S_v(f)$	Power spectral density
Sn	Switch at the n-side of the DAC
Sp	Switch at the p-side of the DAC
T	Temperature, in Kelvin
T_{easy}	Sum of all regeneration times during a conversion, excluding the hardest one
$T_{FIX,TOT}$	Sum of all fixed delays for the DAC settling
T_S	Sampling period
V_{eff}	Effective gate-source voltage
V_h	Harmonic distortion of the ADC
V_{in}	Input voltage
V_n^2	Noise power density (voltage squared)
V_{out}	Output voltage
V_{DAC}	DAC output voltage

V_{DD}	Power supply voltage
V_{DDA}	Analog power supply voltage
V_{DDD}	Digital power supply voltage
V_{FS}	Full-scale voltage
V_{GS}	Gate-Source voltage of a MOS transistor
V_{IH}	Input high logic level
V_{IL}	Input low logic level
V_{LSB}	1 LSB equivalent voltage
V_{OH}	Output high logic level
V_{OL}	Output low logic level
V_{OS}	Offset voltage
V_{Q}	Quantization error of the ADC
V_{REF}	ADC reference voltage
V_{SS}	Ground
V_{SSA}	Analog Ground
V_{SSD}	Digital Ground
V_{TH}	Threshold voltage of a MOS transistor
V_{TOP}	Voltage on the top plate of the capacitors
W	Channel width of a MOS transistor
Δf	Frequency band
ΔV_{in}	Differential input voltage
ΔV_{o}	Differential output voltage

Summary

1. Introduction

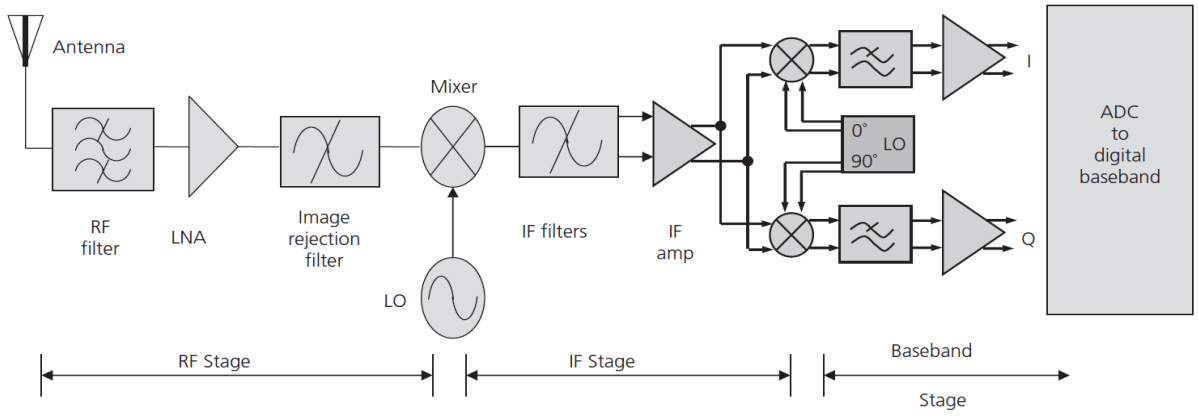
The adoption of internet of things (IoT) solutions for a wide range of applications, such as transportation, manufacturing, and consumer electronics, has increased over the past few years due to its potential of reducing costs and improving processes (COLUMBUS, 2018). Although the demand for software development is predominant in the IoT field, the hardware must also evolve, otherwise it could be a bottleneck for the electronic systems. For example, in low-power applications, efficient algorithms and protocols may not achieve their purpose if the hardware was not optimized for low power consumption.

When it comes to wireless smart utility networks, like smart grid, some hardware developers are adopting the Radio Frequency (RF) transceivers described by IEEE 802.15.4g, which is an amendment of the IEEE 802.15.4 standard (low data rate and long battery life). As reference, a typical block diagram of RF receivers is shown in Figure 1.1. In this scheme, the received RF signal is filtered, amplified, and mixed down to an Intermediate Frequency (IF). At the IF stage, the signal is one more time filtered and amplified before being mixed down again to the baseband stage. In the next stage, the signal (presenting a bandwidth of just a few MHz) must be digitized by an analog-to-digital converter (ADC) before demodulation at the digital circuitry.

For low power applications, the blocks that compose such complex system must present a low power consumption. Although the digital circuitry of such electronic systems benefit from the size reduction of transistors, reducing area and power consumption, their analog and mixed-signal counterparts do not necessarily benefit from new technological nodes (VAN DE PLASSCHE, 2003), being it an opportunity for researchers to

innovate and propose new design techniques for low-power ADCs.

Figure 1.1 – Block diagram of typical RF communication receiver.



Source: (BOWICK, BLYLER and AJLUNI, 2008).

1.1. Objectives

This work aims to design an ADC using state-of-art techniques to reduce power consumption and silicon area. The ADC will be employed in the receiver circuit of an Integrated Circuit (IC) that implements the Physical Layer (PHY) for an IEEE 802.15.4g standard modem, in development by the Eldorado Research Institute, in collaboration with The University of São Paulo and The University of Campinas.

The converter must present a flexible sampling frequency, from few kS/s up to 12 MS/s. This feature allows the circuit designed in this work to be reused in a wide spectrum of low-power systems and subsystems, such as neural signal recorders and modems for different IEEE 802.15.4 standards, such as Zigbee and Thread.

For increased reliability and yield, the circuit must be designed considering fabrication process variations. Also, it should be able to support power supply variation of $\pm$ 10 % and temperature variation, ranging from 0 ºC up to 85 ºC.

1.2. Organization

This dissertation is organized as follows. After the introduction, chapter 2 presents an overview of the characteristics of a typical ADC, a quick review of the binary-search algorithm and an overview of the designed ADC. Chapter 3 revises the theoretical framework for better understanding of this work. Chapter 4 shows in details the design and layout of the ADC, along the proposed implementation of DAC switches and the top plate shielding in the layout view. The results and conclusions are shown in chapters 5 and 6.

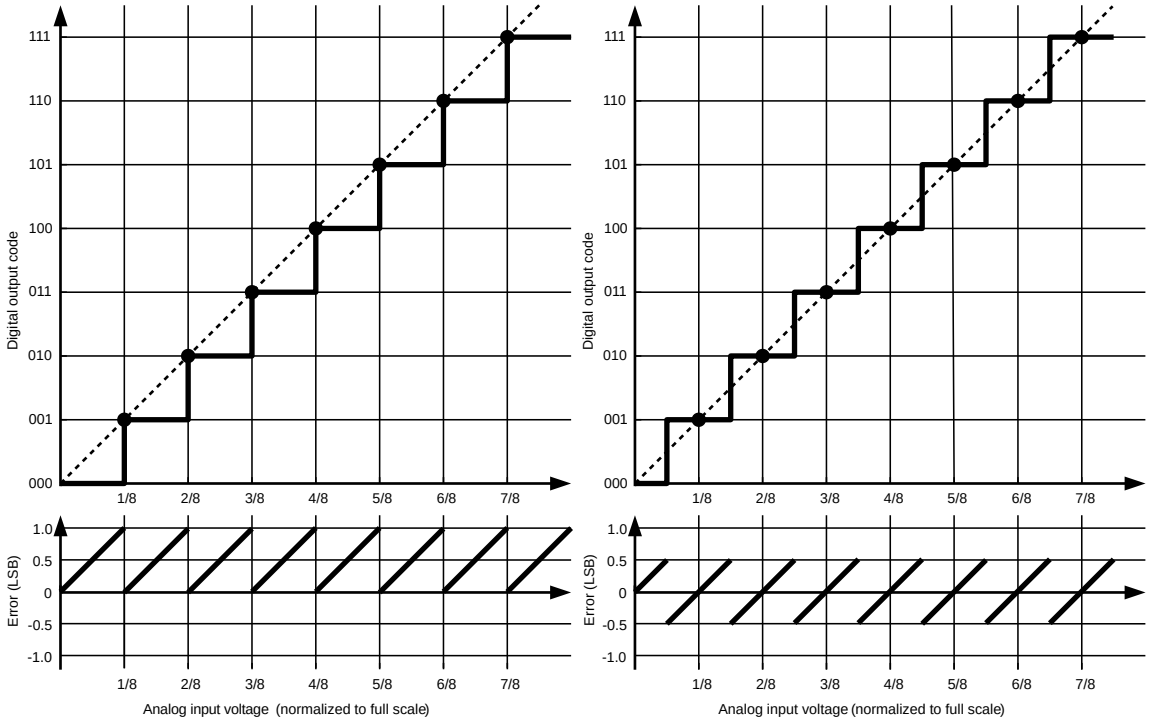
2. The ADC architecture

In this chapter, an overview of the characteristics of a typical ADC and a quick review of the binary-search algorithm are presented.

2.1. Input-output characteristics

The transfer curve (or characteristic curve) of an ADC is a plot that presents the expected digital output code of the ADC according to its analog input signal. Take a 3-bit ADC as an example. The transfer curve is created by plotting the ADC output code for each input voltage, ranging from zero up to V_{REF} (the maximum input voltage) as shown in Figure 2.1(a).

Figure 2.1 – ADC transfer curve considering no offset (a) and -1/2 LSB offset (b).



(a) (b)

Source: Author, adapted from (STALLER, 2005).

Note that for an ideal N-bit ADC this line has the shape of a “staircase”, presenting 2^N “levels” of 1 Least Significant Bit (LSB) width, where the LSB width is $V_{LSB} = V_{REF}/2^N$. Considering that an hypothetical ideal infinite resolution ADC presents a transfer function given by a straight line (the dashed line in Figure 2.1(a)), we can state that a real N resolution ADC presents a conversion error, for a determined input voltage, given by the difference between the real ADC transfer curve and the infinite resolution ADC transfer curve at the input voltage. The conversion error is also known as quantization error. From Figure 2.1(a), the maximum quantization varies from 0 (dots) to +1 LSB.

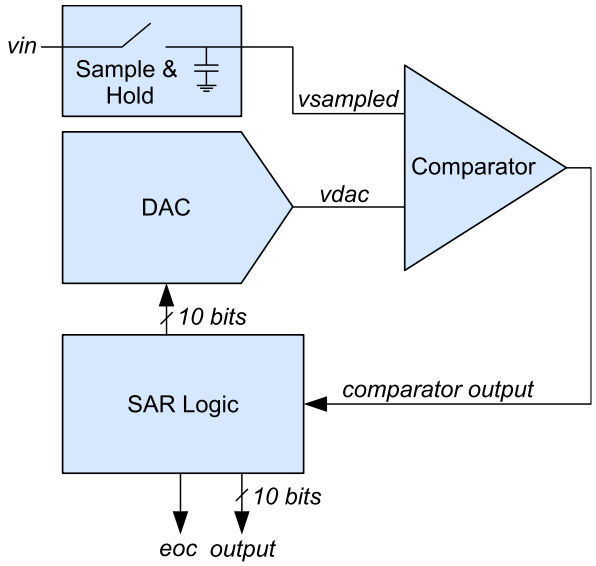
An alternative view of the input-output characteristic is created by shifting the transfer function to the left by 1/2 LSB, as shown in Figure 2.1(b). This new graph presents a quantization error ranging from –1/2 LSB to +1/2 LSB, which is a particularly useful approach for the quantization error analysis.

2.2. The SAR ADC operation

The Successive Approximation Register (SAR) ADC topology makes use of a binary search algorithm to perform the analog-to-digital conversion. This topology presents a fast operation, while keeping a moderate circuit complexity (JOHNS and MARTIN, 1997), and is well suited for moderate resolutions and low-to-medium data rate applications (FREDENBURG and FLYNN, 2015). It is composed by a sample and hold circuit, a Digital-to-Analog Converter (DAC), a comparator, and a digital circuitry to execute a binary search procedure and to store the conversion result. Figure 2.2 illustrates a typical implementation of the SAR ADC.

During the binary search procedure, successive digital words for the internal DAC are produced, and its output voltage, V_{DAC}, will increasingly approach the sampled V_{in}. At the end of the search procedure, a final digital word is found, which is composed by a vector of bits ranging from b_0 up to b_{N-1}, where N is the resolution of the ADC.

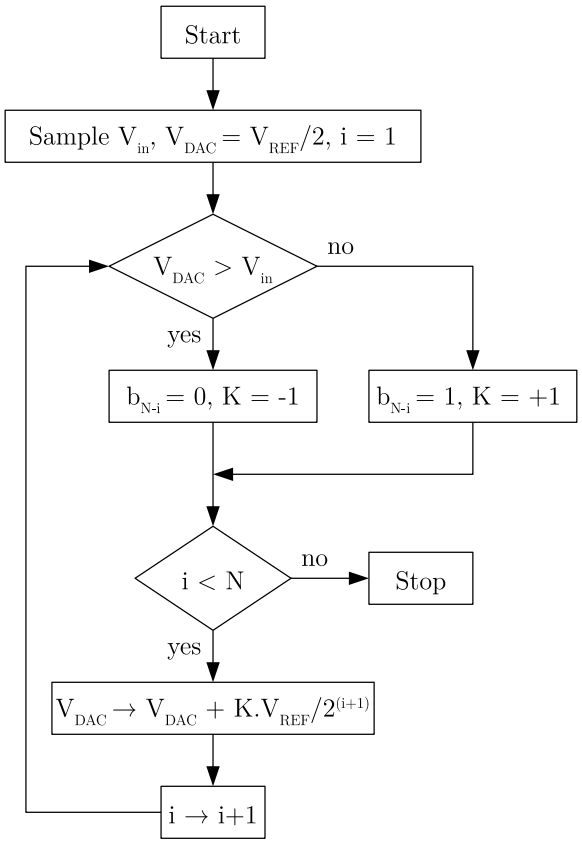
Figure 2.2 – A typical SAR ADC implementation.



Source: Author.

The flowchart of Figure 2.3 describes the binary search algorithm of a SAR ADC.

Figure 2.3 – Flowchart of a typical binary search used in SAR ADCs.



Source: Author, adapted from (JOHNS and MARTIN, 1997).

First, the converter samples V_{in}, sets i (the iteration number) to 1 and sets,

through application of the appropriated digital word, the V_{DAC} to $V_{REF}/2$. Next, N iterations are executed. For each iteration, the V_{DAC} is compared to V_{in}. If the V_{DAC} is smaller than V_{in}, b_{N-i} is set to 1 and V_{DAC} will increase by $V_{REF}/2^{i+1}$ before the next iteration, otherwise b_{N-i} is set to 0 and V_{DAC} will decrease by $V_{REF}/2^{i+1}$ before the next iteration. Finally, i is increased by 1. This compare and set procedure is repeated until all bits are resolved.

For an ideal ADC, V_{DAC} will differ from V_{in} by no more than $V_{REF}/2^{N+1}$ after the N^{th} iteration, meaning the current values in the vector of bits at the DAC are the converted output code.

2.3. Asynchronous SAR ADCs

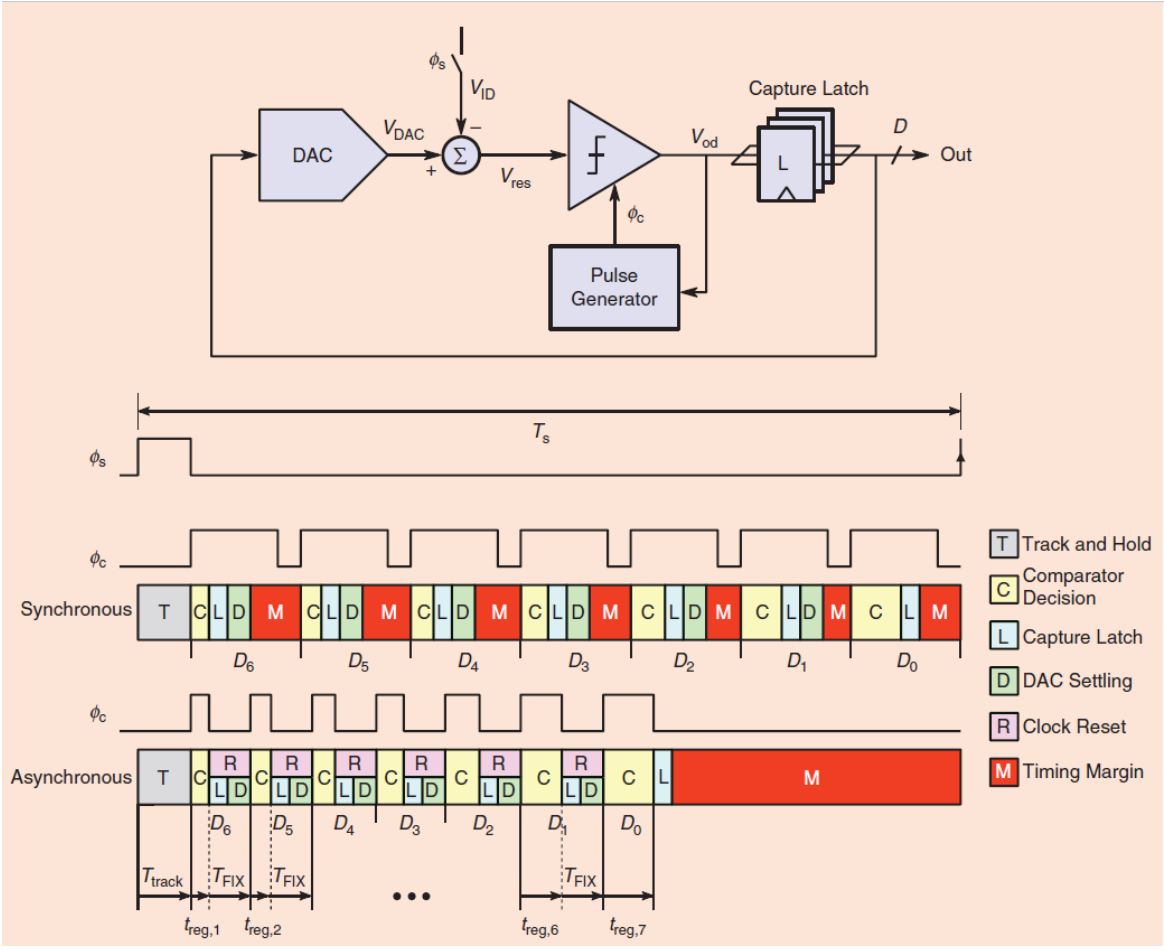
Typical SAR ADCs make use of two clock sources: one to control the sampling (the sampling clock) and other to control the iterations of the binary search algorithm (the SAR clock). Since each iteration in the SAR procedure is synchronized to the SAR clock, this converter is classified as synchronous. On the other hand, there are SAR ADCs, like the ones presented in (CHEN and BRODERSEN, 2006) and (HARPE, ZHOU, *et al.*, 2010), that need only one clock signal, which is responsible for controlling the data sampling. In this case, the iterations of the search algorithm are controlled by a set of combinational digital circuits, delay cells and registers. Since these circuits are not synchronized by any clock source, these types of SAR ADCs are categorized as asynchronous.

The requirement of only one clock source in asynchronous implementations is advantageous since it relaxes the specifications of any frontend circuits responsible for providing clock signals to ADCs working in different sampling rates, attending specifications of diverse smart utility networks.

Another notable advantage of the asynchronous implementation, compared to the synchronous one, is the increased robustness to metastability problems. As analyzed in

(YU, BANKMAN, *et al.*, 2019), and shown in Figure 2.4, the synchronous implementation allocates an individual time budget for each iteration to finish the comparison and set the DAC with the new code value. The remaining time margin (M, highlighted in red) is available to be used by the comparator during a hard decision comparison, i.e., when a small voltage is applied to its input, significantly increasing the comparison time (C, highlighted in yellow). Since there will be only one hard decision among the N iterations of the binary search procedure, the time margin available for the remaining $N-1$ iterations are unused and these time margins are wasted.

Figure 2.4 – Time chart of synchronous and asynchronous SAR ADCs.

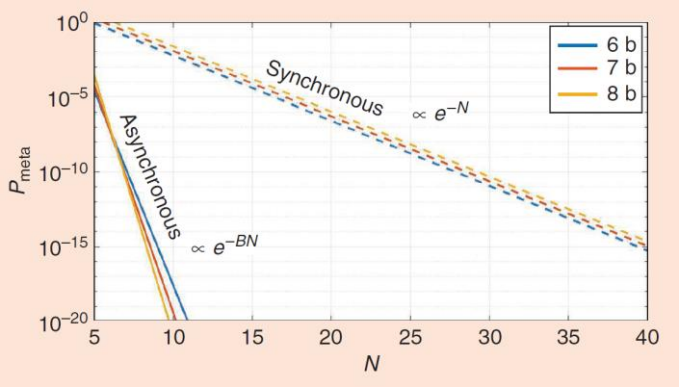


Source: (YU, BANKMAN, *et al.*, 2019).

On the other hand, in the asynchronous implementation, each iteration is triggered as soon as the previous one is finished, giving no timing margin between them, resulting in a single timing margin at the end of the last iteration. This continuous timing

margin can be interpreted as a much bigger headroom available for the comparator, during the hard decision, to quit the metastable state, whichever iteration it is in. This time margin is further increased, as shown in Figure 2.5, when the resolution of the ADC is also increased, because there are more time margins to be "borrowed" from unused bit decisions. As a result, medium/high resolution asynchronous SAR ADCs are expected to present an extremely smaller probability of entering in a metastable event than its synchronous counterpart.

Figure 2.5 – A graph of the probability of a metastable event, for different ADC resolutions.



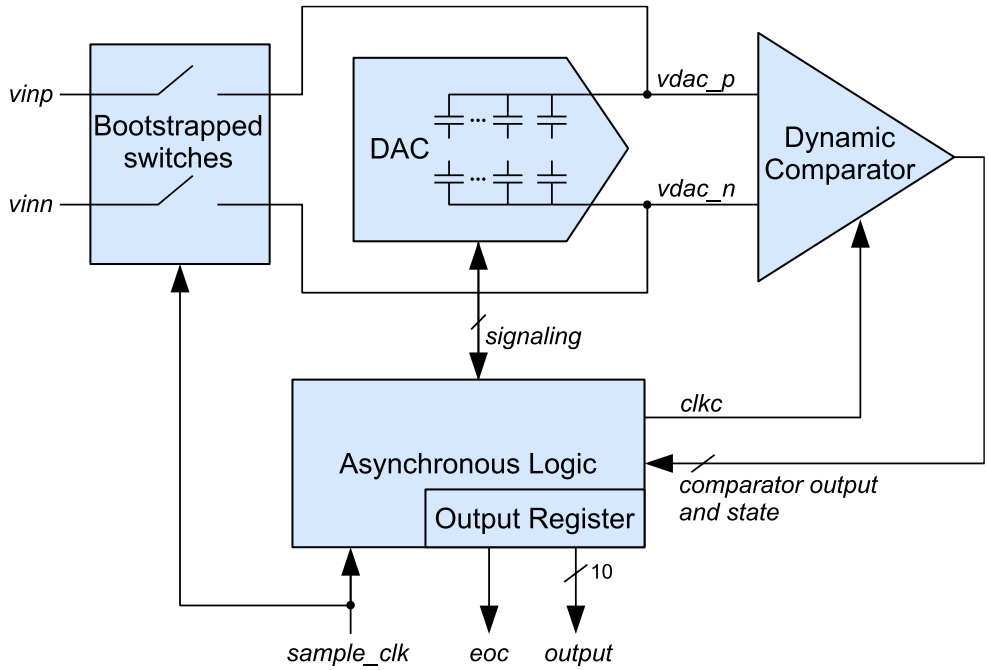
Source: (YU, BANKMAN, *et al.*, 2019).

2.4. An overview of the designed ADC

In this work an asynchronous SAR ADC was implemented. As mentioned in the previous sub-section, this kind of converter requires only one clock source, relaxing the clock distribution requirements. A block diagram of the designed circuit is shown in Figure 2.6 and present a differential architecture. Differential circuits can greatly minimize the effects of common-mode noise and even order harmonics distortion (VAN DE PLASSCHE, 2003). In the block diagram of Figure 2.2, *vsampled* and *vdac* are periodically compared. It is intuitive that, since they are generated by different circuits and present different metal traces, both nodes pick up noise differently, affecting the comparison result, especially when *vsampled* and *vdac* present similar voltage values during a hard decision. Conversely, in Figure 2.6, both signals at the input of the comparator are

provided by identical sub circuits with symmetrical routing, meaning they will ideally pick up noise evenly and the subtraction procedure of the comparator will intrinsically cancel it out (or at least minimize it).

Figure 2.6 – The ADC block diagram.



Source: Author.

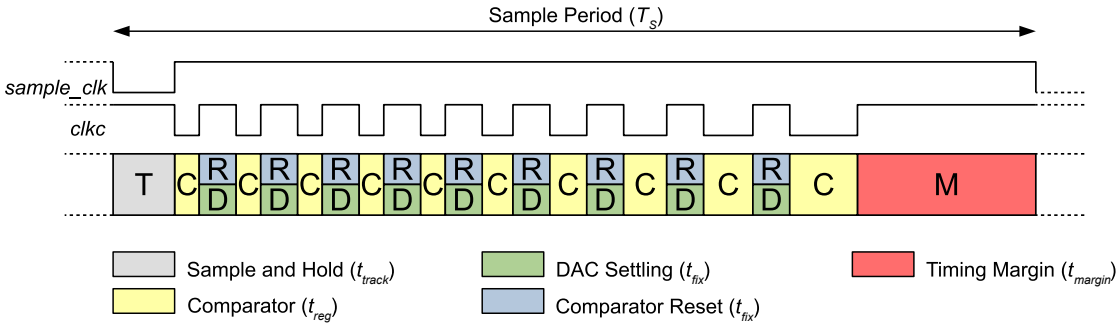
The ADC implemented in this work is composed by: 1) a pair of input switches, implemented using the bootstrapped technique to improve linearity; 2) a pair of capacitor arrays (capacitive DAC); 3) a dynamic comparator; 4) an asynchronous logic; and 5) output registers. A sampling clock (*sample_clk*) controls the bootstrapped switches and the asynchronous logic circuit that sets the ADC to either sampling or conversion phase. When the sampling clock is set to low (sampling phase), the bootstrapped switches turn on and the capacitor array of the DAC is charged according to the differential input signal. In this phase, the power consumption of the ADC is quite low because there is no digital circuit activity and the analog circuits present low current consumption.

When the sampling clock is set to high (conversion phase), the bootstrapped switches are turned off and the SAR procedure is triggered, starting the binary search

procedure, which takes N iterations, where N is the resolution of the ADC. In the first iteration, *vdac_p* and *vdac_n* signals remain constant. From the second iteration on, the *vdac_p* and *vdac_n* signals themselves have their values modified by $(N-1)$ additions/subtractions of $V_{FS}/2^i$, where V_{FS} is the single full-scale voltage (V_{DD}) and i is the iteration number, ranging from 2 up to N.

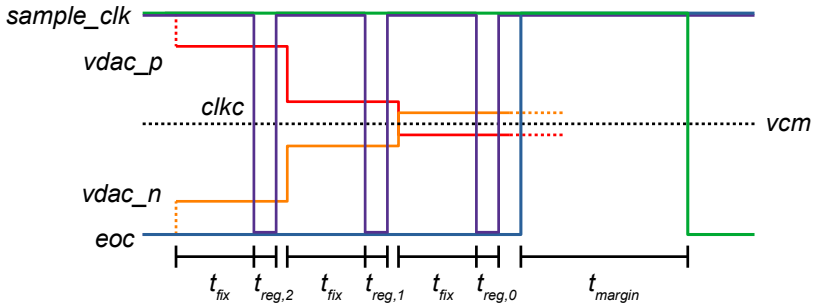
The timing diagram of the asynchronous SAR ADC is shown in Figure 2.7. In the diagram are pointed out the sampling clock (*sample_clk*), the comparator asynchronous clock (*clkc*), and the time intervals at which the signal sampling (t_{track}), the comparator regeneration (t_{reg}), and the comparator reset/DAC charge redistribution (t_{fix}) are performed. In Figure 2.8, the behavior of the *sample_clk*, *clkc*, *vdac_p*, *vdac_n*, and the end-of-conversion flag (*eoc*) are shown with details during the evaluation of the three least significant bits.

Figure 2.7 – Timing diagram of the asynchronous SAR ADC.



Source: Author, adapted from (YU, BANKMAN, *et al.*, 2019).

Figure 2.8 – Internal signal waveforms during the SAR procedure for the three least significant bits.



Source: Author.

For each of the iterations presented in Figure 2.8, the DAC charge redistribution

and the comparator reset are first triggered. After a fixed time interval t_{fix}, the *clkc* signal falls, indicating that a new differential input is provided for the comparator and that the comparator itself is ready. Next, a comparison (regeneration) is performed in a variable interval t_{reg} and, when the result is ready, a signal is sent to the asynchronous logic circuit, causing the rising of *clkc*. At the end of the iteration, the asynchronous logic commands the storage of the result and the start of a new iteration.

An end-of-conversion flag (*eoc*) will indicate that the SAR iterations were successfully performed, and the conversion result will be available at the output registers. The time delay between the beginning of the conversion phase and the rising of the *eoc* flag is mostly limited by the sum of comparator decision time during each iteration and the combinational circuits delay, due to its parasitic elements. For the iteration in which $(vdac\_p - vdac\_n) = \Delta V_{in}$ is the smallest, the regeneration time, $t_{reg,hard}$, can be much higher than the regeneration time of the other iterations.

Note that most of the ADC energy consumption is observed to occur in the interval between the rising of the sampling clock signal (triggering of the asynchronous logic circuit) and the rising of the *eoc* flag. Since the size of this time interval and the amount of operations performed in it does not scale with the sampling frequency, it is expected an almost linear relation between power consumption and sampling frequency (HARPE, ZHOU, *et al.*, 2010). This relation is compromised for low sampling frequencies, once in this case the ADC power consumption will be dominated by the static power consumption.

3. System level considerations

In this chapter some data conversion concepts are reviewed for better understanding of the design and performance indicators of the ADC. Next, characteristics, physical effects and architectures of its sub-circuits are introduced.

3.1. The ADC specifications

The specifications of an electrical circuit are the designer's guide to choose appropriated design techniques, leading to a better use of resources like silicon area and power consumption. Some of the most important ADC specifications are shown in this section.

3.1.1 Offset and gain error

The ADC offset error is defined as the shift of the actual ADC transfer curve from the ideal one (section 2.1). It indicates how much the first transition point, between 0…00 code to 0…01 code, is deviated from 1/2 LSB (JOHNS and MARTIN, 1997). It can be found mathematically as

$$E_{off(ADC)} = \frac{V_{0\ldots01}}{V_{LSB}} - \frac{1}{2}LSB, \tag{3.1}$$

where the $E_{off(ADC)}$ is the offset error in units of LSBs and $V_{0\ldots01}$ is the input voltage which produces the first transition in the actual ADC.

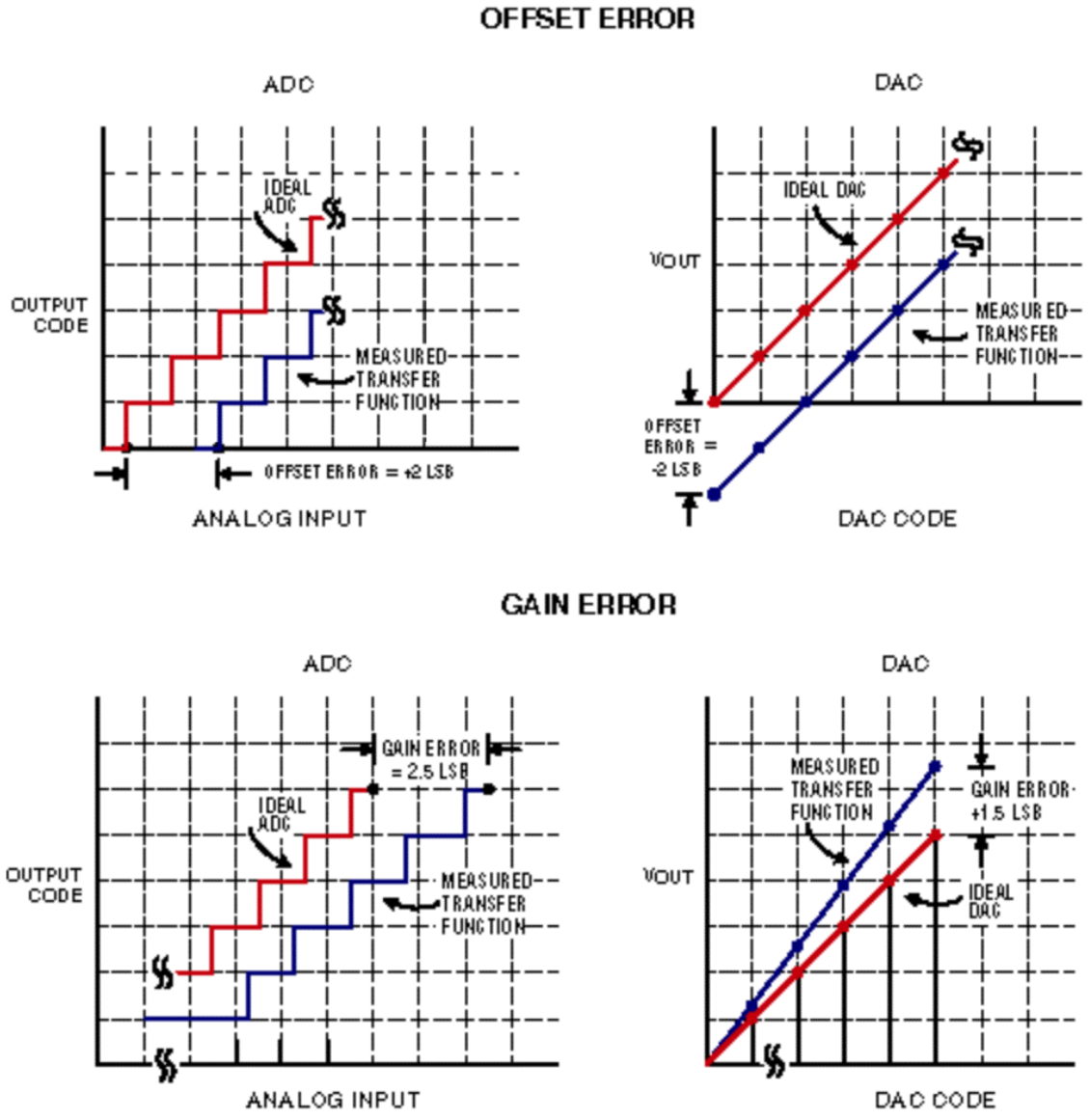
The ADC gain error is defined as the deviation of the last step's midpoint of the actual ADC transfer curve from the last step's midpoint of the ideal one, when the offset error is reduced to zero (JOHNS and MARTIN, 1997). The gain error indicates how well the slope of both transfer curves match each other (MAXIM INTEGRATED, 2002). It

can be found mathematically as:

$$E_{gain(ADC)} = \left(\frac{V_{1...11}}{V_{LSB}} - \frac{V_{0...01}}{V_{LSB}}\right) \; - \; (2^N - 2), \tag{3.2}$$

where the $E_{gain(ADC)}$ is the gain error and $V_{1...11}$ is the input voltage which produces the last transition in the transfer curve. The offset and gain errors in ADCs and DACs are shown in Figure 3.1.

Figure 3.1 – Offset and gain errors in ADCs and DACs.



Source: (MAXIM INTEGRATED, 2002).

3.1.2 DNL and INL

If we look at the transfer curve of an ideal *N*-bit ADC (section 2.1), it can be observed that each level ideally presents a width of 1 LSB. The ADC Differential Nonlinearity (DNL) error refers to the deviation in the width of any of these levels from the ideal value of 1 LSB. The analysis in (VAN DE PLASSCHE, 2003) states that the DNL error at an output code D can be written as

$$E(D)_{DNL} = (\frac{V_{m+1} - V_m}{V_{LSB}}) - 1LSB, \quad 0 < D < 2^N - 2. \tag{3.3}$$

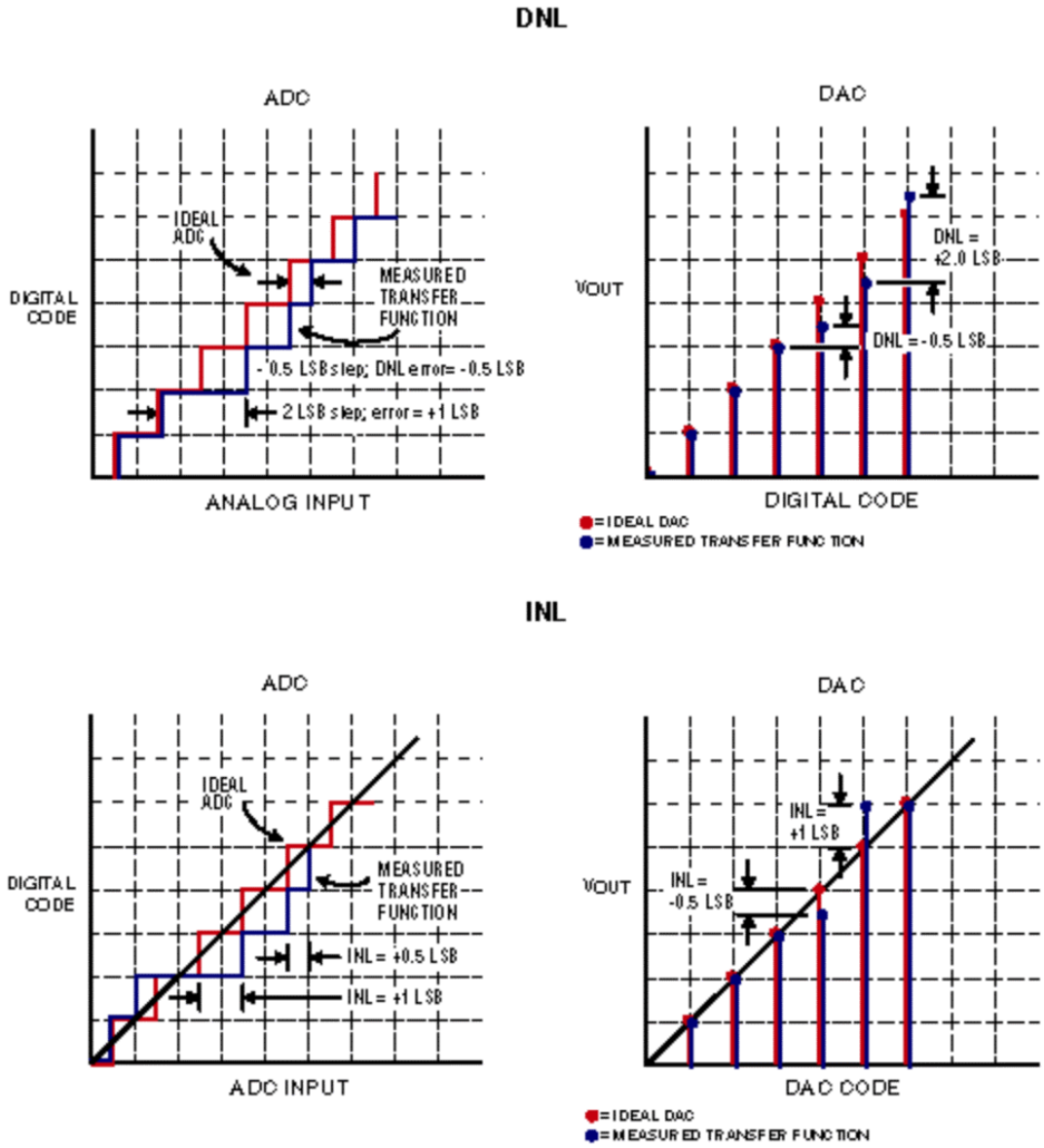
The V_m and V_{m+1} are two adjacent input voltages which produce, respectively, the transitions $(D - 1)$ to D and D to $(D + 1)$ in the transfer curve, once the offset and gain errors are removed.

The ADC Integral Nonlinearity (INL) is the deviation of the actual transfer curve from an imaginary straight line that passes through the middle points of all steps (JOHNS and MARTIN, 1997). The INL at the output code D can be computed as the sum of the DNLs from code 1 up to code D. The INL calculation is also performed after offset and gain errors have been compensated and can be found as

$$E(D)_{INL} = \Big(\frac{V_{m,ideal} - V_{m,actual}}{V_{LSB}}\Big). \tag{3.4}$$

The DNL and INL errors in ADCs and DACs are shown in Figure 3.2. Note that if the maximum DNL error is less than 1 LSB and the maximum INL error is less than 0.5 LSB, the ADC is guaranteed to not present any missing codes in its transfer function (JOHNS and MARTIN, 1997). Also, unless otherwise stated, the literature often considers the DNL/INL error as the maximum DNL/INL error found in the full transfer function span.

Figure 3.2 – DNL and INL errors in ADCs and DACs.



Source: (MAXIM INTEGRATED, 2002).

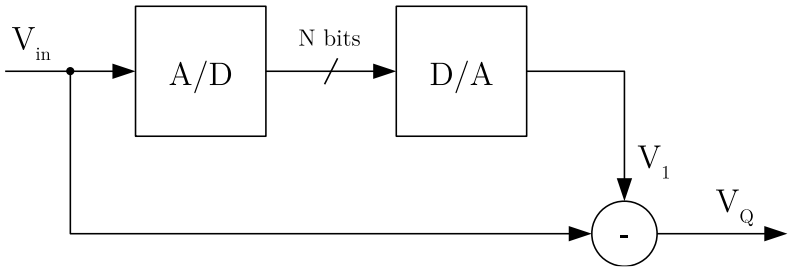
3.1.3 Quantization noise and SNR

Quantization is a process of dividing a quantity in a discrete number of small parts (GRAY and NEUHOFF, 1998). In data converters, this process is unavoidable and introduces error (quantization error) even in ideal circuits (JOHNS and MARTIN, 1997), as shown in section 2.1.

The stochastic analysis, presented in (JOHNS and MARTIN, 1997), can be used to better understand the impact of this error in the performance of the ADC. First, we

consider the circuit shown in Figure 3.3, composed by two *N*-bits ideal converters, where the quantization noise signal, V_Q, is modeled as the quantized signal, V_1, minus the input signal, V_{in}.

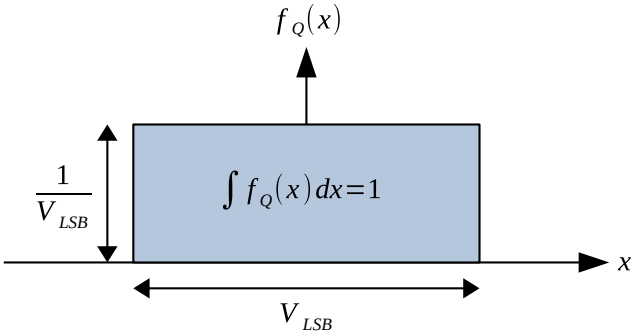
Figure 3.3 – An observation of quantization error.



Source: Author, adapted from (JOHNS and MARTIN, 1997).

In this analysis, V_Q is considered to present a uniform distribution in the range from $-V_{LSB}/2$ up to $+V_{LSB}/2$, as shown in Figure 3.4, where $f_Q(x)$ is the error probability density and x is the quantization error.

Figure 3.4 – Assumed error probability density function for the quantization error.



Source: Author, adapted from (JOHNS and MARTIN, 1997).

The Root-Mean-Square (RMS) value of the error V_Q can be calculated as

$$V_{Q(rms)} = \left[\frac{1}{V_{LSB}}\left(\int_{\frac{-V_{LSB}}{2}}^{\frac{V_{LSB}}{2}} x^2\,dx\right)\right]^{1/2} = \frac{V_{LSB}}{\sqrt{12}}. \tag{3.5}$$

Now, the RMS value of V_Q can be used to determine the Signal-to-Noise Ratio (SNR) of an ideal ADC. The SNR is the most important ADC specification and is a good indication of its dynamic performance (VAN DE PLASSCHE, 2003). It is used to analyze how much noise was added into the original signal by the ADC after a conversion. The

SNR of an ideal N-bit ADC due to quantization error is calculated by taking the logarithm of the ratio between the power of a full-scale sinusoidal input, with amplitude of $2^{N-1} \cdot V_{LSB}$, and the estimated power of the quantization error, V_Q, leading to

$$SNR = 20\log\left(\frac{\frac{V_{LSB} \cdot 2^{N-1}}{\sqrt{2}}}{\frac{V_{LSB}}{\sqrt{12}}}\right) = 6.02N + 1.76dB. \tag{3.6}$$

Therefore, an ideal 10-bit ADC will present a SNR of 61.96 dB, meaning that this is the maximum theorical SNR value for a 10-bit ADC. Non-ideal ADCs present a degraded SNR because the non-ideal characteristic curve and the other sources of noise will increase V_Q in the denominator of equation 3.6.

Note that equation 3.6 is a simplified estimative of the SNR. Although there are more accurate deductions of the SNR for converters with resolutions above 3 bits, equation 3.6 is a general accepted formula (VAN DE PLASSCHE, 2003).

3.1.4 SINAD and ENOB

The Signal-to-Noise-and-Distortion (SINAD) parameter indicates how much noise and distortion were added into the original signal after the analog-to-digital conversion. It is an important specification because its calculation includes the SNR and the Total Harmonic Distortion (THD) as components that degrade the performance of the ADC. The SINAD relation is (ANALOG DEVICES, 2005):

$$SINAD = 20\log\frac{V_{in(RMS)}}{\sqrt{V_{Q(RMS)}^2 + V_{h(RMS)}^2}}, \tag{3.7}$$

where $V_{h(RMS)}$ is the RMS of the harmonic distortion.

The SINAD can be estimated by first applying a sinusoidal signal in the input of the ADC, turning the circuit on during a predefined number of conversions and saving the outputs into a vector of binary codes. Next, the binary codes are converted to analog values and the Discrete-Time Fourier Transform (DTFT) is applied to generate the

frequency spectrum of the converted signal. The computation of the DTFT requires a high computational power, so, in practice, it is taken the Discrete Fourier Transform (DFT) (OPPENHEIM and SCHAFER, 1999).

Finally, the SINAD is calculated by taking the RMS value of the base frequency component and dividing by the root-sum-square of all other spectral components, including harmonics and excluding the Direct Current voltage (DC) level component (ANALOG DEVICES, 2009).

For ADC testing and characterization this parameter is usually converted to Effective Number of Bits (ENOB). To find the ENOB, one replaces the SNR in equation 3.6 by the measured circuit SINAD, leading to a non-ideal value for N, that express the effective resolution:

$$ENOB = \frac{SINAD - 1.76dB}{6.02}. \tag{3.8}$$

Measuring the ENOB, however, can lead to errors if the input signal approaches full scale because the output codes can saturate at codes 0 or $2^N - 1$, significantly degrading the DFT spectrum. A practical method for better ENOB measurement is to use a reduced input signal level and apply a correction factor in equation 3.8 (ANALOG DEVICES, 2009) leading to the new expression

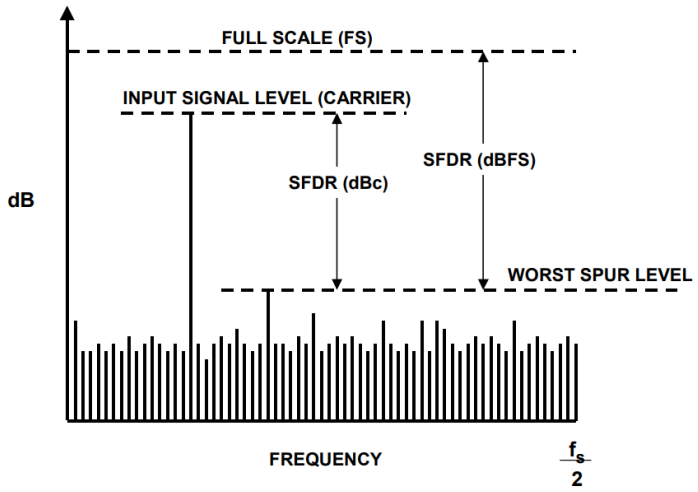
$$ENOB = \frac{SINAD - 1.76dB + 20\log\left(\frac{Fullscale\ Amplitude}{Input\ Amplitude}\right)}{6.02}. \tag{3.9}$$

3.1.5 Spurious-Free Dynamic Range

The Spurious-Free Dynamic Range (SFDR) is a specification that indicates how much is the difference between the maximum, or fundamental, carrier component and the largest distortion component in the frequency spectrum of the converted output signal (VAN DE PLASSCHE, 2003). The SFDR is calculated by dividing the input signal component by the largest distortion component. In Decibels relative to the carrier (dBc)

scale, it can be easily extracted from the frequency spectrum graph by taking the input signal component and subtracting the largest distortion component, as shown in Figure 3.5. For practical converters, the predominant distortion components are the second and third harmonics.

Figure 3.5 – Frequency spectrum, in dB, and the measurement of the SFDR.



Source: (ANALOG DEVICES, 2005).

3.1.6 Bit Error Rate and Converter Error Rate

The Bit Error Rate (BER) of a digital system is the number of errors expected to be observed in data transmissions. The specification of the BER of a system is somewhat subjective and takes in account the desired average time between errors, which can vary significantly for different applications (VAN DE PLASSCHE, 2003). The Conversion Error Rate (CER) of an ADC is a figure that estimates the probability of a converted code to present an erroneous value.

Even though both parameters seems to be similar, their errors have different causes, as pointed out in (BEAVERS, 2014). For example, the determination of the BER of a digital system is straightforward because one can simply transmit a specific set of data and observe it at the receiver side. The difference between the received and expected data are counted as bit errors. On the other hand, the determination of the CER of an

ADC requires special attention because the cause of an erroneous data conversion could be from an intrinsic characteristic of the converter, like DNL, INL, offset and gain error, or could be a non-expected conversion error mainly due to noise and/or metastability problems. The CER of a SAR ADC is typically dominated by the probability of its comparator entering in a metastable state, which is introduced in sub-section 3.4.4

3.1.7 Figure of Merit

A well accepted index for comparison of different ADCs is the Figure of Merit (FOM) (VAN DE PLASSCHE, 2003) given by

$$FOM = \frac{Power}{2.f_{in}.2^{ENOB}}, \tag{3.10}$$

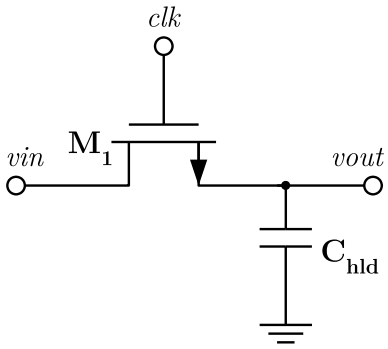
where FOM is expressed in J/Conversion-steps, f_{in} is the fundamental frequency of the input signal, $ENOB$ is the equivalent number of bits and $Power$ is the power consumption. For Nyquist-rate ADCs, the applied input signal frequency should be slightly lower than half the sampling frequency.

3.2. The sample and hold circuit

Sample and hold circuits are widely used in ADCs. They are responsible for sampling an analog signal and storing its value for some defined time for analysis. A simple example of such circuit is shown in Figure 3.6.

This sample and hold circuit is composed by a simple switch, the Metal-Oxide-Silicon (MOS) transistor M_1, and a storage element, the hold capacitor C_{hld}. As analyzed in (JOHNS and MARTIN, 1997) when *clk* is logical high, transistor M_1 is on and *vout* follows *vin*. When *clk* goes low, transistor M_1 is off and *vout* will remain ideally constant, having a value equal to *vin*. In practice, *vout* will present errors due to charge flow in and from C_{hld} and parasitic capacitances.

Figure 3.6 – A basic sample and hold circuit.



Source: Author, adapted from (JOHNS and MARTIN, 1997).

3.2.1 Switch-induced error

The sample hold switches present two well-known error sources responsible by the so-called switch-induced error: the charge injection and the clock feedthrough. The charge injection error is caused by the transistor channel charge that goes to the capacitor when the transistor goes to off. The first-order analysis in (JOHNS and MARTIN, 1997) estimates the charge injection error by calculating the charge flow from the channel into C_{hld}. In Figure 3.6, considering the clock signal is fast enough, the channel charge (Q_{ch}) is expected to flow evenly to both transistor terminals (source and drain) (SHIEH, PATIL and SHEU, 1987). The charge variation in C_{hld} is then given by

$$\Delta Q_{C_{hld}} = \frac{Q_{ch}}{2} = \frac{C_{ox} W L V_{eff}}{2}, \tag{3.11}$$

where C_{ox} is the gate-oxide capacitance per area of the transistor, W and L are the width and length of the transistor, and V_{eff} is given by

$$V_{eff} = V_{GS1} - V_{TH} = V_{DD} - V_{TH} - vin, \tag{3.12}$$

where V_{GS1} is given by the difference between the *clk* voltage at logical high (V_{DD}) and the input voltage (*vin*), and V_{TH} is the threshold voltage of the transistor. We can find the voltage error due to charge injection, ΔV', by using the relationship Q = CV in equation 3.11, which results in

$$\Delta V' = -\frac{C_{ox}WL(V_{DD} - V_{TH} - vin)}{2C_{hld}}. \tag{3.13}$$

The clock feedthrough error is caused by the coupling between the *clk* and the *vout* signals. The coupling is due to the gate-drain/source overlap capacitances of the MOS transistor. Further analysis is performed in (JOHNS and MARTIN, 1997) to estimate the voltage error in *vout* due to the clock feedthrough. The gate overlap capacitance (C_{OV}) of M_1 forms a capacitor arrangement with C_{hld}. The charge variance in C_{OV}, due to the *clk* transition from high to low, $Q_{OV} = C_{OV}\,(V_{DD} - V_{SS})$, will cause in *vout* a voltage error, $\Delta V''$, whose value can be calculated by using the capacitor-divider formula

$$\Delta V'' = -\frac{(V_{DD} - V_{SS})C_{OV}}{C_{hld} + C_{OV}}, \tag{3.14}$$

which can be approximated by

$$\Delta V'' \cong -\frac{C_{ox}WL_{OV}(V_{DD} - V_{SS})}{C_{hld}}, \tag{3.15}$$

where V_{SS} is the *clk* low logical level and L_{OV} is the gate-drain/source overlap length.

The effect described by equation 3.13 is called charge injection and its contribution to the total voltage error is more expressive that the one described in equation 3.15, which is known as clock feedthrough. Note that for differential sampling circuits, where two symmetrical switches are employed, the effects of clock feedthrough are minimized because both branches will present similar errors. However, the effect of charge injection will not cancel out because it is dependent on *vin*.

3.2.2 The bootstrapped switch

The design of high linear analog switches is essential when it comes to design of medium-to-high resolution ADCs. Say a *N*-bit SAR ADC must be designed. If the error added by the switch into the sampled signal is higher than half the V_{LSB}, the effective resolution of the converter will be degraded. Therefore, bootstrapped switches have been

widely used in SAR ADCs (DYACHENKO, 2012) (FIRLEJ, FIUTOWSKI, *et al.*, 2015), which present high linearity by keeping its on-resistance nearly constant even for a wide input swing (STEENSGAARD, 1999).

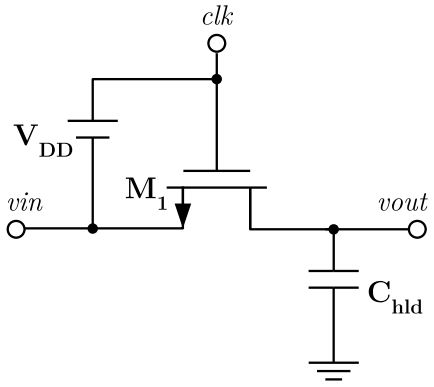
As stated in (RAZAVI, 2001), the on-resistance of a n-type MOS (NMOS) transistor in triode region depends on V_{eff} (equation 3.12) and is given by

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})} = \frac{1}{\mu_n C_{ox} \frac{W}{L} V_{eff}}, \tag{3.16}$$

where R_{ON} is the on-resistance of the transistor and μ_n is the electron mobility. Equation 3.16 elucidates that basic switches, like the one implemented in the sample and hold circuit in Figure 3.6, suffer from a nonlinear behavior due to different input voltage levels, that induce distortions.

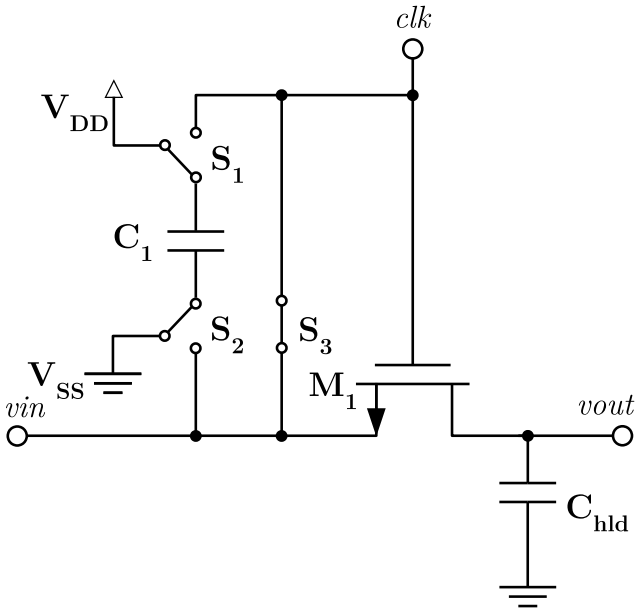
The bootstrapped switch can minimize this problem, as mentioned before, by maintaining V_{GS} constant over the entire input swing, although a small variation in V_{TH} will still be present. The circuit concept is illustrated in Figure 3.7. In this circuit, V_{GS1} is kept constant by mean of a voltage source. In general, the value of the voltage source is chosen to be equal to V_{DD}, which implies that the transistor gate voltage should go from V_{DD} to $2\,V_{DD}$ when the input changes from V_{SS} to V_{DD}. A practical implementation of the voltage source makes use of a switched capacitor circuit to perform voltage doubling and is shown in Figure 3.8.

Figure 3.7 – Bootstrapped switch concept, at sampling phase.



Source: Author, adapted from (STEENSGAARD, 1999).

Figure 3.8 – Switched capacitor for bootstrapped switch.



Source: Author, adapted from (STEENSGAARD, 1999).

The switched capacitor circuit is composed by three switches and the capacitor C_1. Its operation is as follows: during the hold phase the C_1 is charged to V_{DD} and the gate of M_1 is shorted to its source. During the sample phase the gate and source of M_1 are not shorted anymore and C_1 is attached to them, producing a constant V_{GS1}.

3.2.3 Thermal noise

As shown in Figure 3.6, a basic sample and hold circuit is made of a switch and a hold capacitor. The switch analysis of (RAZAVI, 2001) estimates the noise due to random motion of electrons, which induces fluctuations in the voltage across a conductor. This noise is proportional to temperature and is known as thermal noise.

Prior the analysis of this circuit, the thermal noise of a resistor is introduced, since a non-ideal MOS switch, in triode region, has the behavior similar to that of a resistor. The Power Spectral Density (PSD), $S_v(f)$, of the thermal noise of a resistor R is

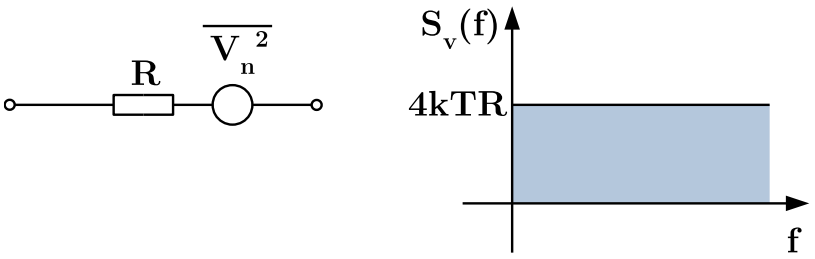
$$S_v(f) = 4kTR, \ f \geq 0, \tag{3.17}$$

where $k = 1.38.10^{-23}$ J/K is the Boltzmann constant. The $S_v(f)$, expressed in V^2/Hz, states

how much power the signal carries at each frequency (per 1Hz bandwidth).

In circuit analysis, the thermal noise of a resistor can be modeled as a voltage source in series with the noiseless resistor, as shown in Figure 3.9.

Figure 3.9 – Thermal noise of a resistor.



Source: Author, adapted from (RAZAVI, 2001).

It is important to notice that noise is a random process, meaning that instantaneous values of voltages and currents cannot be predicted. The average power, though, is predictable in many cases and can be calculated from a long time scale waveform. So, the voltage source of Figure 3.9 indicates the average power (noise voltage squared). In fact, $\overline{V_n^{\,2}} = 4kTR\Delta f$, where Δf is the frequency band of the measurement.

The model for the resistor thermal noise can be applied into the calculation of the noise generated by a simple RC low pass filter to proper estimate the noise introduced by the sample and hold circuit. As shown in Figure 3.10, the series voltage source that represents the noise of R, V_R, is used to compute the transfer function

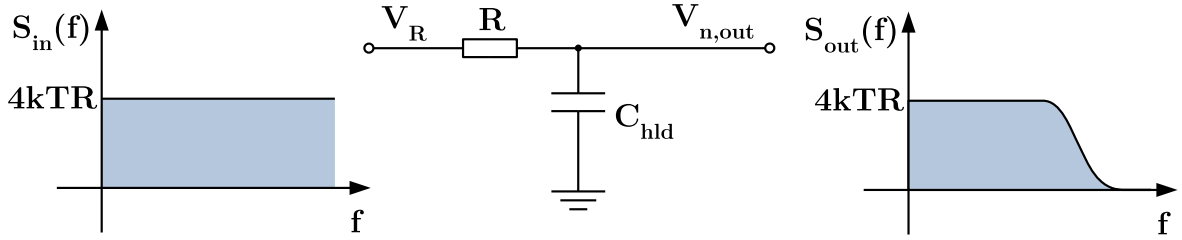
$$\frac{V_{out}}{V_R}(s) = \frac{1}{RCs + 1}. \tag{3.18}$$

In a Linear Time-Invariant (LTI) system, the PSD of the input signal, $S_{in}(f)$, and the PSD of the output signal, $S_{out}(f)$, are related by the following theorem (COUCH, 1993):

$$S_{out}(f) = S_{in}(f)|H(f)|^2, \tag{3.19}$$

where $H(f)$ is the transfer function of the LTI system.

Figure 3.10 – Noise spectrum shaping by a low pass filter.



Source: Author, adapted from (RAZAVI, 2001).

By combining equations 3.18 and 3.19 we obtain the expression of the PSD at the output of the sample and hold circuit, which can be integrated, in frequency domain, to provide the total noise power in the output, resulting in

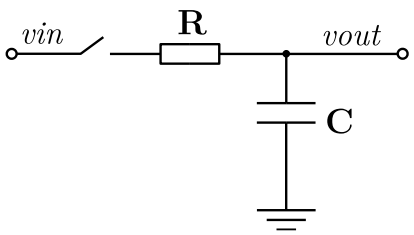
$$P_{noise,out} = \frac{kT}{C_{hld}}. \tag{3.20}$$

The unit of $P_{noise,out}$ is V^2 and we can take the square root of this expression to obtain the RMS noise, also known as KTC noise.

3.2.4 Track bandwidth

Switched-capacitor based sampling circuits have a limited capacity of charging/discharging its hold capacitor at high frequency operation. The maximum input signal frequency is limited by the RC nature of the circuit, which can be analyzed as a simple RC charging circuit, shown in Figure 3.11.

Figure 3.11 – A simple RC circuit.



Source: Author.

In the abovementioned circuit, the hold capacitor is initially discharged and the input voltage V_{in} is constant. When the switch is closed it will present the voltage settling

behavior given by the charging capacitor equation

$$V_{out}(t) = V_{in}\left[1 - e^{\frac{-t}{RC}}\right]. \tag{3.21}$$

Considering the circuit has a 50% duty cycle, i.e., the switch is turned on during half of the sampling period, the voltage in the hold capacitor has this exact amount of time to settle to the input signal with some voltage error, according to specifications.

The maximum allowed voltage error for a 10-bit SAR ADC, with input swing of $V_{in} = V_{DD}$, is

$$\Delta V_e \leq \frac{V_{LSB}}{2} = \frac{V_{DD}}{2^{N+1}}, \tag{3.22}$$

where N is the ADC resolution.

Combining equations 3.21 and 3.22, the constraint for track bandwidth is

$$\frac{1}{2^{N+1}} \leq e^{\frac{-0.5T_S}{RC}}, \tag{3.23}$$

where T_S is the sampling period.

3.2.5 Coherent sampling

Coherent sampling is a relevant topic in characterization of ADCs. Suppose we need to plot the frequency spectrum of the output waveform of an ADC. One approach is to apply a sinusoidal signal in the input of the ADC, turn the circuit on during a predefined number of conversions (data window) and save the outputs into a vector of binary codes. Now, similarly to the process described in sub-section 3.1.4, each element of this vector is converted to uniformly-spaced samples of continuous values and the DFT of the resulting vector is performed to obtain the converted signal in the frequency domain.

Since the DFT supposes a periodic expansion of the signal in the time domain, the correct representation of the signal in the frequency domain is only achieved when

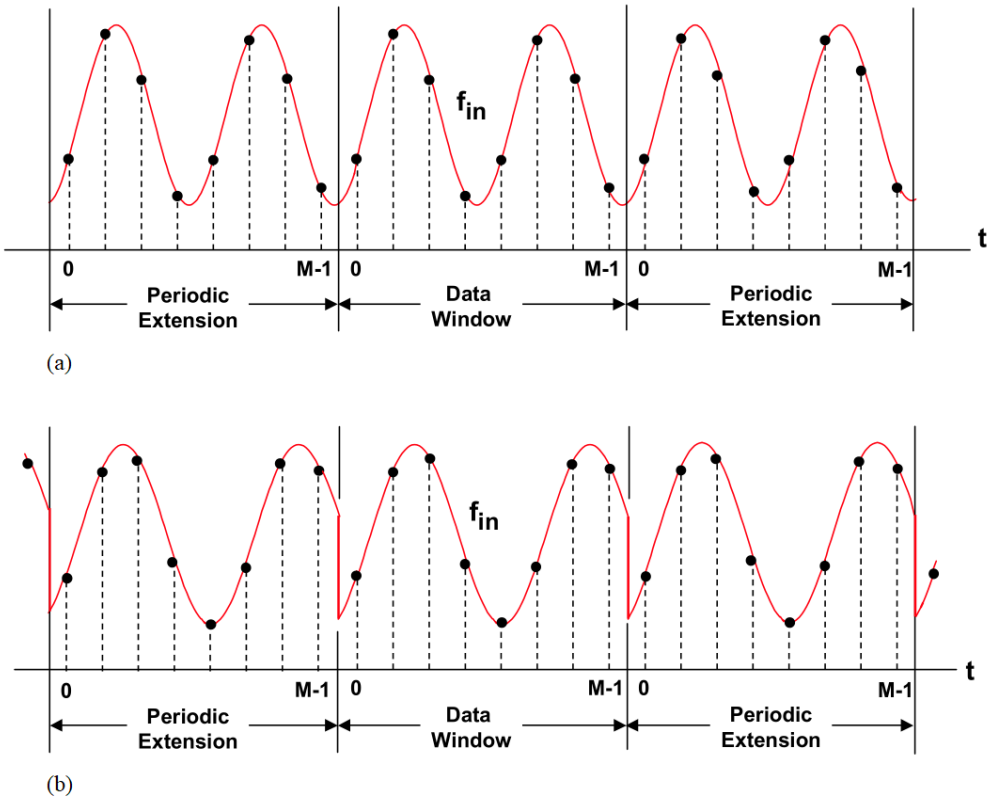
the sample frequency is set to sample an integer number of periods in the sampling window (MAXIM INTEGRATED, 2002), as shown in Figure 3.12(a). If a non-integer number of periods is used to compute the DFT, the periodic expansion of the data window will present a discontinuity, as shown in Figure 3.12(b), and the frequency components of the signal will present incorrect magnitudes.

The sampled waveform discontinuity (spectral leakage) can be reduced if the following condition is true:

$$\frac{f_{in}}{f_{sample}} = \frac{N_{window}}{N_{record}}, \tag{3.24}$$

where f_{in} is the periodic input signal, f_{sample} is the sampling frequency of the ADC, N_{window} is the integer number of cycles that the signal completes within the sampling window and N_{record} is the number of samples stored for the DFT computation.

Figure 3.12 – (a) Sinewave having integral number of periods in the sample window. (b) Sinewave having a non-integral number of periods in the sampling window.



Source: (ANALOG DEVICES, 2005).

Note that there are some restrictions on choosing N_{record} and N_{window}: for taking advantage of the numerical algorithms that implement the DFT, N_{record} must be a power of 2. Additionally, to ensure samples will not be repeated across any signal period, a prime number (except for 2) must be chosen for N_{window}.

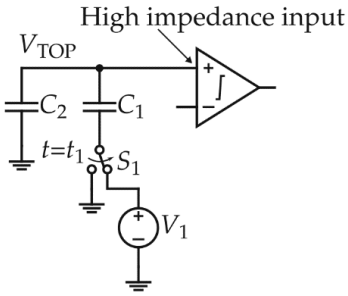
3.3. The capacitor array

Low-power SAR ADCs that use capacitive DACs typically adopt the charge sharing or charge redistribution techniques (RABUSKE and FERNANDES, 2017). In this section, the charge redistribution technique is presented for proper introduction of the split array topology and the merged capacitor switching scheme.

3.3.1 Charge redistribution

The charge redistribution technique has been largely employed in SAR ADCs during the last decades. By taking advantage of the constant charge in a capacitor network, one may switch the bottom plate of any number of its elements to different voltage levels in order to induce a defined voltage level at the top plate of the capacitors (common node). The example of Figure 3.13 illustrates this concept.

Figure 3.13 – Charge Redistribution Concept.



Source: (RABUSKE and FERNANDES, 2017).

In this example, as analyzed in (RABUSKE and FERNANDES, 2017), the voltage variation in V_{TOP} caused by switching S_1 is derived as follows. When $t=t_0$ the bottom plates of both capacitors are shorted to ground, and their total charge, Q_{TOP}, is given by

$$Q_{TOP}(t_0) = V_{TOP}(t_0)(C_2 + C_1). \tag{3.25}$$

Now, consider that at $t{=}t_1$ the bottom plate of C_1 is switched to V_1 through S_1. After proper settling of V_{TOP} at t_2, where $t_0{<}t_1{<}t_2$, the charge in the top plates is given by

$$Q_{TOP}(t_2) = V_{TOP}(t_2)C_2 + (V_{TOP}(t_2) - V_1)C_1. \tag{3.26}$$

Since there is conservation of charge in the top plate, we can state that $Q_{TOP}(t_0){=}Q_{TOP}(t_2)$, leading to

$$V_{TOP}(t_2) = V_{TOP}(t_0) + V_1 \frac{C_1}{C_1 + C_2}. \tag{3.27}$$

By extrapolating this concept, an increased number of capacitors can be used to define an increased number of possible voltage levels for V_{TOP}.

3.3.2 Split binary-weighted capacitive array

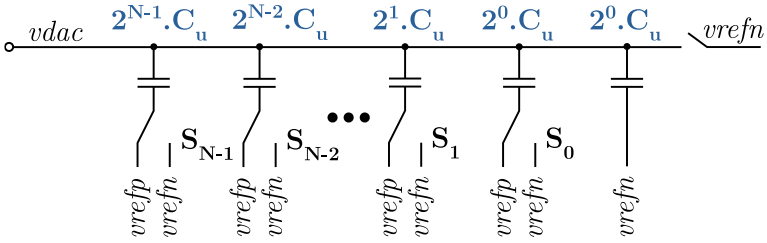
SAR ADCs must implement the binary search algorithm. By using the charge redistribution concept described in the previous sub-section with capacitors placed in a binary-weighted pattern, as first introduced in (MCCREARY and GRAY, 1975), the binary search algorithm can be easily performed in hardware. Figure 3.14 shows the implementation of a DAC used in a typical SAR ADCs, where N is the resolution of the ADC, *vrefp* is the high reference voltage node (typically V_{DD}), *vrefn* is the low reference voltage node (typically ground) and C_u is the capacitance value of the unit capacitor C_U. In the reset phase, the bottom plates of all capacitors are connected to *vrefn* and the top plates are connected to a reset voltage (in this case, *vrefn*). In the conversion phase, each bottom plate can either remain connected to *vrefn* or switch to *vrefp*, leading to different voltage levels in *vdac* according the positions of the switches. Considering that a signal s_i controls the switch S_i, and when $s_i = 0$ the switch S_i will connect the capacitor to *vrefn*,

otherwise, when $s_i = 1$, it will connect to *vrefp*, then

$$V_{DAC} = \sum_{i=0}^{N-1} s_i \cdot \frac{(V_{REFP} - V_{REFN})}{2^{N-i}}. \tag{3.28}$$

Although this topology has been extensively used by mixed-signal IC designers, the physical implementation of such circuit becomes quite expensive when N is increased because the number of elements in the capacitor array grows exponentially. This holds even when C_U is implemented with the smallest available device from a given technology.

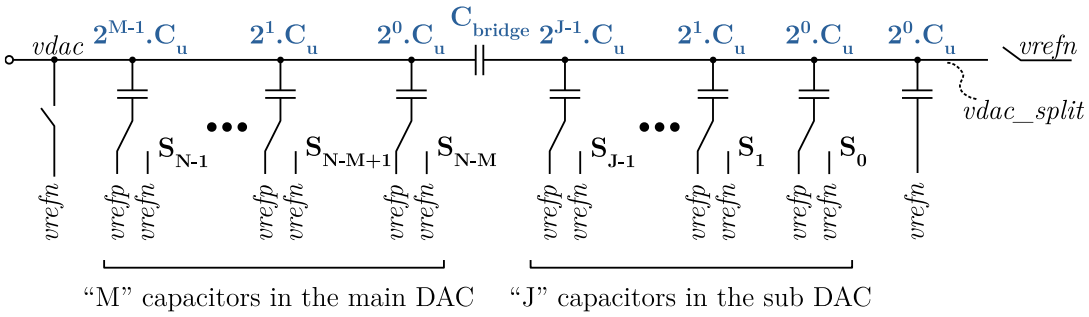
Figure 3.14 – The binary-weighted capacitive DAC.



Source: Author, adapted from (BAKER, 2010).

In order to reduce the size of the capacitor array, the split binary-weighted capacitive array architecture (BAKER, 2010) places a bridge (or attenuation) capacitor C_{bridge}, as shown in Figure 3.15, to split the capacitive DAC in two DACs. In this architecture, the binary-weighted arrangement is preserved, and J elements (capacitor plus switch) are placed into a sub DAC, as well as M elements into the main DAC. The series association of C_{bridge} and the sub DAC can provide capacitance values, referred to the main DAC, which ranges from $2^{-J} \cdot C_u$ up to C_u, according the binary code. To accomplish it, the series association of the capacitor C_{bridge} and the capacitor array of the sub DAC, when all their bottom plates are short-circuited, must have the capacitance value of C_u. Unfortunately, in general, it leads to a value of C_{bridge} which is not an integer multiple of C_u.

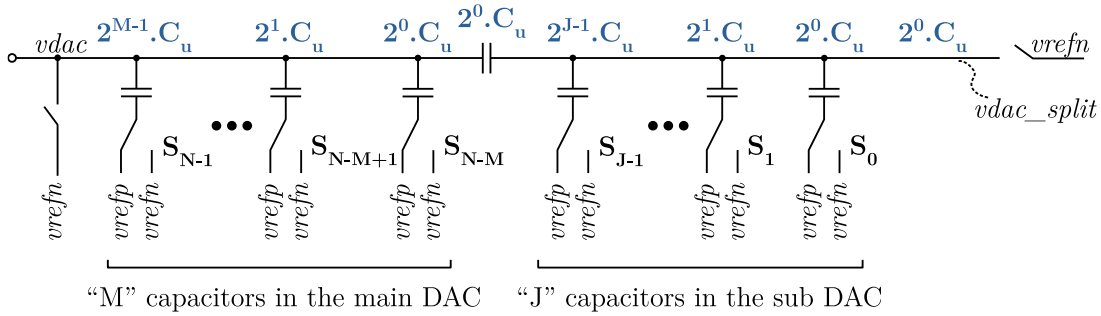
Figure 3.15 – The split binary-weighted capacitive array.



Source: Author, adapted from (BAKER, 2010).

A practical implementation of the split technique is depicted in (ZHANG, 2012) and is shown in Figure 3.16.

Figure 3.16 – The modified split binary-weighted capacitive array.



Source: Author, adapted from (ZHANG, 2012).

In this implementation, C_{bridge} is replaced by C_U and the capacitor related to the LSB of the sub DAC (the capacitor placed more to the right) is removed to compensate the voltage scaling. The resulting circuit aims to avoid a fractional capacitance value, improving the layout and the array matching, although the gain error is augmented.

For low-power applications, C_u is set as small as possible. Its value is limited mainly by thermal noise introduced by the switches and the capacitor mismatches. Due to the thermal noise in sample and hold circuits, introduced in sub-section 3.2.3, the minimum value of C_u is estimated by constraining the KTC noise, with a hold capacitor of $2^M \cdot C_u$ (equivalent DAC capacitance), to be less than the quantization noise of the converter.The mismatch limitation arises from the variability in the fabrication process.

The fabricated C_U device presents, in practice, a mean capacitance value of C_u with a standard deviation of σ_u, which can result in DNL and INL errors. The analysis in (ZHANG, 2012) concludes that, for the split binary-weighted capacitive array, the mismatch in the main DAC is the major contribution to the worst case DNL. The INL analysis was not carried out because the DNL error is more expressive than the INL one. The worst-case standard deviation of DNL is

$$\sigma_{DNL,MAX} = \sqrt{2^M - 1}\,\frac{\sigma_u}{C_u} LSB', \tag{3.29}$$

where $LSB' = V_{REF}/2^M$.

Considering that Metal-Insulator-Metal (MIM) capacitors are employed for better matching, its effective fabrication characteristics can be analyzed in order to better estimate the yield. Some parameters can be either straightforwardly read or calculated. For MIM capacitors, they relate as follows

$$\begin{cases} \sigma(\frac{\Delta C}{C}) = \frac{K_\sigma}{\sqrt{A_C}}, \\ C = K_C \cdot A_C \end{cases} \tag{3.30}$$

where K_C is the capacitor density, A_C is the capacitor area, K_σ is the matching coefficient and $\sigma(\Delta C/C)$ is the standard deviation of the difference of two identical capacitors, normalized to their absolute value C. Considering that the standard deviation of a single capacitor is smaller than the standard deviation of the difference of two capacitors, by a factor of $\sqrt{2}$ (HAENZSCHE, HENKER and SCHÜFFNY, 2010), we can write:

$$\frac{\sigma_u}{C_U} = \frac{K_\sigma}{\sqrt{2}\sqrt{A_C}}. \tag{3.31}$$

where σ_u is the standard deviation of the value of C_u.

Therefore, the minimum value of C_u due to mismatch restrictions is estimated by combining the previous equations with the constraint $3\sigma_{DNL,MAX} < 1/2\text{LSB}$ to ensure monotonicity, leading to

$$C \geq 9 \cdot (2^M - 1) \cdot 2^{2(N-M)} \cdot K_\sigma^2 \cdot K_C. \tag{3.32}$$

Note that this restriction can be relaxed by half when the circuit is made differential, because the signal range is doubled whereas the mismatch error is only increased by a factor of $\sqrt{2}$ (ZHANG, 2012).

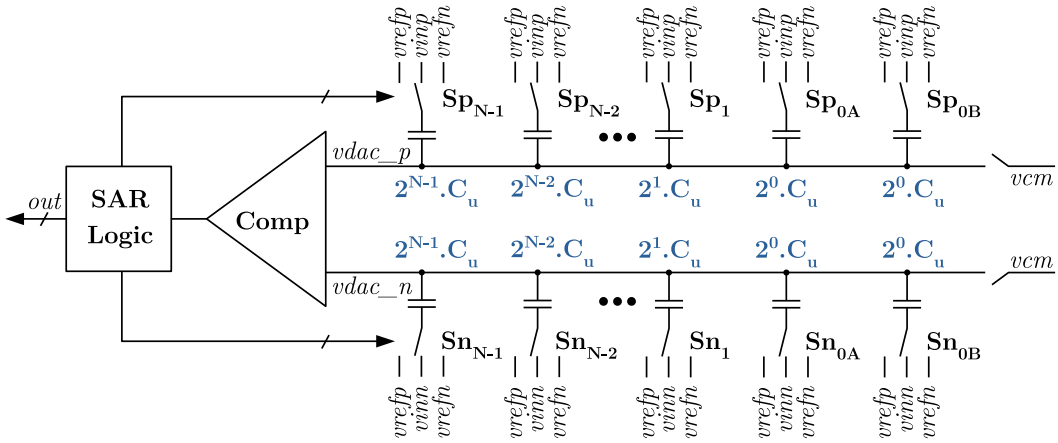
3.3.3 The merged capacitor switching scheme

The capacitive DACs presented in the previous sub-section have the voltage level of *vdac* changed by simply connecting the bottom plates of the capacitors to either *vrefp* or *vrefn*. Although the conventional approach is quite simple, it does not make an efficient use of the energy charged in the capacitor array when the circuit is employed in SAR ADCs.

Take the conventional implementation of Figure 3.17 as an example. In this scheme, the bottom plates of all capacitors can be connected to *vrefp*, *vrefn* or to the input voltage (*vinp*/*vinn*), whereas the top plates (*vdac_p*/*vdac_n*) can be connected to the common mode voltage, *vcm*, or left floating. Since it is differential, the positive (*vdac_p*) and negative (*vdac_n*) sides are complementary and only the positive side will be analyzed. At the beginning of the binary search algorithm, all its capacitors present their bottom plates connected to the input signal *vinp* and their top plates shorted to *vcm*. Next, the top plates are disconnected from *vcm*, the top plate of the Most Significant Bit (MSB) capacitor is connected to *vrefp* and the remaining capacitors have their bottom plates connected to *vrefn*. Then, after voltage settling, if *vdac_p* is higher than *vdac_n*, the bottom plate of the MSB capacitor remains connected to *vrefp* (*up* transition). On the other hand, if it was found that *vdac_p* is lower than *vdac_n*, the MSB capacitor must be connected to *vrefn* (*down* transition), wasting energy and leading to asymmetry in the power consumption for *up* and *down* transitions (CHEN, TSUKAMOTO and KURODA, 2009).

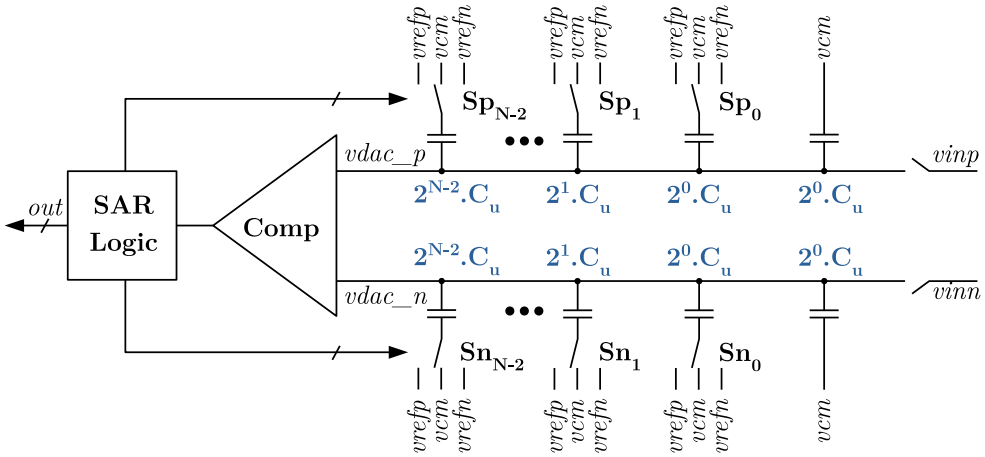
The Merged Capacitor Switching (MCS) scheme (HARIPRASATH, GUERBER, *et al.*, 2010) requires a much lower average energy to charge/discharge these capacitors. A differential implementation of the MCS is shown in Figure 3.18. In this scheme, the bottom plate of all capacitors (with exception to the last one) can be connected to *vrefp*, *vrefn* or to the common mode voltage, *vcm*, whereas the top plates (*vdac_p*/*vdac_n*) can be connected to the input voltage (*vinp*/*vinn*) or left floating. Since the input signal is connected to the top plate of the capacitor array, this sampling method used by the MCS is also known as top-plate sampling.

Figure 3.17 – A conventional differential 10-bit SAR ADC.



Source: Author, adapted from (LIU, CHANG, *et al.*, 2010).

Figure 3.18 – The Merged Capacitor Switching scheme (MCS).



Source: Author, adapted from (HARIPRASATH, GUERBER, *et al.*, 2010).

In the MCS scheme, at the sampling phase of the ADC, the bottom plates of all capacitors are shorted to the common-mode voltage, *vcm*, and the top plate of the capacitors are connected to the differential input signal. During the conversion phase, the DAC is decoupled from the input signal and N iterations are performed during the SAR procedure. The sequence of steps in the conversion phase is as follows: in the first iteration, *vdac_p* and *vdac_n* are compared and the result is stored in the MSB of the output register. In the second iteration, if it was found that *vdac_p* was higher than *vdac_n* in the previous iteration, Sp_{N-2} and Sn_{N-2} switches to *vrefn* and *vrefp*, respectively (*down* transition), or, if *vdac_p* was lower than *vdac_n*, to *vrefp* and *vrefn* (*up* transition). A new comparison between *vdac_p* and *vdac_n* is performed, and the result is stored in the second MSB of the output register. In the next iterations, Sp_k and Sn_k are successively connected to either *vrefp* or *vrefn* according to the comparison result of the previous step, *vdac_p* and *vdac_n* are again compared and the result is stored. After the last iteration, ten comparisons were performed, *vdac_p* and *vdac_n* converged to *vcm* and the ten bits are available at the output register.

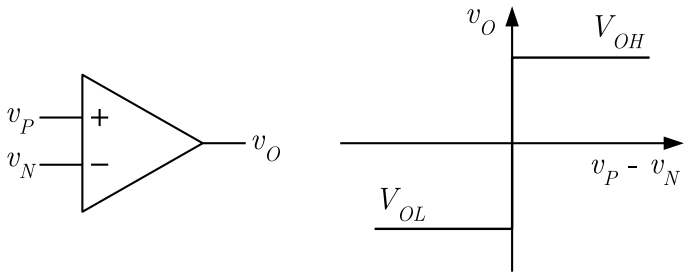
Note that, conversely to the conventional switching scheme, *up* and *down* transitions are symmetrical and does not require bottom plates to be disconnected and reconnected to the same reference voltage in *down* transitions. Moreover, due to the inherently top-plate sampling characteristic of MCS, the first iteration scheme needs no switching at all, meaning that a 10-bit ADC can use a 9-bit DAC, saving switching energy and area. Also, although the top-plate sampling can increase the charge injection and parasitic capacitances, only one pair of bootstrapped switches is required to provide a differential rail-to-rail input.

3.4. Comparators

The comparator is one of the most important circuits in converting analog signals to digital signals. This circuit is responsible for comparing two analog signals and

providing an output in the digital domain according the result. For presenting the analog-to-digital characteristic, the comparator can be considered as a 1-bit ADC. The symbol of the comparator is shown in Figure 3.19 alongside its transfer curve.

Figure 3.19 – Comparator symbol and transfer function.

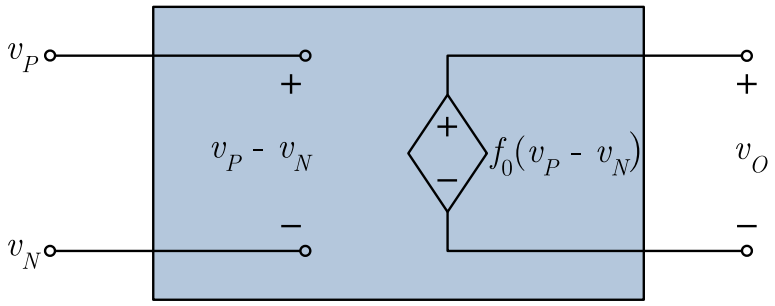


Source: Author, adapted from (ALLEN and HOLDBERG, 2002).

According its transfer curve, the output of the comparator is set to high logic level (V_{OH}) when the difference between v_P and v_N is positive or is set to low logic level (V_{OL}) otherwise. Note that this transfer curve presents a slope tending to infinity (infinity gain). As presented in (ALLEN and HOLDBERG, 2002), a plain model for the circuit is shown in Figure 3.20 with the mathematical behavior detailed in equation 3.33.

$$f_0(v_P - v_N) = \begin{cases} V_{OL}, & (v_P - v_N) < 0 \\ V_{OH}, & (v_P - v_N) \geq 0 \end{cases} \tag{3.33}$$

Figure 3.20 – A model for the ideal comparator.



Source: Author, adapted from (ALLEN and HOLDBERG, 2002).

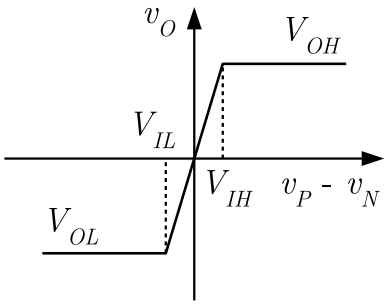
A more realistic first-order transfer curve for the comparator presents a non-perpendicular slope (limited gain). The new transfer curve is shown in Figure 3.21 and its mathematical behavior is described by equation 3.34,

$$f_1(v_P - v_N) \begin{cases} V_{OL}, \ (v_P - v_N) < 0 \\ A_V(v_P - v_N), \ V_{IL} < (v_P - v_N) < V_{IH}, \\ V_{OH}, \ (v_P - v_N) \geq 0 \end{cases} \tag{3.34}$$

where A_V is the open-loop gain, given by

$$A_V = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}}. \tag{3.35}$$

Figure 3.21 – The comparator transfer curve with finite gain.



Source: Author, adapted from (ALLEN and HOLDBERG, 2002).

The input change ($v_P - v_N$) needed to saturate the output is called the resolution of the comparator and must be adequate to meet the requirements of the following digital circuits in the system.

3.4.1 Dynamic characteristics

Comparators present some characteristics that could limit its operation in a system like an ADC. One of these characteristics is the propagation delay, which is the time between the comparator input excitation and its output transition (ALLEN and HOLDBERG, 2002). The propagation delay, in general, varies with the amplitude of the input signal.

Prior to entering in detail about propagation delay, it is necessary to analyze the frequency response of the circuit. Since a simple comparator is like an operational amplifier, a first order model for its frequency response is derived in (ALLEN and HOLDBERG, 2002) by considering the circuit is an amplifier with a single pole.

Therefore, the frequency response is given by

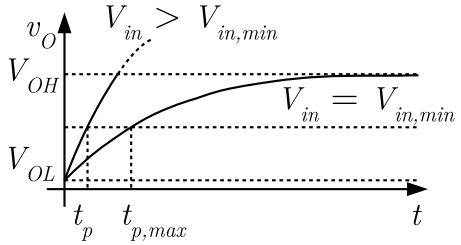
$$A_V(s) = \frac{A_V(0)}{\frac{s}{\omega_c}+1} = \frac{A_V(0)}{s\tau_c+1}, \tag{3.36}$$

where $A_V(s)$ is the transfer function in the s-plane, $A_V(0)$ is the DC gain and $\omega_c = 1/\tau_c$ is the pole position. Now, the resolution of the comparator can be estimated by calculating the minimum input voltage required to change its output from V_{OL} to V_{OH}, leading to

$$V_{in,min} = \frac{V_{OH} - V_{OL}}{A_V(0)}. \tag{3.37}$$

The previous equations aid us to draw the exponential time response of the comparator, shown in Figure 3.22. For a small input step V_{in}, the output response in time domain is a growing exponential according the transfer function in equation 3.36. If V_{in} is higher than $V_{in,min}$, the exponential growing curve saturates at V_{OH}.

Figure 3.22 – The small signal transient response for a step input in a comparator.



Source: Author, adapted from (ALLEN and HOLDBERG, 2002).

In Figure 3.22 it is also drawn a horizontal line at the midpoint of V_{OH} and V_{OL}. The time required for the output to cross this line, coming from V_{OL} (or from V_{OH}), is called propagation time (t_p). The maximum value of t_p, $t_{p,max}$, occurs when $V_{in} = V_{in,min}$. In this case, we can write

$$\frac{V_{OH} - V_{OL}}{2} = A_V(0)\left[1 - e^{\frac{-t_{p,max}}{\tau_c}}\right] V_{in,min}. \tag{3.38}$$

Resolving the above equation for $t_{p,max}$, the propagation delay of the comparator

is given by

$$t_{p,max} = \tau_c \ln 2 = 0.693\tau_c. \tag{3.39}$$

This expression can be generalized for input voltages of P times $V_{in,min}$:

$$t_p = \tau_c \ \ln(\tfrac{2P}{2P-1}). \tag{3.40}$$

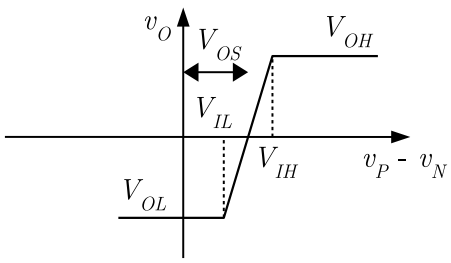
For a large-signal operation, the Slew-Rate (SR), due to the comparator capability of charging/discharging load and parasitic capacitors, will limit the propagation delay. In this case, t_p is given by

$$t_p = \tfrac{\Delta V}{SR} = \tfrac{V_{OH} - V_{OL}}{2 \cdot SR}. \tag{3.41}$$

3.4.2 Offset

The input-offset voltage (V_{OS}) is a non-ideal effect in comparators. It is seen as a transition point shift in the transfer curve of the comparator and is shown in Figure 3.23. In practice, we can model this effect by adding a voltage source in any port of the differential input (ALLEN and HOLDBERG, 2002), as shown in the model of Figure 3.24. Note that the voltage source value and polarity are unknown before the circuit fabrication because they are mostly caused by device mismatches.

Figure 3.23 – The comparator transfer curve, including the input-offset voltage.

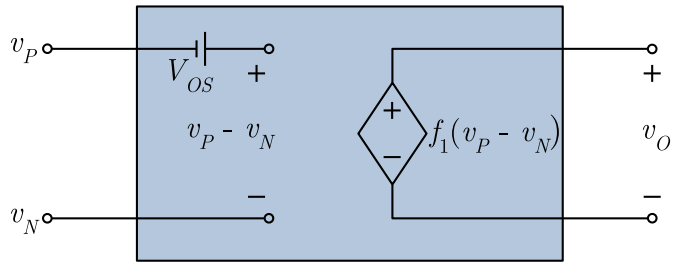


Source: Author, adapted from (ALLEN and HOLDBERG, 2002).

There are basically two sources of offset voltages. The first one is the mismatch between transistors that should present the same dimension and process parameters. We

can alleviate this problem by increasing the transistor dimensions and executing a meticulous floor planning for better devices matching.

Figure 3.24 – A model for the comparator, including the input-offset voltage.



Source: Author, adapted from (ALLEN and HOLDBERG, 2002).

The second source of offset voltage is the mismatch generated by parasitic capacitances. As stated in (ZHANG, 2012) and (NIKOOZADEH and MURMANN, 2006), even small parasitic wiring capacitances could lead to an offset of tens of millivolts. It can be reduced if connections from/to matched devices are drawn symmetrical, aiming to present similar parasitic elements.

3.4.3 The regenerative comparator

The regenerative comparator is a type of discrete-time circuit that makes use of positive feedback to perform the comparison of two input signals. It is also called a latch.

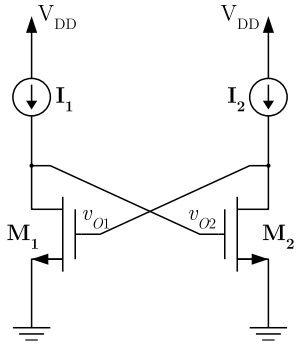
The positive feedback structure shown in Figure 3.25 is analyzed by (ALLEN and HOLDBERG, 2002). In this arrangement, the drain of M_2 (output of M_2) is connected to the gate of M_1 (input of M_1), and the drain of M_1 (output of M_1) is connected to the gate of M_2 (input of M_2).

This circuit presents two modes of operation. First, the feedback is disabled and nodes v_{O1} and v_{O2} receive the initial voltages V'_{O1} and V'_{O2}. Next, the feedback is restored, and the outputs will latch due to the positive feedback, according the relative values of V'_{O1} and V'_{O2}. Since we have an equivalent of two inverter circuits connected in anti-parallel, both outputs will lock at opposite logic levels.

To estimate the time the latch takes to properly lock its outputs to a defined logic

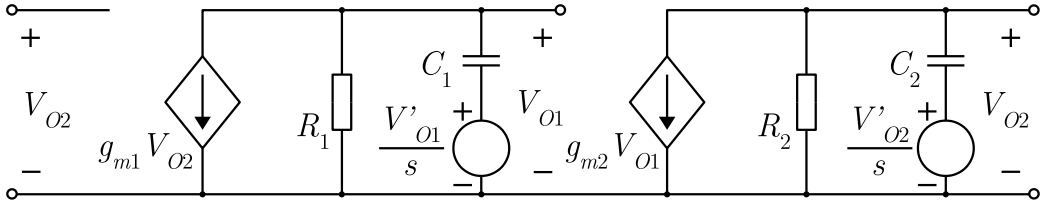
level, a nodal analysis is performed with the equivalent electrical circuit shown in Figure 3.26.

Figure 3.25 – A NMOS latch.



Source: Author, adapted from (ALLEN and HOLDBERG, 2002).

Figure 3.26 – An equivalent model for the NMOS latch.



Source: Author, adapted from (ALLEN and HOLDBERG, 2002).

We can write, respectively, the current sum at nodes v_{O1} and v_{O2} as:

$$\begin{cases} g_{m1}V_{O2} + G_1V_{O1} + sC_1\left(V_{O1} - \frac{V'_{O1}}{s}\right) = 0 \\ g_{m2}V_{O1} + G_2V_{O2} + sC_2\left(V_{O2} - \frac{V'_{O2}}{s}\right) = 0 \end{cases}, \tag{3.42}$$

where G_1 and G_2 is the inverse of the resistances seen from the drains of M_1 and M_2 to ground, C_1 and C_2 are the capacitances seen from the drains of M_1 and M_2 to ground, and g_{m1} and g_{m2} are the transconductances of the transistors. Note that the voltage sources in Figure 3.26 are step functions and represent the initial values V'_{O1} and V'_{O2} of nodes v_{O1} and v_{O2}. This equation can be solved for V_{O1} and V_{O2} to have

$$\begin{cases} V_{O1} = \frac{\tau_1}{s\tau_1+1}V'_{O1} - \frac{g_{m1}R_1}{s\tau_1+1}V_{O2} \\ V_{O2} = \frac{\tau_2}{s\tau_2+1}V'_{O2} - \frac{g_{m2}R_2}{s\tau_2+1}V_{O1} \end{cases}, \tag{3.43}$$

where τ_i is equal to R_iC_i. Considering that both transistors are equal, further simplifications can be made ($\tau_1=\tau_2=\tau$, $V_{O2} - V_{O1}=\Delta V_O$ and $V'_{O2} - V'_{O1}=\Delta V_{in}$) to lead this equation to a single expression:

$$\Delta V_O = \frac{\tau\ \Delta V_{in}}{s\tau + (1-g_m R)} = \frac{\frac{\tau\ \Delta V_{in}}{1-g_m R}}{\frac{s\tau}{1-g_m} + 1} = \frac{\tau' \Delta V_{in}}{s\tau' + 1}, \tag{3.44}$$

where

$$\tau' = \frac{\tau}{1-g_m R}. \tag{3.45}$$

Now, the inverse Laplace transform can be taken to provide the voltage difference between both nodes in function of time as

$$\Delta v_o(t) = \Delta V_{in} e^{-t/\tau'} = \Delta V_{in} e^{-t(1-g_m R)/\tau} \approx e^{\frac{g_m R t}{\tau}}\ \Delta V_{in}. \tag{3.46}$$

Considering the gains of each stage (g_mR) is greater than one, the time constant of the latch (τ_L) is expressed as

$$\tau_L \approx \frac{\tau}{g_m R} = \frac{C}{g_m} \tag{3.47}$$

and, therefore,

$$\Delta V_{out}(t) \approx e^{t/\tau_L}\ \Delta V_{in}\ . \tag{3.48}$$

Since the propagation time delay of the latch, t_{pL}, is defined as the amount of time required to the voltage difference between both nodes to reach $(V_{OH} - V_{OL})/2$, we can find

$$t_{pL} \approx \tau_L \ln\left(\frac{V_{OH}-V_{OL}}{2\ \Delta V_i}\right). \tag{3.49}$$

As a conclusion, a successfully designed comparator must present a τ_L such that t_{pL} will be less than a given time budget for any comparison, where ΔV_{in} is higher than

a minimum target value.

3.4.4 Metastability

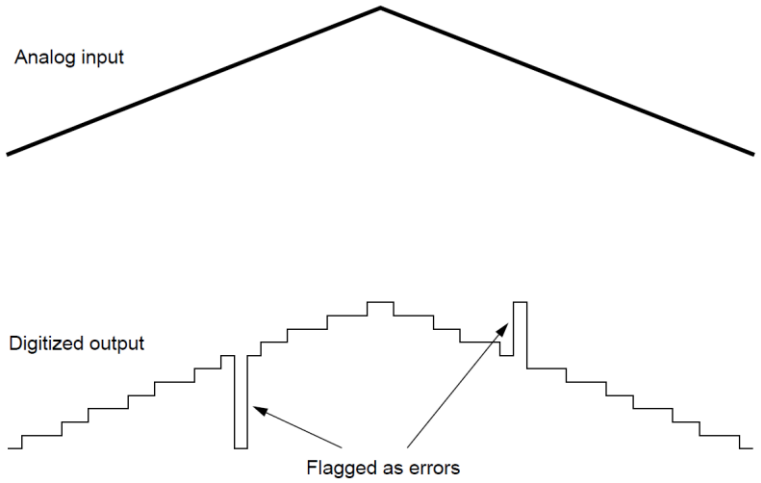
The analysis of sub-section 3.4.3 resulted in an expression that estimates the output settling time as a function of τ_L and ΔV_{in}, for constant V_{OH} and V_{OL}. It was inferred that designing a latch with a minimal τ_L would greatly reduce the time delay of the latch. However, regardless of τ_L, there will always some probability of ΔV_{in} being so small that t_{pL} will be higher than any given time budget, leading to the expiration of the comparison time. This problem is known in the literature as metastability.

The borderline value for ΔV_{in}, $\Delta V_{in,min}$, in which the comparison time will expire is derived by rearranging equation 3.48 with $t = t_{max}$, leading to

$$\Delta V_{i,min} \approx \frac{V_{OH} - V_{OL}}{2} e^{-t_{max}/\tau_L}. \tag{3.50}$$

The comparators employed in typical SAR ADCs suffer from this problem as well. As consequence, whenever a comparison time expires, the converted code is not guaranteed to be correct. Moreover, the erroneous value could be overly deviated from its correct value, as shown in Figure 3.27 .Therefore, if one estimates the probability of this event to happen, the CER of a SAR ADC due to metastability can be calculated.

Figure 3.27 – Typical metastability errors spotted in SAR ADCs.

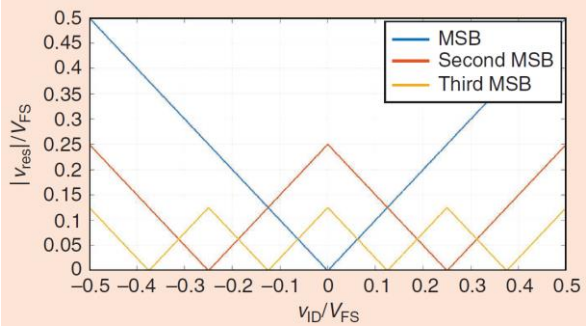


Source: (PORTMANN and MENG, 1995).

Take a 3-bit SAR ADC as an example. The analysis in (YU, BANKMAN, *et al.*, 2019) draws the residual voltage at the input of the comparator (in our case $|\Delta V_{in}|$) as a function of the ADC input voltage (both normalized to the full-scale voltage), shown in Figure 3.28.

It can be easily concluded that an N-bit SAR ADC will present $2^N - 1$ regions where the residual voltage is smaller than $|\Delta V_{i,min}|$, leading the conversion to a metastable state.

Figure 3.28 – A plot of the differential input voltage of the comparator as a function of the input voltage of a 3-bit SAR ADC, normalized to the full-scale voltage.



Source: (YU, BANKMAN, *et al.*, 2019).

Considering, for simplicity, the input voltage of the ADC presents a constant probability density throughout the entire full-scale range, V_{FS}, the CER due to metastability can be roughly estimated as

$$CER = P(|\Delta V_{in}| < |\Delta V_{in,min}|) = \frac{(2.\,|\Delta V_{in,min}|)}{V_{FS}/(2^N - 1)}\,, \tag{3.51}$$

leading to

$$CER \approx \frac{V_{OH} - V_{OL}}{V_{LSB}}\; e^{-t_{max}/\tau_L}. \tag{3.52}$$

4. The SAR ADC design

This chapter presents the design of the SAR ADC in the 65 nm Complementary Metal-Oxide-Semiconductor (CMOS) technology of Taiwan Semiconductor Manufacturing Company (TSMC). It describes the advanced techniques used in this work to implement each sub-circuit of the converter and makes use of the theoretical framework depicted in Chapter 3 as a guideline for sizing their devices. At the end of this chapter, the cares taken to draw the layout are also described, since the performance of the circuit is strongly related to a high quality and planned physical implementation.

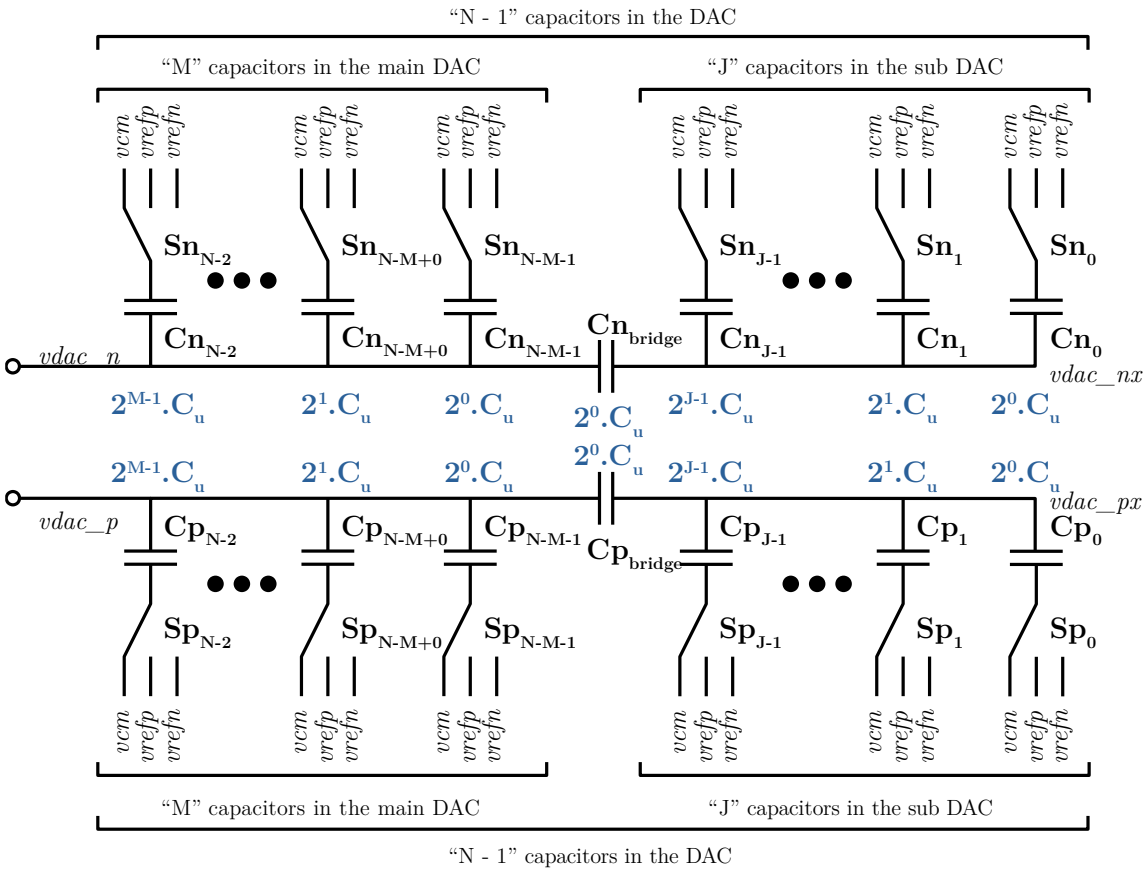
4.1. The capacitive DAC

The capacitive DAC of a SAR ADC is also the capacitor array responsible for tracking the input voltage during the sampling phase and for holding the input related charge throughout the conversion phase. Due to charge redistributions, different voltage values are set in the capacitor array and applied to the comparator.

The capacitive DAC structure employed in the design is shown in Figure 4.1. A pair of identical capacitor arrays were placed in $vdac\_p$ and $vdac\_n$ inputs (the p array and the n array). To improve the capacitor matching, capacitors of different sizes within the capacitor arrays were implemented by using multiple similar unit capacitors. The split binary-weighted capacitive array structure, introduced in sub-section 3.3.2, was applied in this design to reduce, considerably, the required number of unit capacitors in the DAC and, in consequence, to reduce the area and power consumption. In the structure, M binary-weighted capacitors were placed on the left side of a bridge capacitor and compose the called main DAC, and J binary-weighted capacitors are placed on the right

side of the bridge capacitor and compose the sub DAC. To further reduce power consumption and area, the MCS scheme (sub-section 3.3.3) was adopted. Although there are a variety of switching schemes that can achieve a higher efficiency, they all present common-mode variations to the comparator or additional digital circuitry.

Figure 4.1 – The capacitive DAC array.



Source: Author.

The split array structure is known to reduce the number of capacitors, but, as main drawback, the minimum value for C_u to attend the mismatch requirements is increased. It can be calculated by using equation 3.32 with convenient values for M and J. In this design, they were set to 5 and 4, respectively, because they led to the minimal number of unit capacitors needed to implement the array, improving the matching and connection routing between these devices. Using MIM capacitors for better matching coefficient, equation 3.32 resulted in a minimum C_u of 42 fF. This value also satisfies the

requirement of the RMS thermal noise (equation 3.20) being smaller than the quantization noise (equation 3.6) of an ideal 10-bit ADC (VAN DE PLASSCHE, 2003), *i.e.,*

$$32C_u \geq 12kT\frac{2^{2N}}{{V_{FS}}^2}, \tag{4.1}$$

where V_{FS} is the full-scale voltage.

In typical implementations of the split capacitive array structure, there is an additional unitary capacitor C_f in parallel with the last significative capacitor of the sub DAC. This capacitor C_f is permanently connected to *vcm*, and it is necessary to provide correct binary weighted steps. In this case, C_{bridge} should ideally present a capacitance of $(16/15)\cdot C_u$ (BAKER, 2010), when $J = 4$. Nonetheless, as shown in sub-section 3.3.2, it is a common practice to use $C_{bridge} = C_u$ for a better layout and matching, and, as a result, the ADC transfer curve will present several output codes with higher expected length.

In the implementation of Figure 4.1, the capacitor C_f is not present. In this case, the bridge capacitor should present a value close to $(1.0669)\cdot C_u$. When the bridge capacitor is implemented as a unitary capacitor, a common practice as mentioned, a −1.0 LSB offset and a tolerably small gain error are introduced in the DAC transfer curve (ZHANG, 2012).

In addition to the errors caused by the bridge capacitor value, parasitic capacitances between nodes *vdac_n*, *vdac_p*, *vdac_nx*, and *vdac_px* and V_{DD} or ground will introduce an additional offset and gain errors. If the parasitic capacitances in the nodes *vdac_n*/*vdac_p* are C_p and in the nodes *vdac_nx*/*vdac_px* are C_{px}, the offset error is around $(16C_p + C_{px})/C_u$. Note that errors caused by the parasitic in the nodes *vdac_n*/*vdac_p* are by far the most important.

Since the offset errors due to the parasitic capacitors are probably higher than 1.0 LSB and the DAC implementation without C_f and with $C_{bridge} = C_u$ causes only offset and small gain errors, but not alteration in the code length of the transfer curve, such implementation was chosen for application in the ADC.

4.2. The sampling circuit

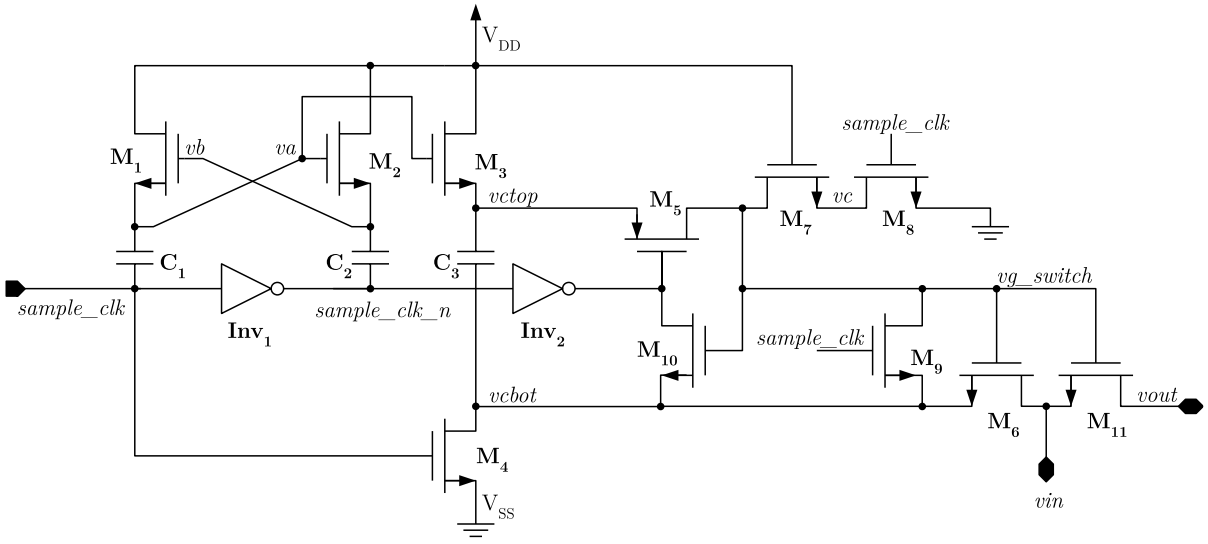
Typical sample and hold circuits make use of a hold capacitor and a switch. The hold capacitor, described and sized in section 4.1, is the total capacitance of the capacitive DAC whereas the switch, depicted in this section, can be as simple as a single MOS transistor. However, to provide a low distortion differential sampling, a pair of low distortion switches was considered in this design, which should present a voltage error aimed to be less than a quarter of the ADC quantization error. Therefore, a switch designed for a 10-bit ADC should present, at least, 12 bits of effective resolution.

The conventional bootstrapped switch, as stated in sub-section 3.2.2, can provide such resolution due to its linear output characteristic for a full range input signal. Figure 4.2 shows the implementation of the switch. In this circuit, transistors M_1 and M_2 and capacitors C_1 and C_2 constitute a voltage doubler necessary to the operations of transistor M_3. So, when *sample_clk* is set to high logic level, *va* is clamped to approximately $2\,V_{DD}$, both transistors M_3 and M_4 are turned on, and C_3 is charged with V_{DD}. At the same time, node *vg_switch* is connected to V_{SS} through transistor M_8, switching off the transistor M_{11}. When *sample_clk* is set to low logic level, *va* is clamped to approximately V_{DD} and both M_3 and M_4 are turned off. Now, node *vg_switch* is connected to the top plate of C_3 through transistor M_5, node *vin* is connected to the bottom plate of C_3 through transistor M_6. In this moment, the gate-source voltage of M_{11} is V_{DD} and, in consequence, M_{11} is on (switch on). In this circuit, transistors M_9 and M_{10} are responsible for turning on/off M_6 and M_5, respectively, according to the above-mentioned operation. Transistor M_7 is added to reduce the drain to source voltage experienced by M_8.

The transistor M_{11} dimensions were carefully determined. The choosing of L_{11} is straightforward because both switch-induced errors (sub-section 3.2.1) and bandwidth limitations (sub-section 3.2.4) are proportional to the length of the switch. In this design, it was set to the minimum possible value $L_{min} = 60$ nm. Conversely, for W_{11}, the switch-

induced error limits its maximum value, and the bandwidth, on the other hand, limits its minimum value.

Figure 4.2 – The bootstrapped switch schematic.



Source: Author, adapted from (ABO and GRAY, 1999).

The switch-induced errors are dominated by clock feedthrough and charge injection. As evaluated in sub-section 3.2.1, clock feedthrough is not the major concern because the circuit is differential. Charge injection, however, is expected to not evenly contribute to each switch sampling error and it should be minimized.

The highest voltage error contribution into the capacitive DAC of a differential ADC, due to charge injection, is observed when a switch is sampling a signal close to V_{DD} and its counterpart is sampling a signal close to zero. In that case, equation 3.13 states that both switches will induce different errors because the threshold voltage of a MOS transistor is a function of its body biasing. Therefore, considering the magnitude of the differential error should not be greater than $V_{LSB} = V_{FS}/2^N$ for a differential circuit, the maximum allowed W_{11} is limited by

$$\left|\Delta V_p' - \Delta V_n'\right|_{max} = \frac{C_{ox} W_{11} L_{11} (V_{TH}(VDD) - V_{TH}(0))}{2C_{hld}} \leq \frac{V_{FS}}{2^N}, \tag{4.2}$$

where $\Delta V_p'$ and $\Delta V_n'$ are the voltage errors due to charge injection of the two switches.

On the other hand, the minimum allowed W_{11} is estimated in view of the necessary input bandwidth. Considering the switch and the hold capacitor act as a low pass RC filter, the minimum W_{11} is derived by calculating the maximum allowed switch resistance, described in equation 3.16, for charging the hold capacitor within half the sampling period, according equation 3.23 (50% duty cycle sampling clock). Therefore, the minimum W_{11} is constrained by

$$\frac{1}{2^{N+1}} \leq e^{\frac{-T_S\left(\mu_n C_{ox}\frac{W_{11}}{L_{11}}V_{eff}\right)}{2.C_{hld}}}. \tag{4.3}$$

The transistors M_5-M_{10} are small and were sized according to the required strength to drive the gate of M_5, M_6, M_{10}, and M_{11} within a short period. They were implemented with $L = L_{min}$, $W = 440$ nm, and one finger, with exception to M_5 and M_9. Transistor M_5 is a p-type MOS (PMOS) and presents double the width of the NMOS transistors, and transistor M_9 needs an increased number of fingers because it must deal with the high parasitic capacitance of node *vg_switch*.

Some transistors could be implemented with $W < 440$ nm, but, for this technological node, their layout would present only 1 contact at the source and 1 contact at the drain. Setting $W = 440$ nm allows the placement of 2 contacts per terminal, increasing the manufacturing reliability.

The remaining transistors M_1-M_4 and both inverter logic gates were sized after the choosing of C_1, C_2 and C_3 because they must deal with charging/discharging of these devices within half the sampling period. To minimize errors, C_3 minimum value must be relatively larger than the parasitic capacitances added by the transistors connected to their terminals when *sample_clk* is set to low logic level. In this case, the voltage drop in C_3, due to the charge redistribution in those transistors, is not significant. The device dimensions are shown in Appendix Table A.4 and Appendix Table A.5.

In the switch, special attention must be paid at low frequency operation because the charge in the hold capacitor, as the electric potential difference between its terminals,

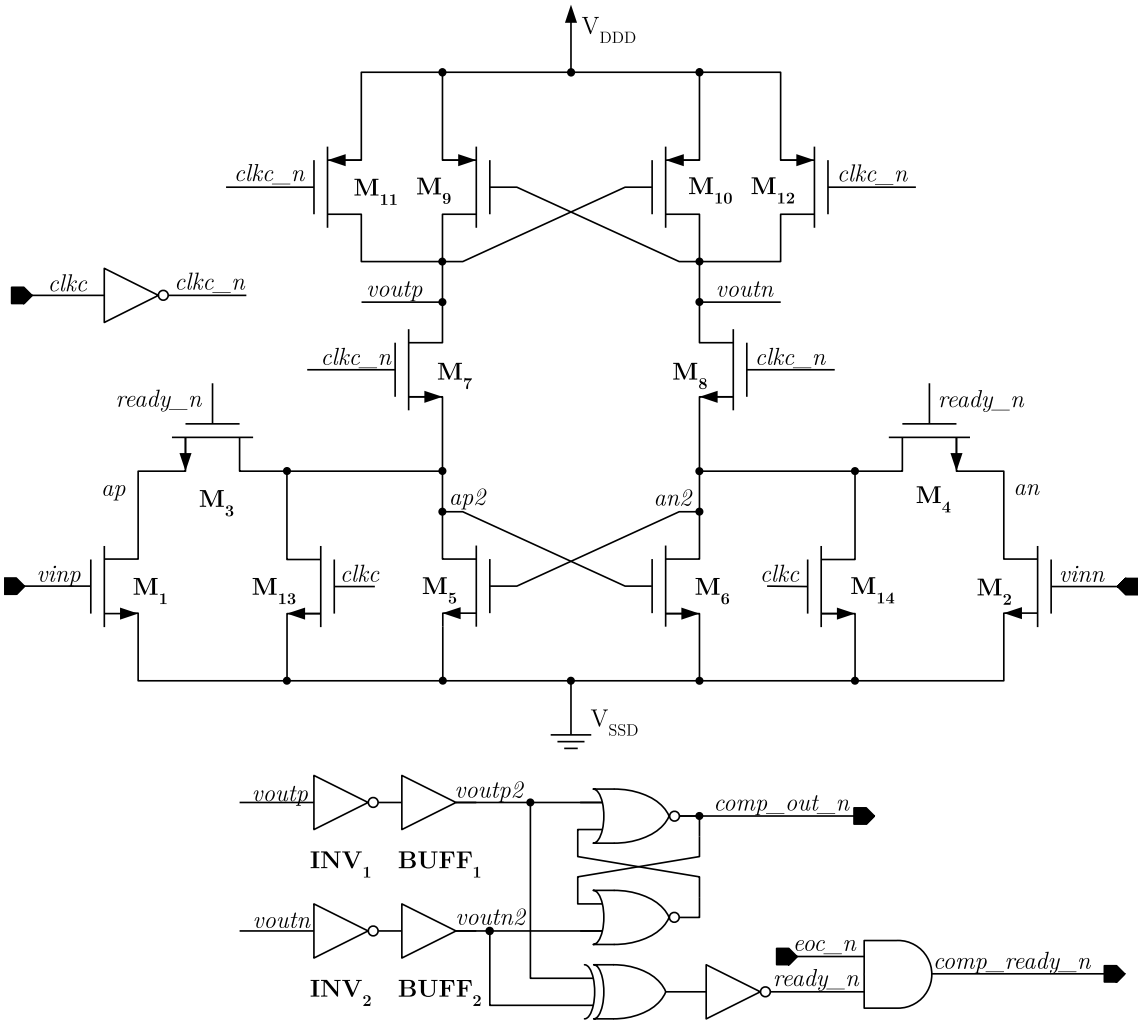
must be kept constant after the sampling phase. However, due to parasitic elements, the switch presents charge leakage throughout the conversion phase, reducing the voltage at the hold capacitor. In the asynchronous ADC implementation, this problem is alleviated because the SAR operation, after triggered, presents a short conversion time, limited only by asynchronous switching devices (HARPE, ZHOU, *et al.*, 2010). Nonetheless, in both implementations, charge leakages observed in C_1, C_2 and C_3 also leads to resolution degradation at low frequency operation. The leakage from C_1 and C_2 reduces the potential at *va*, compromising the charging of C_3 to V_{DD}, whereas the leakage from C_3 reduces V_{GS11}, compromising R_{ON} and, as consequence, the track bandwidth.

4.3. The dynamic comparator

The comparator circuit design plays an important role in the system performance. Although this circuit must present a fast operation, it can be inferred from (CHEN and BRODERSEN, 2006) that the asynchronous implementation relaxes the required speed of a comparator designed for a 10-bit SAR ADC by approximately 36%, in the worst case.

To fulfill the time constraints, a fast response comparator topology with low kick-back noise was considered (HUANG, SCHLEIFER and KILLAT, 2013) and is shown in Figure 4.3. In this circuit, the comparator is composed by transistors M_1 up to M_{14}. The logic gates connected at *voutp* and *voutn* are the output logic circuit and are responsible for delivering the comparison result (*comp_out_n*) and the indication flag (*comp_ready_n*) to other circuits.

Figure 4.3 – The low kickback noise comparator.



Source: Author, adapted from (HUANG, SCHLEIFER and KILLAT, 2013).

The comparator works as follows: when *clkc* is set to high logic level (and *clk_n* to low), the circuit is at reset phase, which turns on the transistors M_{11}, M_{12}, M_{13} and M_{14} and turns off transistors M_7 and M_8, setting both output voltages, *voutp* and *voutn*, to V_{DD} and *ap2* and *an2* to V_{SS}. The *ready_n* signal is high and is fed back to switches M_3 and M_4, keeping them on during the reset phase. The *comp_ready_n* is a copy of *ready_n*, with exception that it is forced to low by *eoc_n* (the inverted version of the ADC end-of-conversion flag) when *ready_n* is locked at high due to a metastability event. This action is necessary for a proper resetting of the asynchronous logic, which depends on *comp_ready_n*, before the next conversion.

When *clkc* is set to low logic level (and the *clk_n* to high), the circuit triggers the regeneration phase. In this phase, transistors M_{11}, M_{12}, M_{13} and M_{14} are turned off, transistors M_7 and M_8 are turned on and the output voltages will fall from V_{DD} according to the current drained by the differential pair M_1 and M_2, which depends on the differential input voltage (*vinp* – *vinn*). The cross-coupled transistor pairs M_5/M_6 and M_9/M_{10} further amplify the differential input, increasing the difference among *voutp* and *voutn*.

As soon *voutp* and *voutn* present enough magnitude to trigger the output logic circuits, the *ready_n* signal opens the switches M_3 and M_4, decoupling M_1 and M_2 differential pair from the circuit. Once the drain terminals of the differential pair will not sense all the voltage swing driven by the cross-coupled pairs, this topology will reduce the M_1 and M_2 gate-drain voltage swing, therefore, reducing noise coupling between *ap2*/*an2* and *vinp*/*vinn* through the gate-drain capacitance C_{GD} of M_1 and M_2 (kickback noise). Finally, *comp_ready_n* is forced to low logic level by *ready_n*, meaning that *comp_out_n* holds the actual comparison result. If *vinp* > *vinn*, *comp_out_n* is set to low, otherwise, it is set to high.

Transistors M_{13} and M_{14} were added in a second version of the ADC. They are responsible for discharging parasitic capacitors of nodes *ap2* and *an2* in the reset phase, ensuring they will present the same voltage level at the beginning of the regeneration phase.

The $BUFF_1$ and $BUFF_2$ are buffers, composed by two inverters, and were added in the second version as well. Besides decreasing the coupling between *comp_out_n* and *voutp*/*voutn*, during the regeneration phase, they present a much lower capacitive load to INV_1 and INV_2. As a cascade effect, it permitted the reduction of the capacitive load in *voutp* and *voutn* by decreasing the size of INV_1 and INV_2.

The dimensions of the transistors were chosen considering the regeneration time constant of the dynamic comparator, τ_L. In this design, the ADC does not present a SAR clock and the sampling period itself is used half to do the input sampling and half to do

the conversion. During the conversion phase, the comparator should perform N decisions, as shown in Figure 2.7, where the available time is allocated to each comparison according to the greater or lesser difficulty in carrying it out. In consequence, more time can be employed in the harder comparisons, relaxing the requirements for the maximum value of τ_L. With that in mind, (YU, BANKMAN, *et al.*, 2019) expands equation 3.52 to find the probability of a metastability event occurring in the conversion of a sample, P_{meta}, and concludes that this feature reduces the CER due to the exponential reduction of P_{meta}, when compared with its synchronous counterpart of same resolution. For the asynchronous SAR ADC, P_{meta} is as a function of τ_L and is given by

$$P_{meta} = 2^{N+1} e^{-(T_S - t_{track} - T_{FIX,TOT} - T_{easy})/\tau_L}, \tag{4.4}$$

where T_S is the sampling clock period, t_{track} is the sampling phase, $T_{FIX,TOT}$ is the sum of all fixed delays for DAC settling and comparator reset, T_{easy} is the sum of all regeneration times, excluding the hardest one ($t_{reg,hard}$). Note that T_{easy} also depends on τ_L and its value is approximately

$$T_{easy} = \tau_L \sum_{i \in \{N-1 \ softest \ comparisons\}} \ln\left(\frac{V_{DD}}{2|\Delta V_{in,i}|}\right), \tag{4.5}$$

where $\Delta V_{in,i} = vinp_i - vinn_i$ is the input voltage of the comparator in the i-th iteration.

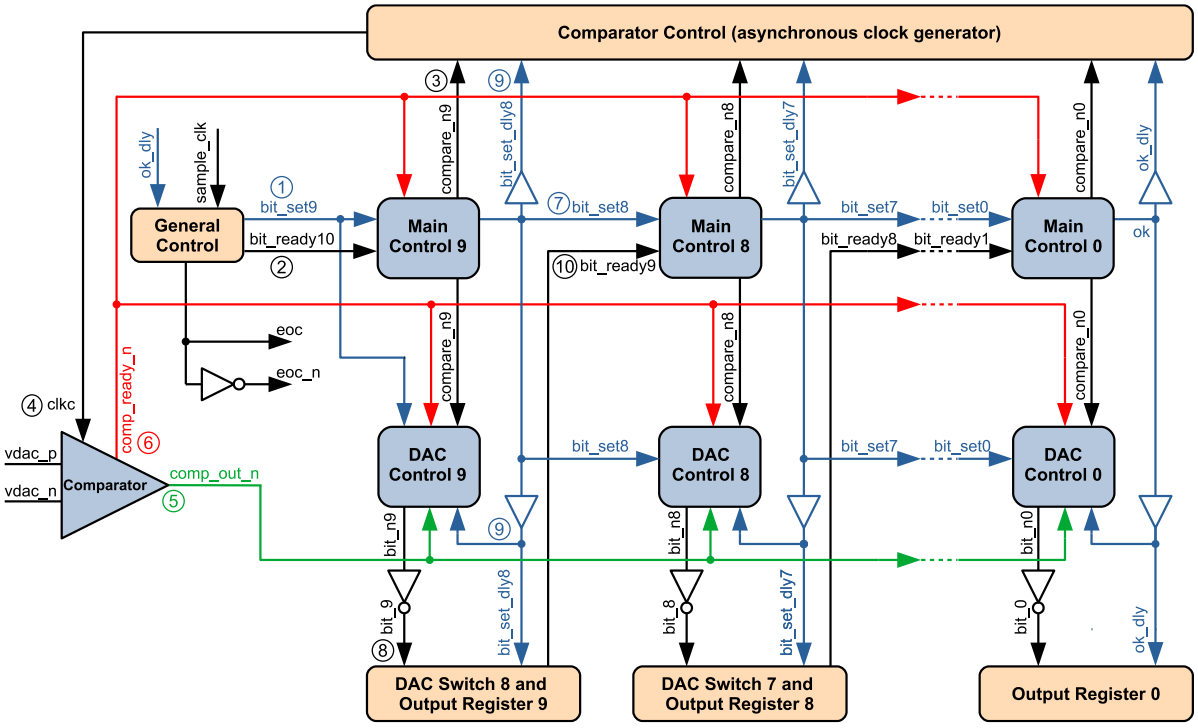
At first analysis, the mismatches, and the offset caused by them, would not be a critical concern, since offset will slightly influence the ADC linearity when the common-mode voltage at the input of the comparator is kept constant (LIU, CHANG, *et al.*, 2010). However, the offset could decrease the SNR by reducing the input voltage swing (ZHANG, 2012). Therefore, the differential pair transistors had their width increased, being their size limited by the kickback noise problem. The remaining transistors were made small to avoid increasing parasitic capacitances and power consumption. The device dimensions are shown in Appendix Table A.6.

4.4. The asynchronous SAR logic

The SAR logic circuit is responsible for providing the switching sequence for the DAC circuit (Figure 4.1). In this work, the custom combinational asynchronous SAR circuit described in (HARPE, ZHOU, *et al.*, 2010) was employed along the MCS scheme (HARIPRASATH, GUERBER, *et al.*, 2010). These topologies allow a "manual" device placement, present a reduced power consumption, and make use of only one clock source.

In this sub-section, Figure 4.4 presents the SAR logic circuit block diagram, and Figure 4.5, Figure 4.6, and Figure 4.7 present, respectively, the implementation of the Main Control, DAC Control and Comparator Control circuits.

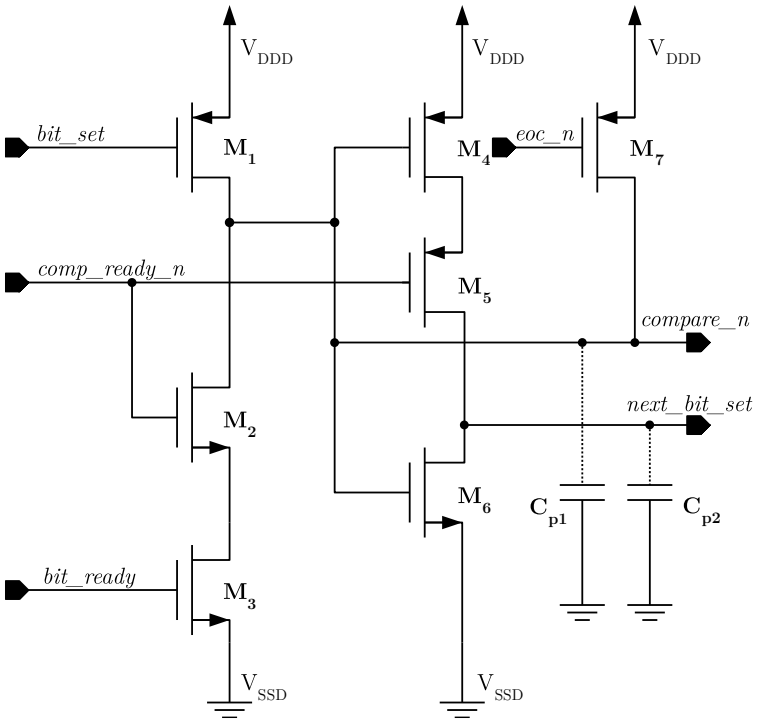
Figure 4.4 – The SAR logic block diagram. Some signals are omitted for simplicity.



Source: Author, adapted from (HARPE, ZHOU, *et al.*, 2010).

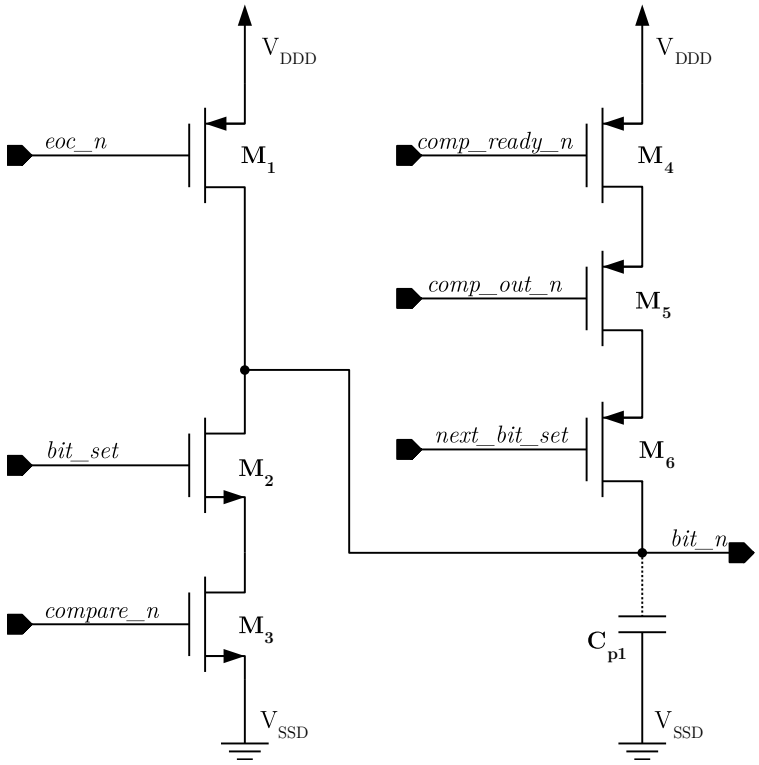
During the sampling phase of the ADC, the *sample_clk* signal has low logic level and no activity is observed in the SAR logic circuit. When the *sample_clk* signal has high logic level, the SAR logic circuit is triggered by the negated end-of-conversion flag (*eoc_n*) and, from now on, N successive switching procedures will take place.

Figure 4.5 – One Main Control circuit, for each bit.



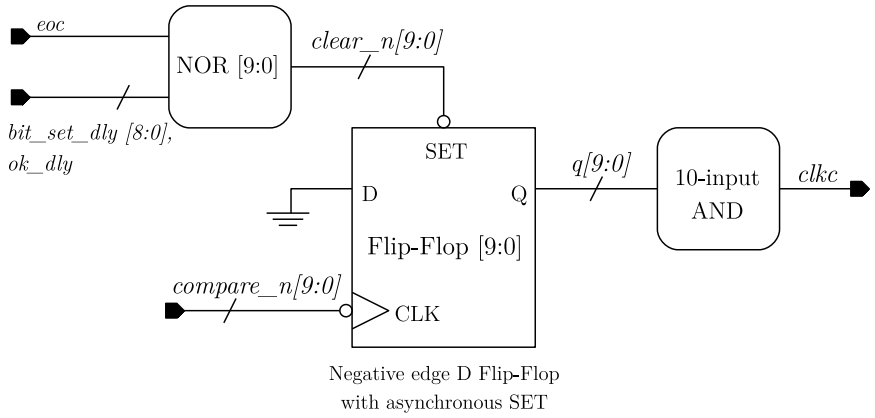
Source: Author, adapted from (HARPE, ZHOU, *et al.*, 2010).

Figure 4.6 – One DAC Control circuit, for each bit.



Source: Author, adapted from (HARPE, ZHOU, *et al.*, 2010).

Figure 4.7 – The Comparator Control circuit.



Source: Author.

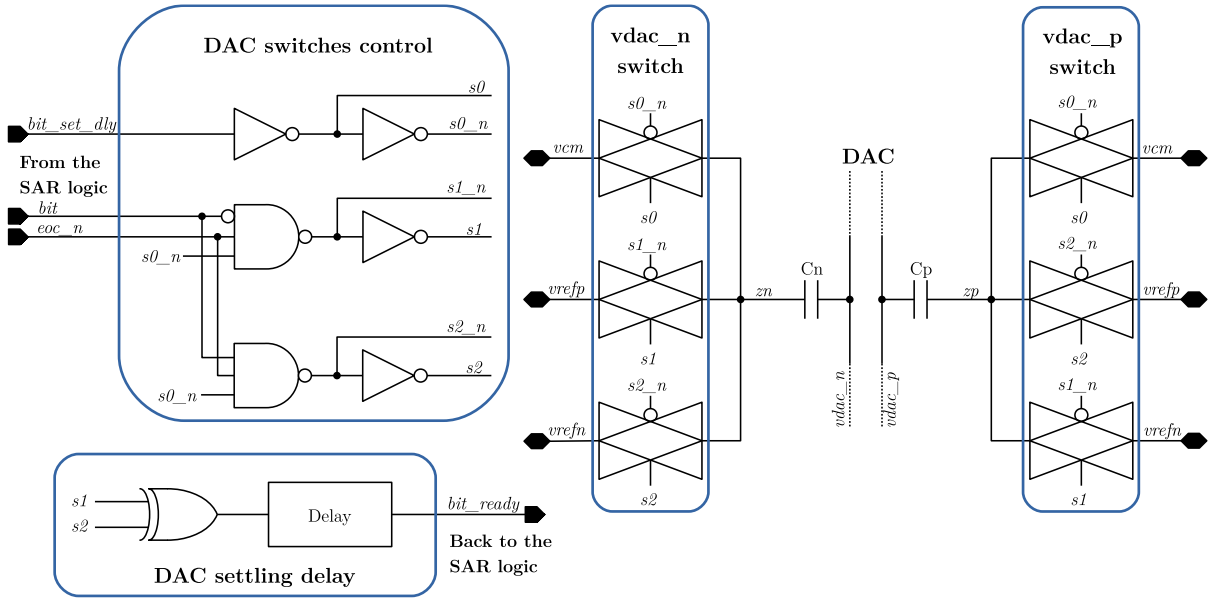
In the first iteration, the General Control presets the Main Control 9 (1), *bit_set9* = "1", and waits for the input signals of the comparator to settle, after the opening of the bootstrapped switches. Once the signals are settled (2), *bit_ready10* = "1", the Main Control 9 requests a comparison (3) to the Comparator Control, *compare_n9* = "0", which, in turn, sets the dynamic latch comparator to the regeneration phase (4), *clkc* = "0".

When the result is available in the output of the comparator (5), the Main Control 9 and DAC Control 9 blocks are signalized (6) with *comp_ready_n* = "0". After the comparison, *bit_set8* rises (7) to preset the Main Control 8 and DAC Control 8. Also a delayed and buffered version of *bit_set8*, *bit_set_dly8* (9), is used to lock the DAC Control 9 (*next_bit_set*) after the settling of *bit9*, to reset the Comparator Control and to trigger the DAC Switch 8 and Output Register 9. Now, *bit9* (8) holds the actual 10^{th} bit of the converted signal, which will be used by the Output Register 9 and DAC Switch 8 circuits. This circuit will determine, according to the value of *bit9*, to which reference voltage the bottom plate of the MSB capacitors of the capacitive array should be switched. Finally, after a fixed delay, the *bit_ready9* is set to high (10), and the Main Control 8 will initialize the next iteration. The Main Control 8 and the DAC Control 8 will repeat the operations done by the DAC Control 9 and the Main Control 9 and will obtain the 9^{th} bit. The sequence of iterations will continue until all bits are obtained.

Once the conversion is completed, the *ok_dly* signal is fed back to the General Control, the *eoc* flag will rise and all the circuits of the SAR logic Block will be reset. It should be mentioned that the *bit_n0* holds the first bit of the converted signal and does not trigger any switching in the DAC.

As commented in sub-section 3.3.3, and illustrated in Figure 4.1, all the DAC switches must short the bottom plates of all capacitors to *vcm* during the ADC sampling phase. After that, during the ADC conversion phase, according to the comparison result in each iteration, the DAC Switch $k-1$ must switch $Cp_{k\text{-}1}$ and $Cn_{k\text{-}1}$, respectively, to either *vrefn* and *vrefp* or *vrefp* and *vrefn*, where $k-1$ ranges from eight down to zero. To do so, the custom DAC Switch circuit of Figure 4.8 was proposed to properly perform the three-level voltage switching.

Figure 4.8 – One DAC Switch circuit, for each bit, with exception for the LSB one.



Source: Author.

Each DAC Switch has three input signals, *bit*, *bit_set_dly*, and *eoc_n*, and one output signal, *bit_ready*, which is responsible for signalizing the asynchronous circuit that the DAC has settled. The DAC Switch also generates six internal signals, *s0*, *s0_n*, *s1*, *s1_n*, *s2*, *s2_n*, which control the capacitive array switches.

The *bit* input signal of the DAC Switch $k-1$ is provided by inverting the *bit_n*

output of the DAC Control *k*. This was accomplished by inverter logic gates, which also provide buffering and protection to the high impedance *bit_n* nodes from the noise coupled in the long interconnections going from the DAC Control to the DAC Switches and Output Registers. At the beginning of the comparison phase, the *bit_set_dly* state is "0" and only the switches connecting to *vcm* are closed. When the comparison is ready, the Main Control *k* set the *bit_set_dly* of the DAC Switch $k-1$ to high, which will open the *vcm* switches. Now, the two NAND gates will prepare the signals controlling the other switches, according to the value of *bit*, coming from the DAC Control *k*. The utilization of the delayed version of *next_bit_set*, *bit_set_dly*, will provide a longer time for the preparation of the node *bit* and ensure that this signal is stable when *s0_n* is set to high. This will avoid glitches in the NAND gates. The signal *bit_ready*, sent to the Main Control $k-1$, is set to high after the charge redistribution is completed.

4.5. Supply and reference voltages

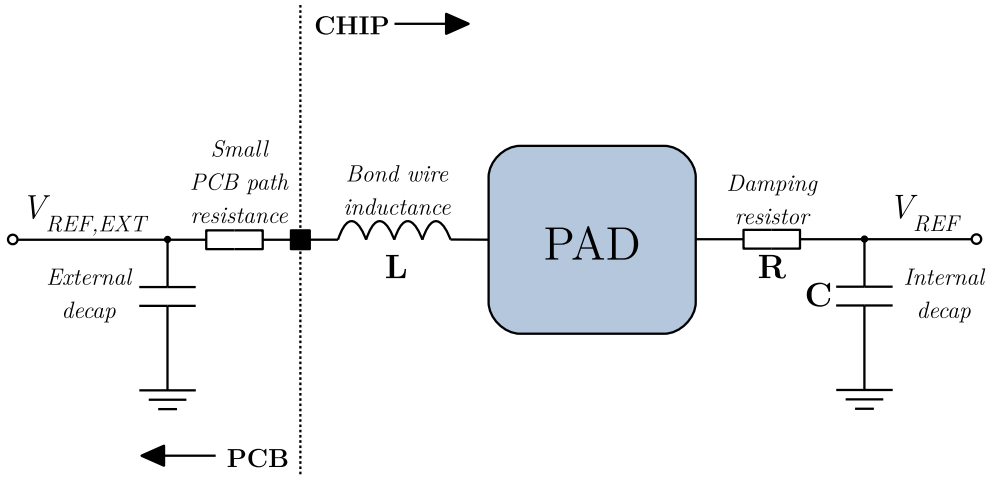
It is known that switching based circuits suffer from supply and reference voltage variations due to large electrical currents demand within short time periods. This is caused by the presence of parasitic elements, particularly the resistors and inductors, in the path from any reference voltage source to the actual circuit. If one considers external voltage sources, the voltage variations are worsened by the presence of bond wires and their parasitic inductances. An equivalent electrical circuit for the path from an external reference voltage, $V_{REF,EXT}$, to an internal reference voltage, V_{REF}, is shown in Figure 4.9.

Considering the voltage at the PCB side is well damped by high quality decoupling capacitors (from nF scale) with low Equivalent Series Resistance (ESR), and by a small path resistance between the decoupling capacitors and the chip interface, the voltage settling analysis can be limited to the internal nodes.

The internal nodes (chip side) of reference voltage paths are composed, at first analysis, of the bond wire, the pad and chip parasitic elements. To lessen the voltage

ringing, damping resistors, and decoupling capacitors (*decaps*) are often added close to the internal reference node. Equation 4.6, obtained from mesh analysis and the derivative of the result, can be used to estimate the R and C values for a desired damping factor in the series RLC circuit at the chip side.

Figure 4.9 – A model for voltage settling analysis of reference voltage sources.



Source: Author.

$$\frac{d^2}{dt}i(t) + \frac{R}{L}\frac{d}{dt}i(t) + \frac{1}{LC}i(t) = 0 \tag{4.6}$$

Equation 4.6 is a second order differential equation and can be rewritten as a characteristic equation in function of the damping ratio ζ. For a desired damping ratio, we can choose R and C according equation 4.7.

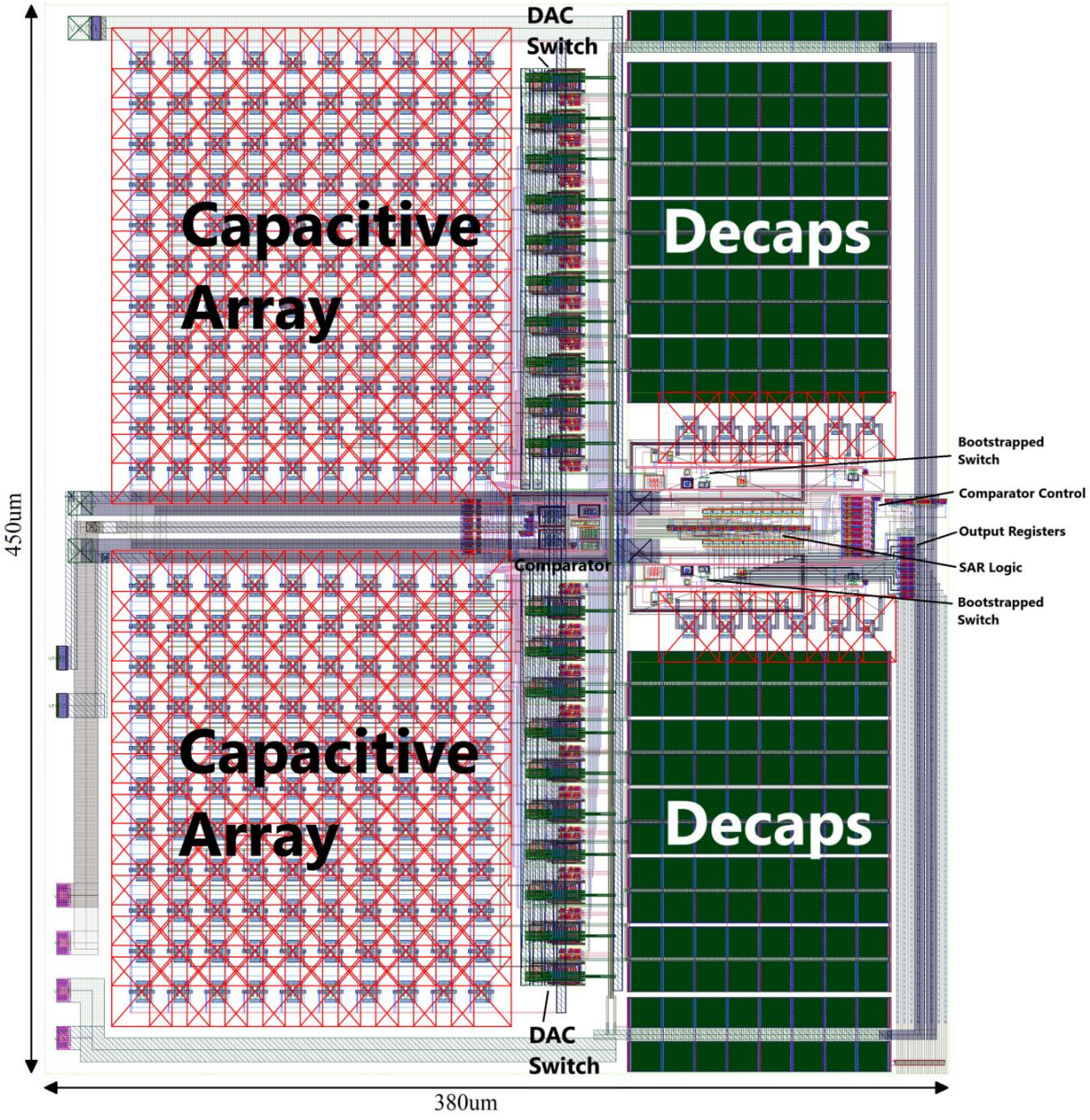
$$\frac{R^2}{4}\frac{C}{L} = \zeta^2 \tag{4.7}$$

The bond wire inductance, as a rule of thumb, is estimated to be 1 nH/mm. So, for damping ratio of 1, the parameters of equation 4.7 were set to $L = 5$ nH and $R = 5$ Ω, leading to a calculated damping capacitance of 800 pF for each reference voltage. Since this capacitance value requires a large area, the capacitors had their sizes reduced. In fact, they were the last devices to be implemented since they can take use of the remaining unused circuit area.

4.6. Layout

The layout of integrated circuits usually has its analog circuitry placed as far as possible from its digital circuitry and presents dedicated supply voltages for each domain, to reduce the noise coupled into sensitive areas. The first version of the ADC was layout in 65 nm CMOS technology following these guidelines and is shown in Figure 4.10.

Figure 4.10 – Layout of the first version.

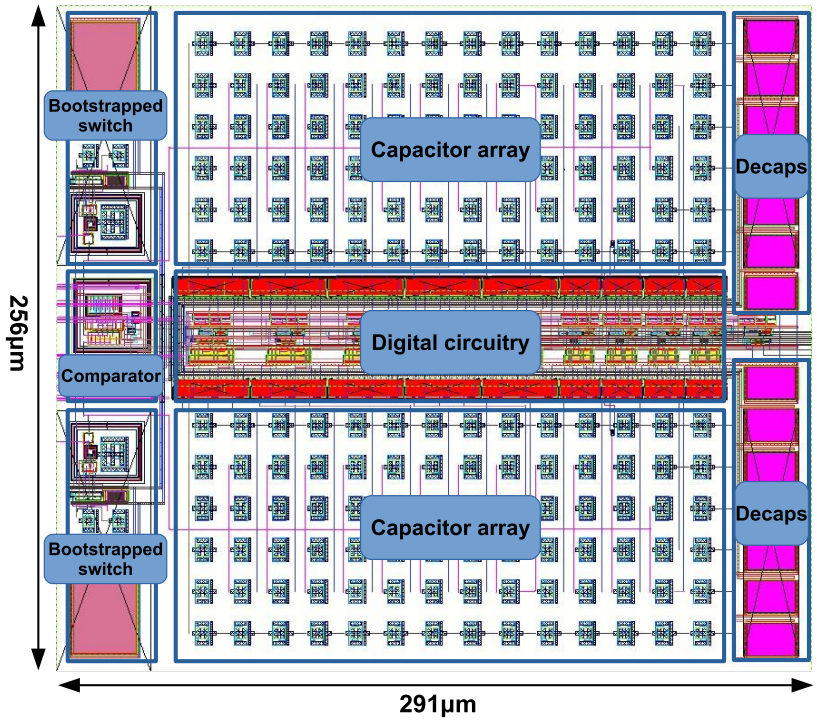


Source: Author.

The first layout drawing provided a netlist of the ADC, including parasitic elements. Then, post-layout simulations were carried out to analyze the performance of the circuit. The ADC performance had shown to be degraded mainly due to bad placement/routing and improper sizing of the switches for charge redistribution, as will be discussed in chapter 5. As a result, a second version of the converter was designed and drawn to layout, with a better placement, routing, and devices sizing. It is shown in Figure 4.11.

In the second version of the layout, the bootstrapped switches and the comparator were placed at the leftmost side of the chip to reduce the routing length of the sensitive wires *vinp*, *vinn*, *vdac_p* and *vdac_n*.

Figure 4.11 – Layout of the second version.



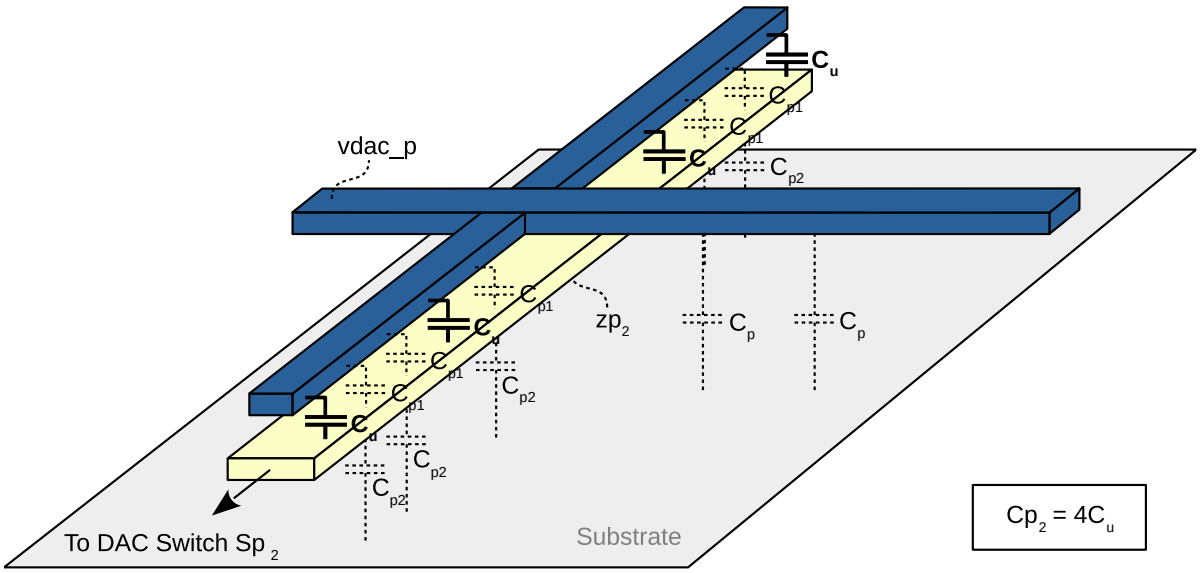
Source: Author.

As discussed in section 4.1, the reduction of the parasitic capacitances of wires *vdac_p* and *vdac_n* to the substrate, C_p, are critical for decreasing the ADC gain error. Therefore, for the new layout version, these nodes had their widths decreased (0.1 µm) and were reallocated to a higher metal level (*metal 7*). Additionally, the interconnections

routing of the bottom plates of all capacitors in the DAC (Figure 4.1) were drawn, whenever was possible, immediately below their top plates. It means that, in some regions, the bottom of *vdac_p* and *vdac_n* metal traces see a series association of the parasitic capacitances between the top and the bottom plates of the unitary capacitors, C_{p1}, and between the bottom plates of the unitary capacitors and the substrate, C_{p2}. As consequence, at cost of slightly increasing the overall hold capacitance of the DAC, C_{hld}, the *vdac_p* and *vdac_n* nodes are "shielded" from the substrate, reducing C_p. This technique is shown in Figure 4.12. For simplicity, it is only illustrated for the *vdac_p* node, the Sp_2 switch, and Cp_2 capacitor (composed by four unitary capacitors, C_u).

In order to keep the power supply and reference nodes as steady as possible, as shown in section 4.5, *decaps* were added to these nodes, at the rightmost side of the chip.

Figure 4.12 – The top plate shielding in the capacitive DAC interconnections.



Source: Author.

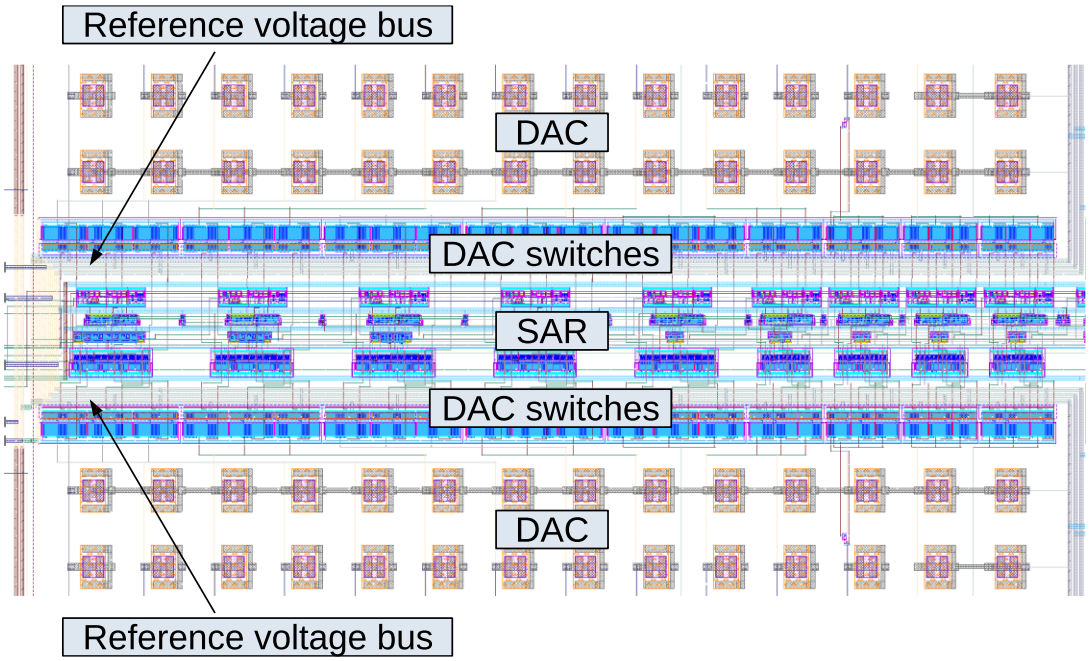
The symmetry in the layout of a differential ADC can affect the system linearity. So, all circuits implemented in pairs, like the bootstrapped switches, capacitive arrays, DAC switches and *decaps*, were symmetrically placed along a horizontal axis. Although the comparator presents itself as a single circuit, any asymmetry in its implementation directly affects its offset voltage. Therefore, a meticulous layout drawing was performed

for it. The layout of all designed circuits are shown in Appendix B.

To greatly reduce the congestion due to digital signals routing, the digital circuitry was placed along the horizontal axis in sequential bit order. Following this alignment, a row of DAC switches was placed near each capacitor array, allowing the creation of a pair of reference voltage buses from the *decaps* throughout the DAC switches, as shown in Figure 4.13.

Additionally, for each bit, some delay cells were used to ensure proper delay is given between the charge redistribution, due to DAC switching, and the comparator triggering. For the least significant bits, however, delay cells were not necessary because the delay of the logic circuits is enough to ensure the small amount of charge is redistributed before the next comparison.

Figure 4.13 – Layout of the second version, zoomed at the digital circuitry and reference voltages.



Source: Author.

Finally, to further isolate sensitive circuitries, some transistors were implemented within a deep N-Well guard ring. This careful procedure is applied to the transistors of the bootstrapped switch, except for those related to its voltage doubler circuit, and to the transistors of the comparator circuit.

5. Results

In this chapter, simulation results regarding power consumption and effective resolution of the designed ADC are shown and discussed. Although the post-layout simulation results validated the system level operation, some characteristics of its sub-circuits indicated the need for modifications to increase their reliability and performance. In that sense, a second version of the converter was designed, drawn to layout, and simulated. The simulation results of the second version is shown and discussed as well.

5.1. The first version

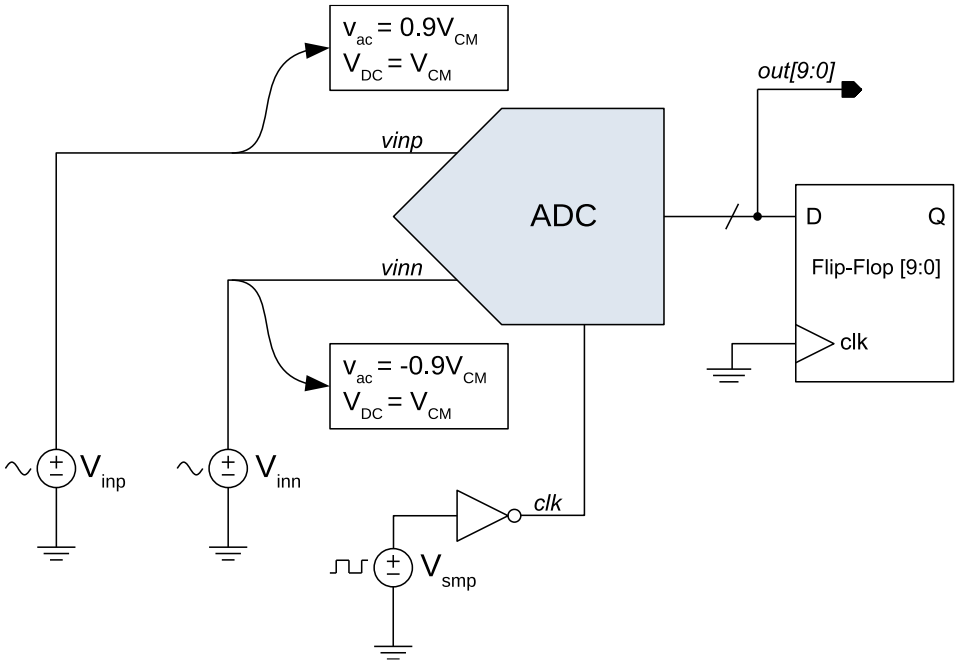
The simulation results regarding the first implementation of the ADC are presented in this section. The simulations make use of the post-layout netlist, containing parasitic resistances and capacitances extracted by the Calibre PEX tool from the layout view.

The behavior of the ADC and its sub-circuits, alongside the obtained values of their dynamic and static parameters, were fundamental for deciding whether there are blocks which should be redesigned or not.

5.1.1 Power consumption and ENOB

The test bench used for characterization of the ADC is shown in Figure 5.1. The netlist presents no element models for external bond wires or pad capacitances because the simulations are intended to analyze and understand the behavior and performance of the converter, isolated from system level circuits. Also, the digital output pins of the circuit were connected to external registers acting as simple loads.

Figure 5.1 – Test bench circuit for the ADC.



Source: Author.

For proper extraction of the ENOB and simulation of the ADC power consumption, a differential signal, with an appropriate frequency for coherent sampling, is applied into the input of the ADC. This is achieved by using two sinusoidal voltage sources as input signals (*vinp* and *vinn*) phased by 180º, with a frequency slightly lower than half the sampling rate, satisfying both Nyquist theorem and equation 3.24. To avoid saturation in the converted codes, the amplitude values of both input signals were set to 90% of the full scale, reducing the presence of distortion in the computed DFT and not significantly affecting the power consumption measurement. Although this amplitude reduction decreases the SINAD and, consequently, the ENOB, this effect is compensated by applying a correction factor, as shown in equation 3.9. Since the ADC only samples signals between zero and V_{DD}, the sinusoids must present a DC level of $V_{DD}/2$.

By using the test bench shown in Figure 5.1, with the abovementioned input signal characteristics, a transient simulation was run in typical corner at 27 ºC and V_{DD} = 1.2 V. For ENOB calculation, the circuit was set to convert 1027 samples. The Cadence ADE tool computed the DFT with only 1024 samples (points), since the first three

converted points were discarded. These three samples were taken when the system was not in permanent regime and present errors due to the transient. The results are summarized in Table 5.1.

As expected, and commented in section 2.4, the simulated power consumption of the circuit presented an almost linear dependency of the sampling frequency. By drawing the Figure 5.2, the coefficient (slope) "Power/Sampling rate" is observed to be roughly constant for sampling rates above 0.1 MS/s.

Figure 5.3 shows the current consuption from the voltage sources applied in the ADC. They are the digital power supply (*vddd*), the analog power supply (*vdda*), the positive reference power reference (*vrefp)*, the commom-mode power supply (*vcm*) and the input signals (*vinp* and *vinn*). The biggest contribution to the power consumption is given by the digital circuitry (current sinking from *vddd*) and by the capacitive DAC (current sinking from *vrefp*).

Table 5.1 – Simulated ADC dynamic parameters for different sampling frequencies (first version).

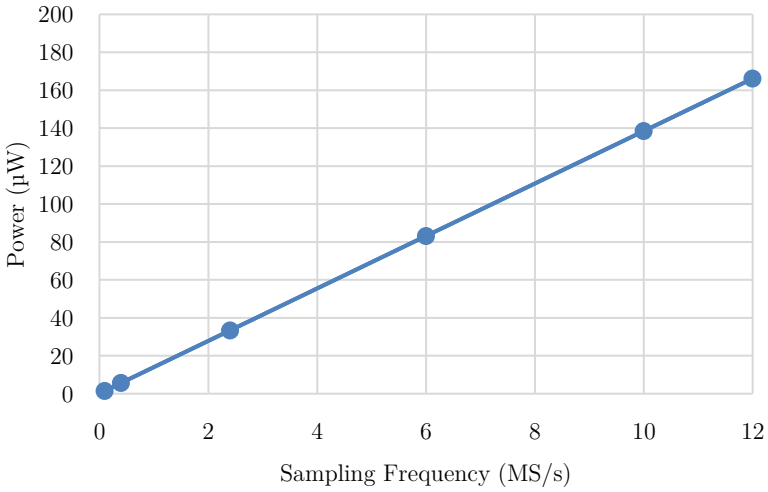
Sampling Rate [MS/s]	**Input frequency**	**ENOB [bit]**	**SFDR [dBc]**	**Power [µW]**	**FOM [fJ/Conv. step]**
0.001	497.0703125 Hz	9.07	69.5	0.205	383.67
0.005	2.4853515625 kHz	9.07	70.27	0.26	97.32
0.01	4.970703125 kHz	9.07	69.92	0.329	61.57
0.05	24.853515625 kHz	9.07	69.61	0.882	33.01
0.1	49.70703125 kHz	9.05	70.23	1.574	29.87
0.4	198.828125 kHz	9	70.71	5.723	28.10
2.4	1.19296875 MHz	9.02	70.25	33.37	26.94
6	2.982421875 MHz	9	70.15	83.15	27.22
10	4.970703125 MHz	9	69.92	138.49	27.20
12	5.96484375 MHz	9.04	70.64	166.14	26.45

Source: Author.

Although the simulation results for power consumption are within the boundaries of normality, the same cannot be said about the simulated ENOB. This parameter was

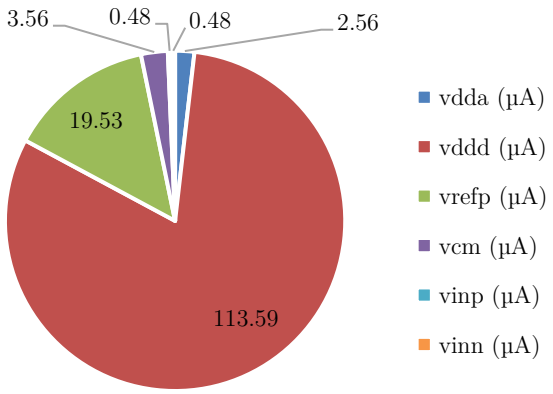
expected to be higher than 9.3 for post-layout simulations, as shown in different works in the literature. The average simulated value of 9, besides degrading the FOM, indicates performance problems and further investigation were performed to find its root cause, which is detailed in the next sub-section.

Figure 5.2 – Simulated average power consumption vs. Sampling Frequency.



Source: Author.

Figure 5.3 – ADC average current consumption @12MS/s.



Source: Author.

5.1.2 DNL and INL

A practical way to extract DNL and INL parameters of an ADC is to use the histogram method, also referred as code density test (MAXIM INTEGRATED, 2003).

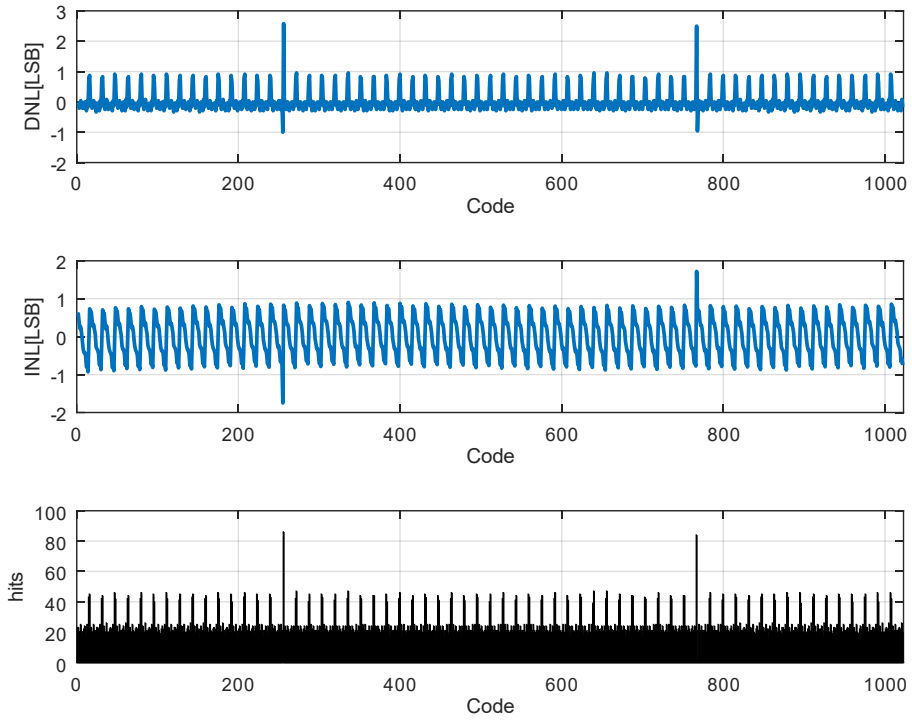
In this work it was performed by running a transient simulation where the ADC converts a huge number of samples of a differential ramp input signal (*vinp* increasing from zero up to the full-scale voltage and *vinn* decreasing from the full-scale voltage down to zero). Since the input signal characteristics guarantee that the sampled analog values are evenly spaced across the input range, every converted code of an ideal histogram should ideally present the same density.

The DNL and INL are calculated according discrepancies between the ideal histogram and the histogram generated by the actual converted codes. By using the test bench of Figure 5.1 with the abovementioned input signal characteristics, a transient simulation was run with sampling frequency of 12 MS/s for 25.603 conversions, in typical corner at 27 ºC, where the first three conversions were not considered since they were generated when the system was not in permanent regime. Note that the increasing and decreasing ramp are inclined such that all the codes in the histogram are expected to present 25 hits.

The extracted parameters for each code are shown in Figure 5.4. It can be noted that for codes 255 and 768 the DNL presented magnitude greater than 1, meaning that a monotonic behavior with no missing codes is not guaranteed in the transfer function. In fact, Figure 5.5 shows the simulated ADC output codes for a decreasing ramp input signal, where a missing code (255) is spotted, greatly degrading the DNL, the INL and the ENOB.

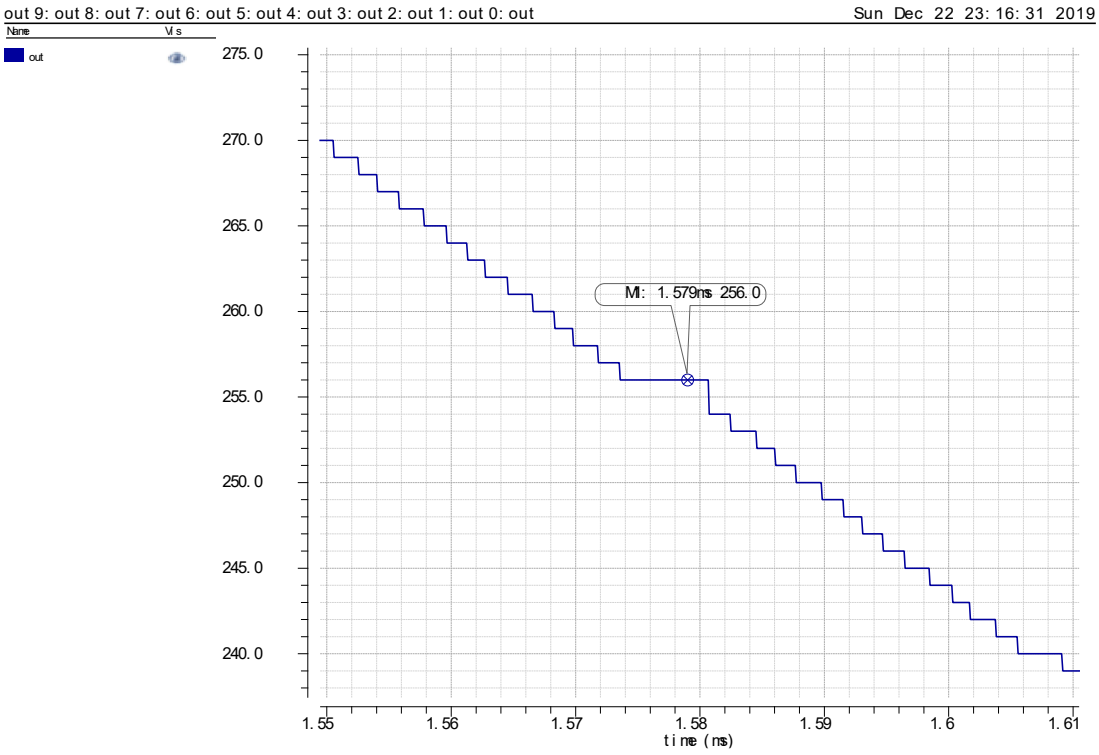
The internal signals of the ADC during the conversion of code 255 were captured in Figure 5.6 and reveals that the nodes *vdacp* and *vdacn* are not appropriately converging because the charge redistribution in the first DAC switching is not fast enough (green circle). In this case, the dynamic comparator is entering in regeneration phase before the proper settling of the DAC voltage, leading to a wrong comparison and, subsequently, the wrong conversion to code 256.

Figure 5.4 – DNL, INL and histogram of the simulated ADC.



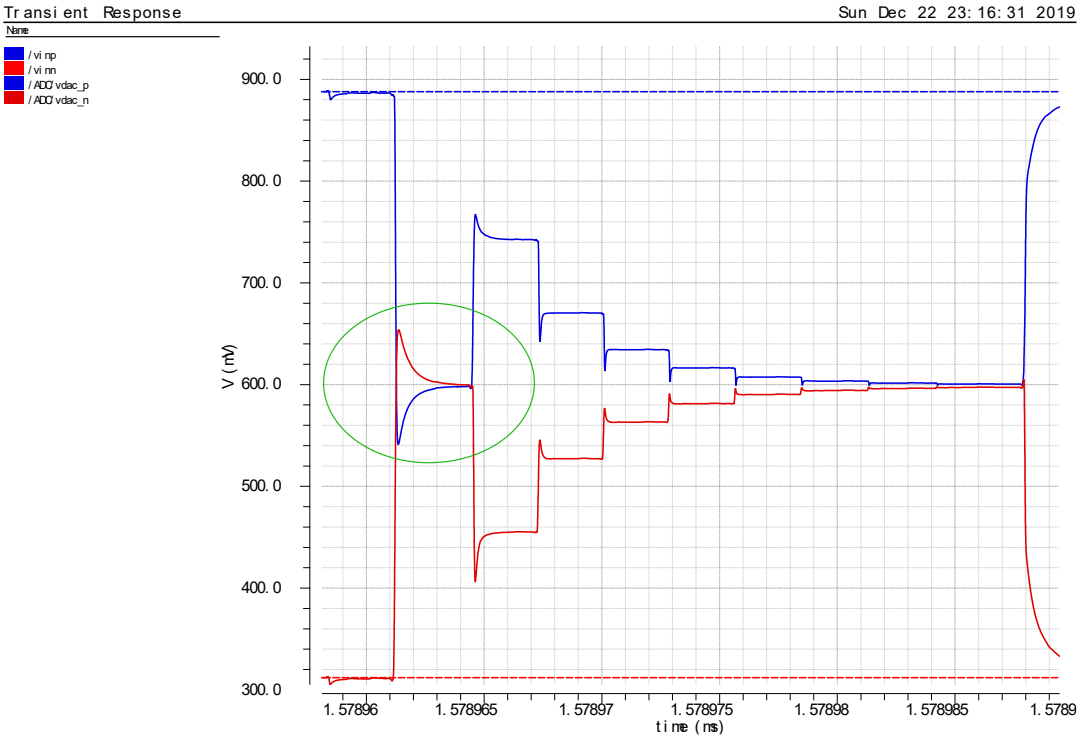
Source: Author.

Figure 5.5 – Conversion of a decreasing ramp input signal, zoomed around code 256.



Source: Author.

Figure 5.6 – Error for conversion to code 255.



Source: Author.

5.1.3 The bootstrapped switch

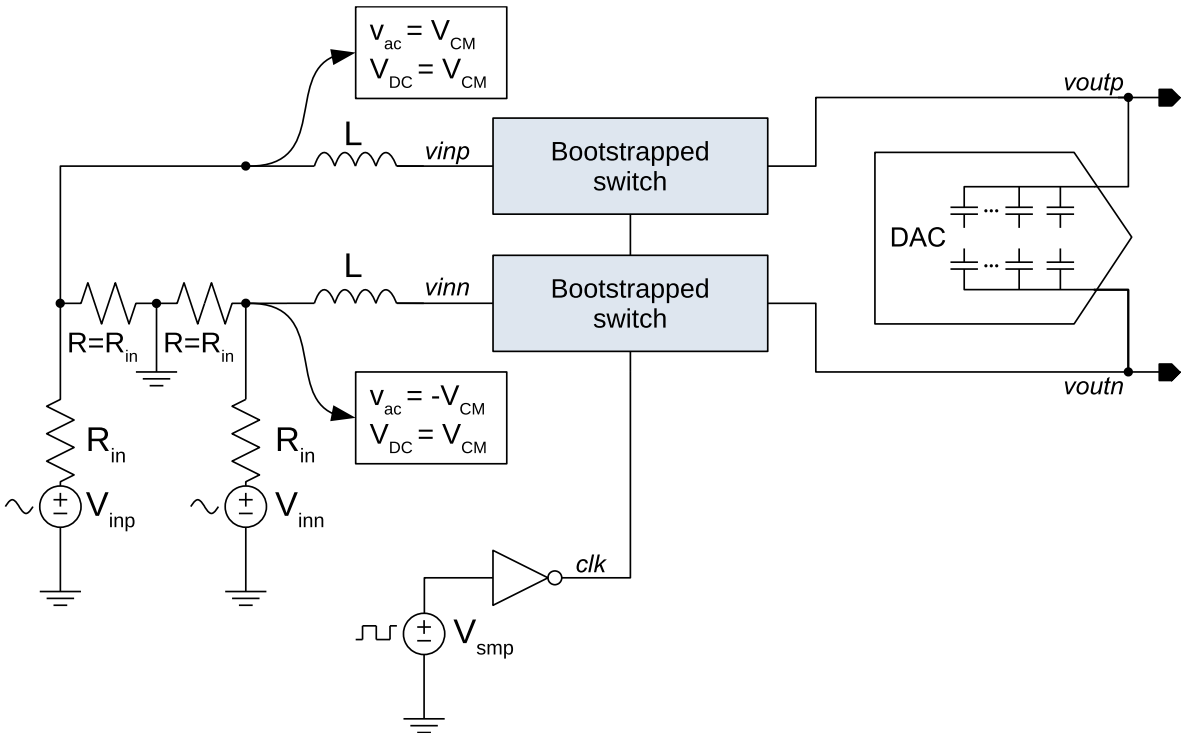
The bootstrapped circuit is also evaluated in this section because the effective resolution of the ADC is strongly related to the switch performance and it can be easily simulated out of the system level. The test bench for the bootstrapped switch is shown in Figure 5.7. The objective is to take analog samples of a perfect sinusoid and compute its DFT. The obtained frequency spectrum will present the fundamental tone alongside the distortions added by the switches, which can be used to compute its ENOB.

Considering the ADC makes use of two bootstrapped switches to sample differential signals, two voltage sources were added to provide a differential signal to the input nodes of two switches. A voltage-controlled voltage source is placed between the outputs of both switches to translate the analog differential output to an analog single ended output for proper DFT computation. Also, the capacitor array and the comparator were added to the output node as simple loads.

For better characterization, a differential input signal, with an appropriate frequency for coherent sampling, must be applied into the input of the circuit. It presents the same characteristics of the one applied in sub-section 5.1.1.

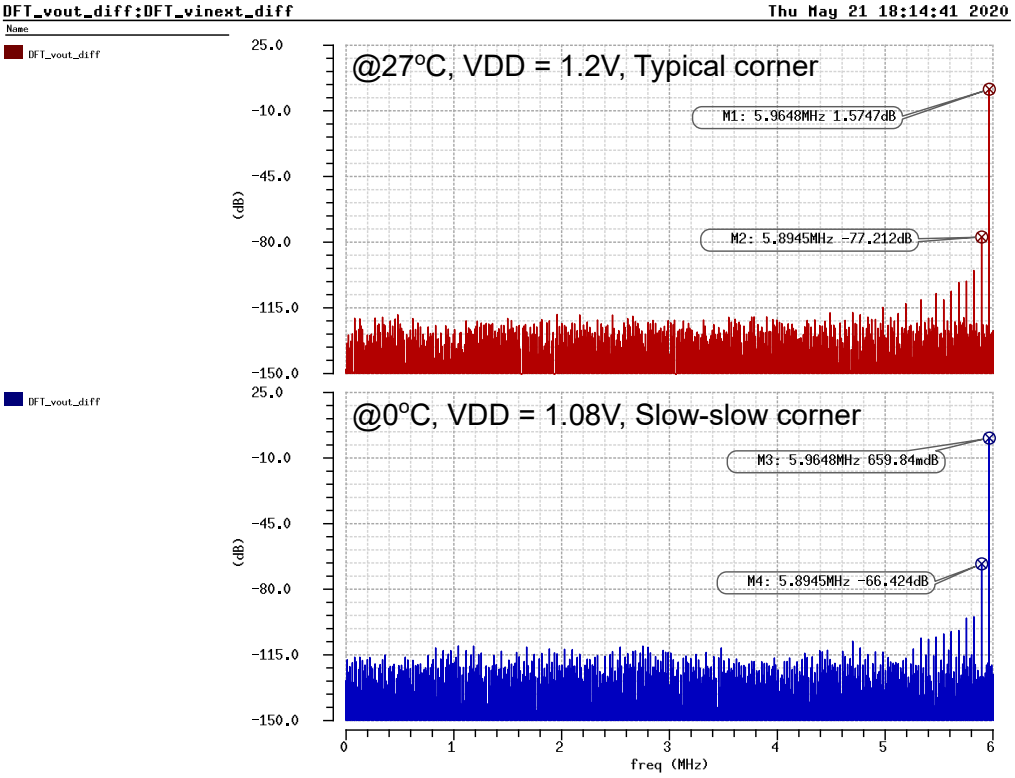
By using the setup of Figure 5.7, a transient simulation was run in typical corner at 27 ºC and V_{DD} = 1.2 V. For 1024 samples, it resulted in an ENOB of 12.72 for a 5.96 MHz input signal, at 12 MS/s, as shown in Figure 5.8. Although this result satisfies the resolution requirement for a 10-bit SAR ADC (ENOB of 12), the circuit was not proved to be robust in simulations considering the effects of Process-Voltage-Temperature (PVT) variations. In fact, the circuit presented an ENOB of 10.84 in the worst case of PVT variations (Slow-Slow corner, V_{DD} = 1.08 V and T = 0 ºC), mainly due to the capacitor C_3 not being properly charged before the next sampling phase.

Figure 5.7 – Test bench circuit for the bootstrapped switch.



Source: Author.

Figure 5.8 – Computed DFT of the differential output signal of the bootstrapped switch.



Source: Author.

5.1.4 The comparator

The comparator was characterized as in (AGAH, 2009). It extracts τ_L by running a set of transient simulations, each with a different constant input voltage, $\Delta V_{in,k}$. If the set of input voltages are arranged in a geometric progression with a common ratio of 1/10, i.e., $\Delta V_{in,n} = \Delta V_{in,n\text{-}1}/10$, equation 3.49 can be used to derive

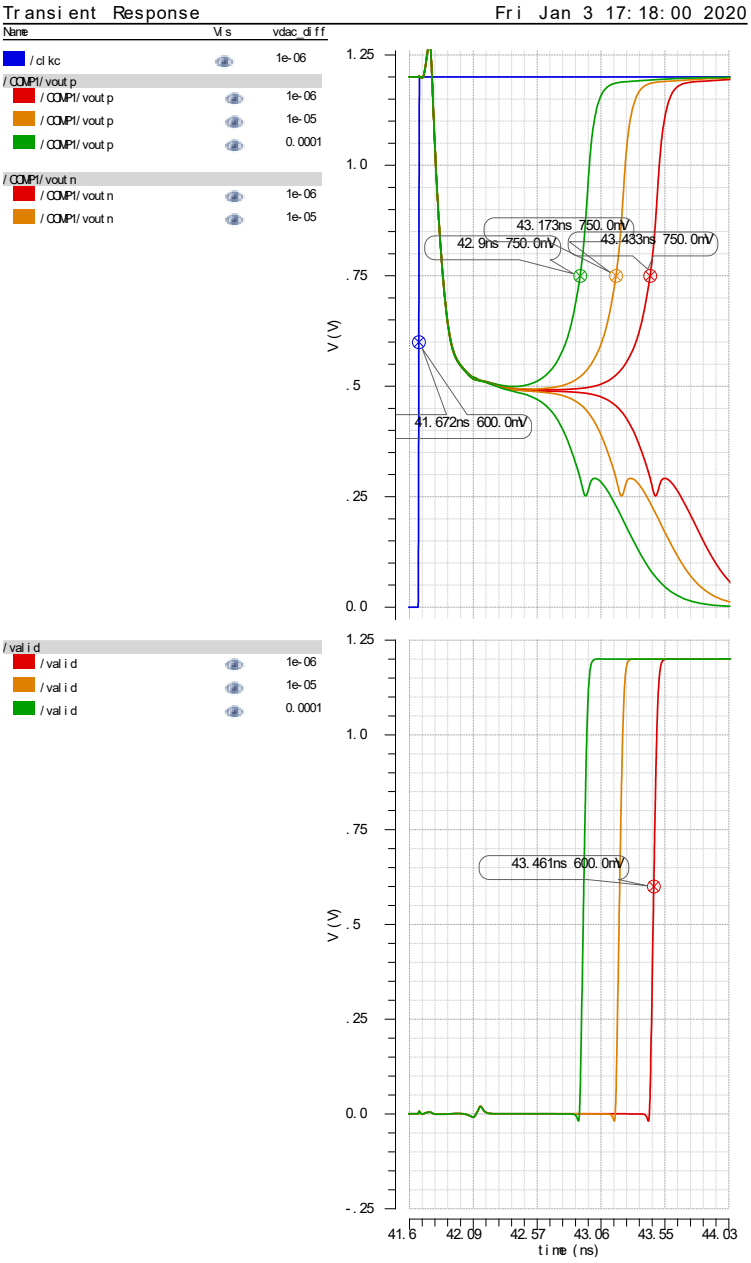
$$\tau_L \approx \frac{t_{pL,n} - t_{pL,n-1}}{\ln 10}. \tag{5.1}$$

It is worthwhile noting that, since we are dealing with a post-layout schematic, the comparator presents non-idealities. So, prior any simulation, the systematic offset value, due to parasitic elements, must be found and compensated, otherwise it would significantly affect the obtained value of $t_{pL,k}$. The offset value was found by running transient simulations with different values of ΔV_{in} until t_{pL} to reach a large value. A small number of iterations (simulations) were required to find the offset of the

comparator with a µV precision. In this implementation, the offset value of 1.41067 mV was found and compensated by adding a constant voltage source in the input node.

After this compensation, transient simulations were run in typical corner at 27 ºC and $V_{DD} = 1.2$ V. Figure 5.9 shows the set of simulation results for different ΔV_{in} values (1 µV, 10 µV and 100 µV), which were used in equation 5.1 to calculate $\tau_L = 112.91$ ps.

Figure 5.9 – Comparator delay for different input voltages (1 µV, 10 µV and 100 µV) at typical corner.



Source: Author.

The same procedure was followed to calculate the time constant in the worst case

of PVT variations (Slow-Slow corner, V_{DD} = 1.08 V and T = 85 ºC). Under this condition, an offset of 1.33351 mV was found and compensated to proper extract $\tau_{L,worst}$ = 174.73 ps.

These results are used in the metastability analysis of the next sub-section.

5.1.5 Metastability

In the previous sub-sections, it was not observed any errors in the output codes of the converter due to metastability. It does not mean, though, they are inexistent. In fact, it could take a huge amount of conversions to observe a single case of metastability. With that in mind, it becomes clear that it is more efficient to estimate the probability of a metastability event to happen, rather than trying to reproduce it, in the ADC.

The probability of the asynchronous SAR ADC to enter a metastable state is ruled by equation 4.4. Therefore, if one extracts the values of τ_L and $t_{margin} = (T_S - t_{track} - T_{FIX,TOT} - T_{easy})$, the CER is straightforwardly obtained.

The τ_L parameter of the comparator was obtained in the previous sub-section, whereas the t_{margin} parameter for the ADC, running at 12 MS/s, can be obtained from the simulation results of section 5.1.1. By observing the internal signals waveforms (Figure 2.8), the t_{margin} is calculated as the time difference between the rising of the *eoc* flag and the falling of the *sample_clk* signal in the time chart. As result, for the obtained values of t_{margin} = 11.74 ns and τ_L = 112.91 ps, the CER is $1.42 \cdot 10^{-42}$. Although this is an exceptional value for typical case of PVT, simulations of the ADC in the worst case (Slow-Slow corner, V_{DD} = 1.08 V and T = 85 ºC) presented $t_{margin,worst} = (T_S - t_{track} - T_{FIX,TOT} - T_{easy}) < 0$, meaning the ADC will present timing violation and, therefore, it is not able to work under this condition.

5.2. The second version

The redesign and simulation results regarding the second implementation of the

ADC are presented in this sub-section. Every simulation makes use of the post-layout schematic view, containing parasitic resistances and capacitances extracted by the Calibre PEX tool from the layout view.

The redesign of the sub-circuits, alongside their better placement and routing, resulted in an expressive improvement of the effective resolution of the ADC, even considering PVT variations.

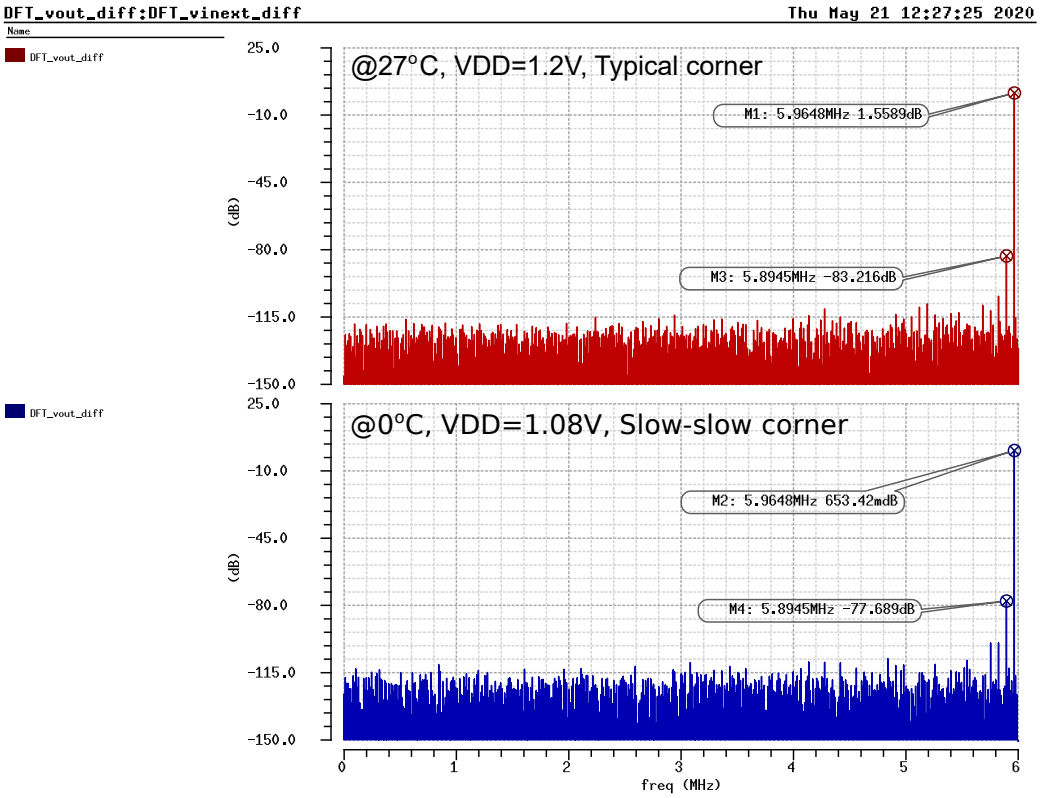
5.2.1 The redesign of the bootstrapped switch

It was observed in the first version that the bottleneck of the switch performance is the ineffective charging of C_3 by the voltage doubler circuit. In this version, the capacitance value of C_3 was reduced (alleviating M_3 and M_4) and the voltage doubler circuit had the size of its devices increased to provide more charge to C_1 and C_2.

Since we had decreased the size of C_3, the widths of M_5-M_{11} were also slightly decreased to reduce the voltage drop due to the charge redistribution with parasitic capacitances.

By using the same simulation setup of sub-section 5.1.3, a transient simulation was run for the second version of the switch in the typical corner at 27 ºC and V_{DD} = 1.2 V. For 1024 samples, it resulted in an ENOB of 13.74 for a 5.96 MHz input signal, at 12 MS/s, as shown in Figure 5.10. In the worst case of PVT variations (Slow-Slow corner, V_{DD} = 1.08 V and T = 0 ºC) the circuit achieved an ENOB of 12.68.

Figure 5.10 – Computed DFT of the differential output signal of the bootstrapped switch.



Source: Author.

5.2.2 The redesign of the comparator

The first version of the comparator was redesigned to further increase its reliability and decision time. In this redesign, it was added a pair of transistors (M_{13}/M_{14}) and a pair of buffers ($BUFF_1/BUFF_2$), as shown in Figure 4.3. Also, the dimensions of its devices were reduced.

As pointed out in section 4.3, the discharging of *ap2*/*an2* through M_{13}/M_{14} imposes the same voltage level at the gate of M_6/M_5 in the beginning of the regeneration phase. It is expected that, after the addition of M_{13}/M_{14}, comparisons will not be influenced by the results of the previous ones due to remaining charges in these high impedance nodes.

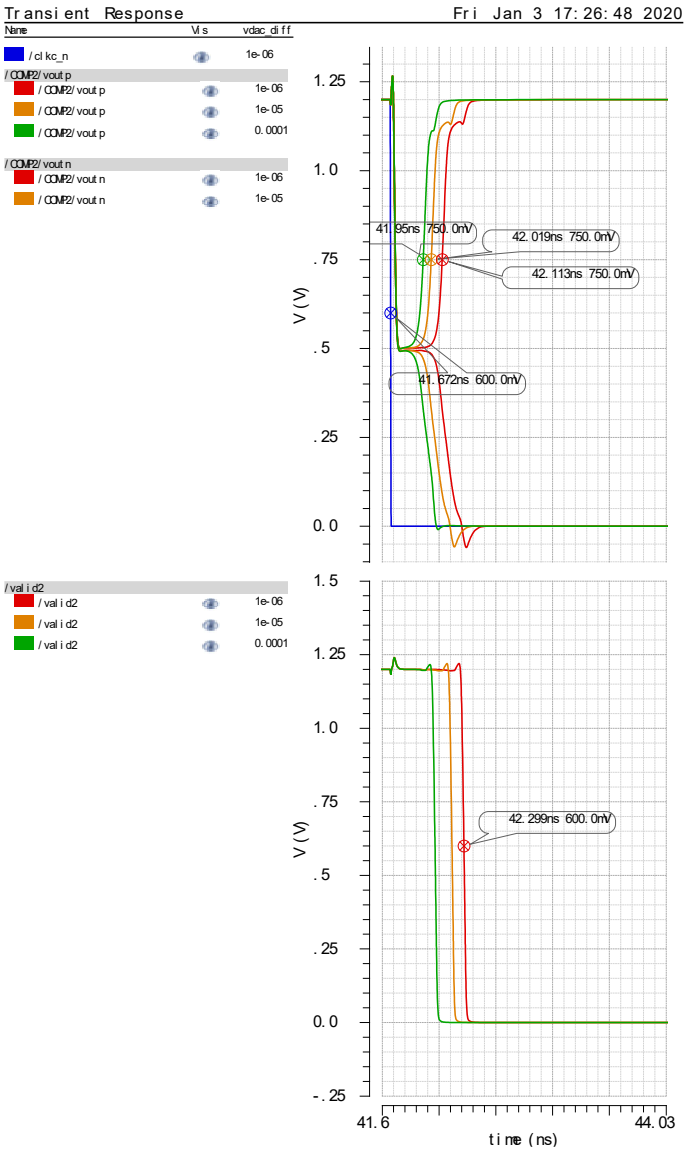
The addition of buffers $BUFF_1$ and $BUFF_2$ in the output logic of the comparator further isolates the output node and the latch. It also permitted the size reduction of INV_1 and INV_2 because the buffers themselves present a much lower capacitive load. The

size reduction of the inverters leads to a reduced capacitive load to *voutp* and *voutn*, improving the decision time of the comparator.

As the last modification, the lengths of the transistors were reduced. This represents a change of compromise by worsening the matching to further improve the decision time and P_{meta}.

Now, by using the same methods of sub-section 5.1.4, the new comparator offset was found and compensated (4.633895 mV) and new transient simulations were run to evaluate the circuit performance. Figure 5.11 shows the simulation results.

Figure 5.11 – Comparator delay for different input voltages (1 µV, 10 µV and 100 µV) at typical corner.



Source: Author.

In the typical corner, it was observed a decrease in τ_L to 29 ps, due to smaller capacitances. In the worst case of PVT variations, (Slow-Slow corner, V_{DD} = 1.08 V and T = 85 ºC) an offset of 5.369196 mV was found and compensated to proper extract $\tau_{L,worst}$ = 52.34 ps.

These results are used in the metastability analysis of sub-section 5.2.6.

5.2.3 The redesign of the DAC switches

The DAC switches had their widths significantly increased to provide a smaller resistance path between the reference voltages and the capacitors of the DAC. So, the charge redistribution presents a faster voltage settling and the missing code errors (Figure 5.6) are mitigated. Because of using larger switches, the logic circuit responsible for controlling them is also slightly increased to deal with larger parasitic gate capacitances.

Also, the logic circuit, which is responsible for connecting the capacitors of the DAC from *vcm* to *vrefp*/*vrefn*, was modified. In the first version, the switch between the capacitors and *vrefp*/*vrefn* is closed simultaneously the opening of the switch between them and *vcm*, shorting *vrefp*/*vrefn* and *vcm* for a brief period. After a minor correction, the system was modified to not change the switches at the same time during the conversion phase.

5.2.4 Power consumption and ENOB

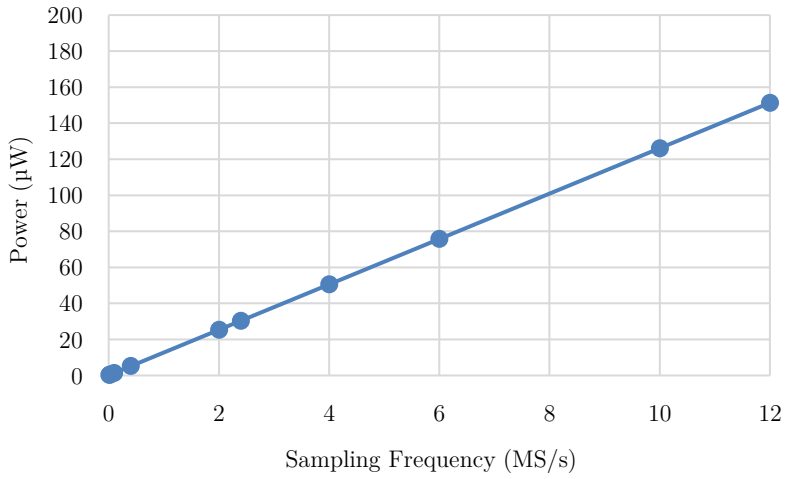
Transient simulations of the second version of the ADC were performed and the results were extracted using the same methods of sub-section 5.1.1. They are summarized in Table 5.2. The simulated power consumption of the circuit still presented an almost linear dependency of the sampling frequency, as expected and shown in Figure 5.12. Also, like in the first version, the biggest contribution to the power consumption are given by the digital circuitry (current sinking from *vddd*) and by the capacitive DAC (current sinking from *vrefp*), as shown in Figure 5.13.

Table 5.2 – Simulated ADC dynamic parameters for different sampling frequencies (second version).

Sampling rate [MS/s]	**Input frequency**	**ENOB [bit]**	**SFDR [dBc]**	**Power [µW]**	**FOM [fJ/Conv. step]**
0.01	4.970703125 kHz	9.63	73.08	0.26	32.8
0.1	49.70703125 kHz	9.62	73.51	1.39	17.8
0.4	198.828125 kHz	9.65	74.38	5.17	16.2
2	994.140625 kHz	9.65	74.28	25.3	15.9
2.4	1.19296875 MHz	9.59	73.26	30.4	16.5
4	1.98828125 MHz	9.63	72.96	50.5	16.0
6	2.982421875 MHz	9.61	73.32	75.7	16.3
10	4.970703125 MHz	9.61	74.13	126.1	16.2
12	5.96484375 MHz	9.65	75.36	151.4	15.8

Source: Author.

Figure 5.12 – Simulated average power consumption vs. Sampling Frequency.



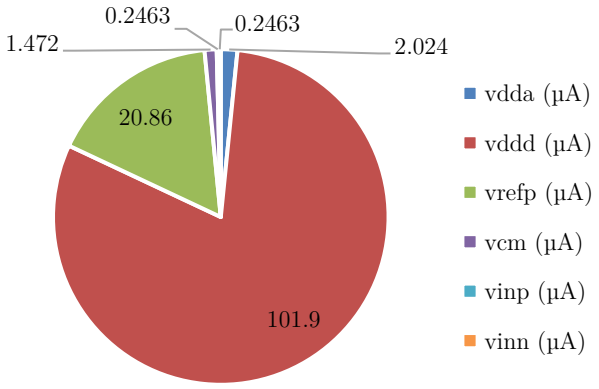
Source: Author.

Additionally, simulations considering process (TT, FF and SS), supply voltage (1.08 V, 1.2 V and 1.32 V) and temperature (0 ºC, 27 ºC and 85 ºC) variations were also run. The results of interest are:

- The worst result for ENOB was 9.44, at (Fast-Fast corner, V_{DD} = 1.32 V and T = 0 ºC).
- The best result for ENOB was 9.69, at (Slow-Slow corner, V_{DD} = 1.08 V and T = 85 ºC).

- The worst result for power consumption was 228.1 µW, at (Fast-Fast corner, V_{DD} = 1.32 V and T = 85 ºC).
- The best result for power consumption was 118 µW, at (Slow-Slow corner, V_{DD} = 1.08 V and T = 0 ºC).

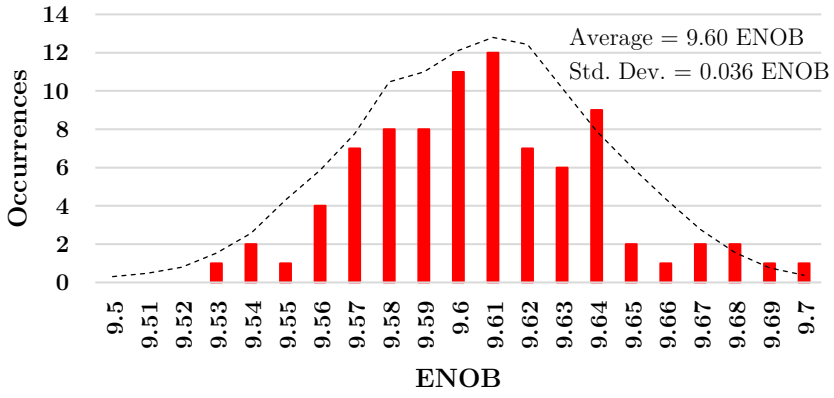
Figure 5.13 – ADC average current consumption @12MS/s.



Source: Author.

Finally, Monte Carlo simulations were run to estimate the impact of the device-to-device and process variations into the ENOB. The obtained results, shown in Figure 5.14, indicate that the cares taken throughout the design procedure resulted in a small standard deviation. Unfortunately, since each simulation required a huge computational time, the number of simulations are small (85) and the confidence degree is somewhat compromised.

Figure 5.14 – Monte Carlo simulations for ENOB



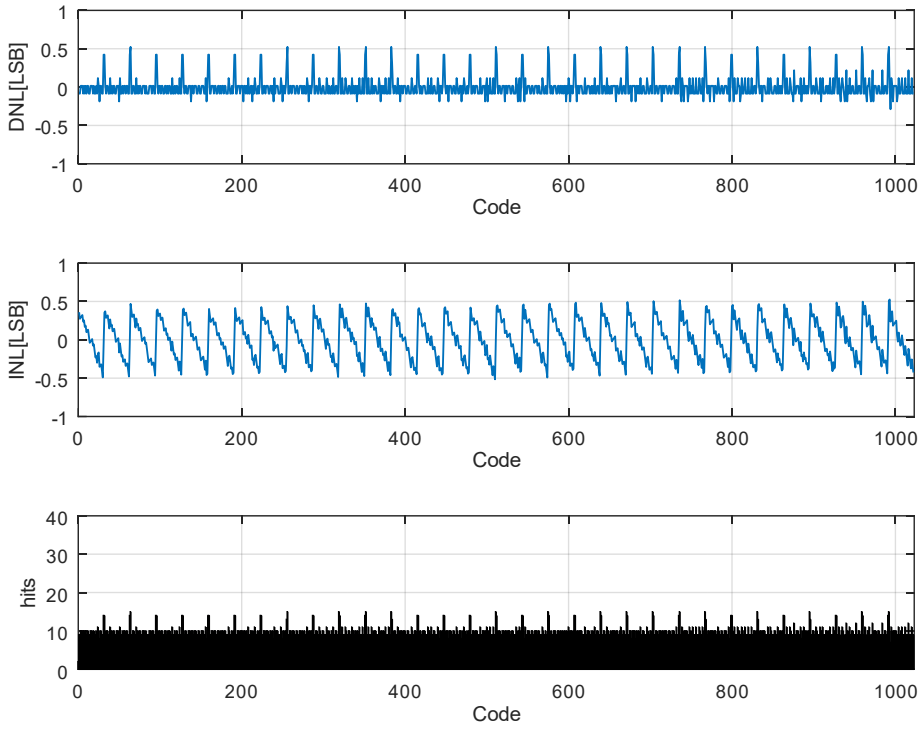
Source: Author.

5.2.5 DNL, INL, offset and gain errors

DNL and INL parameters of the second version of the ADC were extracted using the same methods of sub-section 5.1.2. The extracted parameters for each code are shown in Figure 5.15. The redesign of the DAC switches successfully solved the missing codes problem. The worst DNL and INL errors were significantly reduced to, respectively, 0.52 LSB and 0.53 LSB.

Additionally, the results of this transient simulation were also used to obtain the offset and gain errors. The calculated gain error was 18.1 LSB (less than 1.8% of the full-scale range) whereas the calculated offset error was –11.1 LSB (less than 1.1% of the full-scale range).

Figure 5.15 – DNL, INL and histogram of the simulated ADC.



Source: Author.

5.2.6 Metastability

The new time margin of the ADC at 12 MS/s, t_{margin} = 17.45 ns, was obtained

from the simulations of sub-section 5.2.4. By observing the internal signals waveforms (Figure 2.8), the t_{margin} is calculated as the time difference between the rising of the *eoc* flag and the falling of the *sample_clk* signal in the time chart. As result, for the obtained values of t_{margin} = 17.45 ns and τ_L = 29 ps at typical corner, the CER is negligible (on the order of 10^{-258}, even smaller than the one found in the first version).

For the worst case of PVT variations (Slow-Slow corner, V_{DD} = 1.08 V and T = 85 ºC), the obtained $t_{margin,worst}$ = 1.4 ns significantly deteriorates the CER to $4.95 \cdot 10^{-9}$. For analog frontends with BER ranging from 10^{-3} down to 10^{-6}, the designed ADC will not be a bottleneck for the system performance. For more strict applications, the supply voltage specification for the ADC must be relaxed. For example, if the circuit that provides the supply voltage to the ADC has its voltage regulation tightened to V_{DD} = 1.2V ± 5 %, the worst case of PVT variations for the ADC is (Slow-Slow corner, V_{DD} = 1.14 V and T = 85 ºC). In this condition, the time margin is $t_{margin,worst}$ = 6.4 ns, the time constant is $\tau_{L,worst}$ = 44.81 ps, and the CER is reduced (exponentially) to $1.92 \cdot 10^{-59}$.

6. Conclusions and future work

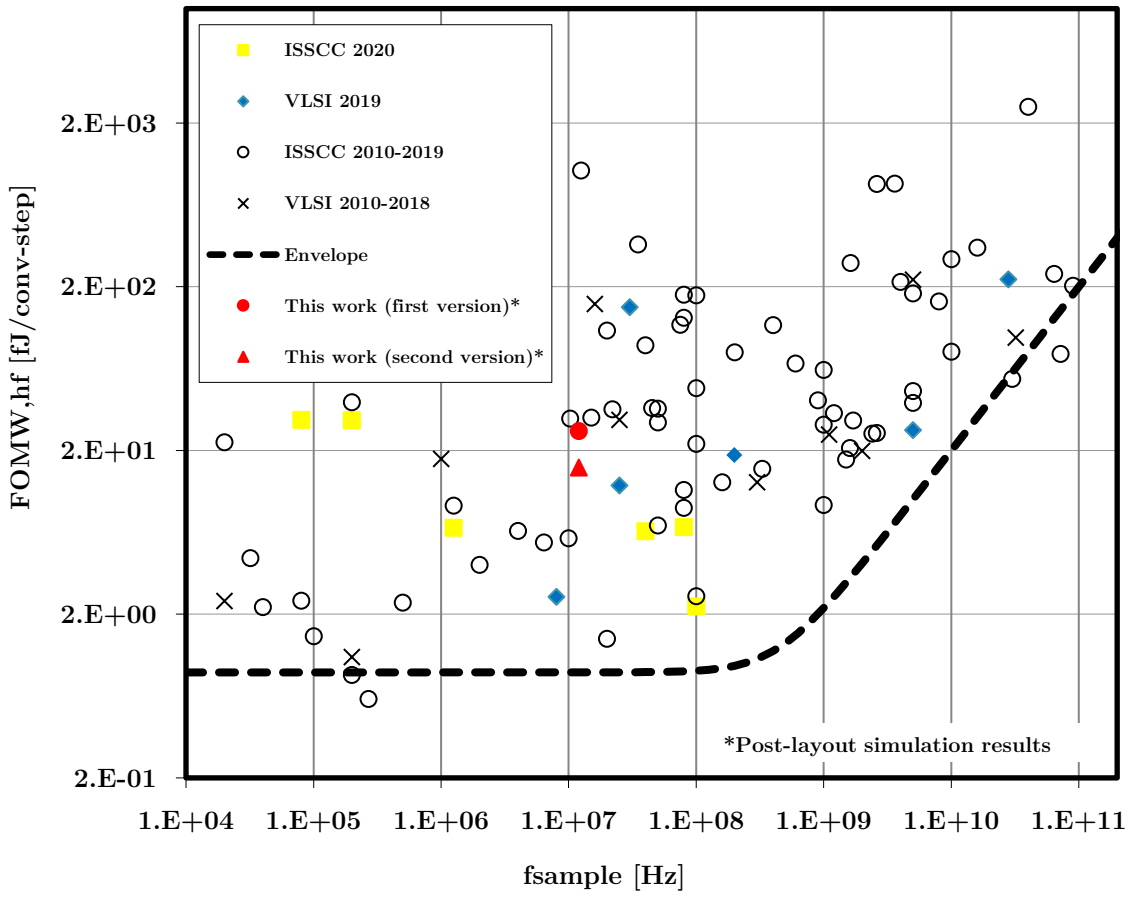
A low-power 10-bit differential asynchronous SAR ADC was successfully designed, drawn to layout, and simulated. The switches of the asynchronous topology of (HARPE, ZHOU, *et al.*, 2010) were modified to support the merged capacitor switching scheme (HARIPRASATH, GUERBER, *et al.*, 2010) using top-plate sampling. A reduced kick-back noise comparator (HUANG, SCHLEIFER and KILLAT, 2013) was applied and presents low power consumption, although additional transistors were required to discharge internal nodes. Also, improved switches were designed to warrant the linearity (ABO and GRAY, 1999). All the modifications resulted in an ADC with a performance comparable with the best circuits of the literature, as shown in Figure 6.1. In post-layout simulations, the circuit achieved a FOM of 32.8 fJ/conversion-step, at 10 kS/s, and a FOM of 15.8 fJ/conversion-step, at 12 MS/s, making it suitable for low-power frontend receivers with signal bandwidth ranging from 10kHz up to 5.96 MHz.

The probability of the system entering in a metastable state was evaluated and a faster comparator was redesigned. The new ADC will typically present an extremely low CER. In the wort case, the CER is $4.95 \cdot 10^{-9}$, suitable for some low-power wireless frontends like Zigbee and Bluetooth Low Energy.

In this design, it was observed an important compromise between system robustness and power consumption. The improvement of the system robustness to PVT variations led to an oversizing of the DAC switches and their logic circuit, wasting additional energy to charge/discharge parasitic capacitances. The switches had to be enlarged to ensure the charge redistribution in the capacitive DAC is done, even in harsh conditions, where the switch on-resistance is greatly reduced at low temperature, low voltage regulation and Slow-slow process variation. Moreover, the post-layout simulations have

shown the need for strong logic cells and output buffers for a reliable signal steering between the ADC sub-blocks and the top-level circuitry. This additional logic cells means that minimal width transistors could not always be used, increasing the system power consumption.

Figure 6.1 – FOM vs. Sampling frequency for recently published SAR ADC designs.



Source: (MURMANN, 2020).

Finally, a comparison between the simulation results of this work with the measurement results of SAR ADC designs with similar technological node, resolution and sampling frequency, is shown in Table 6.1.

The Future work for this project include:

- Perform chip measurements and compare with the simulation results.
- Optimize the Comparator Control circuit to an asynchronous logic.

Table 6.1 – Performance comparison of similar SAR ADCs.

Specifications	(YOSHIOKA, ISHIKAWA and T. TAKAYAMA, 2010)	(CHEN, MIYAHARA and MATSUZAWA, 2015)	(ELZAKKER, TUIJL, *et al.*, 2008)	(LIU, CHANG, *et al.*, 2010)	**This work***
Technology [nm]	65	65	65	180	65
Resolution [bit]	10	10	10	10	10
Supply Voltage [V]	1	0.8	1	1	1.2
Samp. Freq. [MS/s]	50	50	1	10	12
Input Freq. [MHz]	25	6.25	0.5	1	5.96
SNDR [dB]	56.6	58	54.4	60.97	59.8
ENOB [bit]	9.1	9.35	8.74	9.83	9.65
Power [µW]	820	120.7	1.9	98	151.4
FOM [fJ/Conv. step]	29.7	14.8	4.4	11	15.8
Core Area [mm²]	0.039	0.012	0.027	0.086	0.074

***Post-layout simulation results**

Source: Author.

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Appendix A. Devices list

This appendix lists the sizing of all devices, for each circuit designed in this work.

Appendix Table A.1 – The DAC capacitors.

Device name	Sizing
C_u	42 fF
Cp_{bridge}, Cn_{bridge}	$1 \cdot C_u$
Cp_0, Cn_0	$1 \cdot C_u$
Cp_1, Cn_1	$2 \cdot C_u$
Cp_2, Cn_2	$4 \cdot C_u$
Cp_3, Cn_3	$8 \cdot C_u$
Cp_4, Cn_4	$1 \cdot C_u$
Cp_5, Cn_5	$2 \cdot C_u$
Cp_6, Cn_6	$4 \cdot C_u$
Cp_7, Cn_7	$8 \cdot C_u$
Cp_8, Cn_8	$16 \cdot C_u$

Source: Author.

Appendix Table A.2 – The DAC switch transistors, for bits 0 to 3.

Device	Width	Fingers	Length
The PMOS of transmission gates	2.32 µm	16	60 nm
The NMOS of transmission gates	1 µm	16	60 nm
The PMOS of logical gates	920 nm	2	60 nm
The NMOS of logical gates	560 nm	2	60 nm

Source: Author.

Appendix Table A.3 – The DAC switch transistors, for bits 4 to 8.

Device	Width	Fingers	Length
The PMOS of transmission gates	2.32 µm	32	60 nm
The NMOS of transmission gates	1 µm	32	60 nm
The PMOS of logical gates	920 nm	4	60 nm
The NMOS of logical gates	560 nm	4	60 nm

Source: Author.

Appendix Table A.4 – The bootstrapped switch transistors.

Device	Width	Fingers	Length
M_1	440 nm	2	60 nm
M_2	440 nm	2	60 nm
M_3	440 nm	4	60 nm
M_4	440 nm	4	60 nm
M_5	440 nm	2	60 nm
M_6	440 nm	1	60 nm
M_7	440 nm	1	120 nm
M_8	440 nm	1	120 nm
M_9	440 nm	4	60 nm
M_{10}	440 nm	1	60 nm
M_{11}	1.16 µm	4	60 nm

Source: Author.

Appendix Table A.5 – The bootstrapped switch capacitors.

Device	Capacitance
C_1	35 fF
C_2	35 fF
C_3	155 fF

Source: Author.

Appendix Table A.6 – The dynamic comparator transistors.

Device	Width	Fingers	Multiplier	Length
M_1, M_2	680 nm	1	4	60 nm
M_3, M_4	680 nm	1	4	60 nm
M_5, M_6	440 nm	1	2	60 nm
M_7, M_8	440 nm	1	2	60 nm
M_9, M_{10}	920 nm	1	2	60 nm
M_{11}, M_{12}	920 nm	1	2	60 nm
M_{13}, M_{14}	440 nm	1	2	60 nm

Source: Author.

Appendix Table A.7 – The Main Control transistors.

Device	Width	Fingers	Length
M_1	600 nm	1	60 nm
M_2	600 nm	1	60 nm
M_3	600 nm	1	60 nm
M_4	600 nm	2	60 nm
M_5	600 nm	2	60 nm
M_6	600 nm	4	210 nm
M_7	600 nm	1	60 nm

Source: Author.

Appendix Table A.8 – The DAC Control transistors.

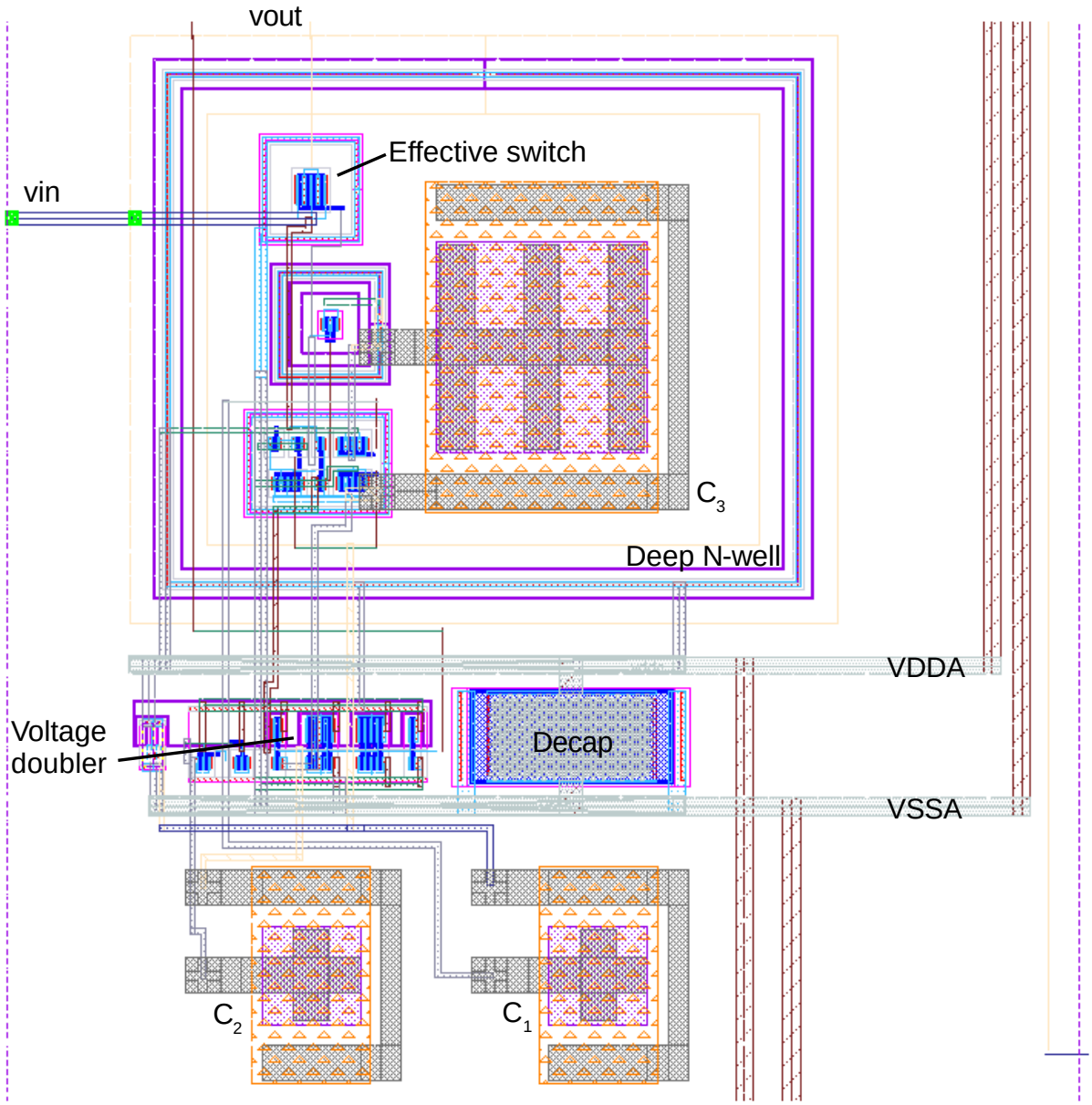
Device	Width	Fingers	Length
M_1	300 nm	1	60 nm
M_2	600 nm	1	60 nm
M_3	600 nm	1	60 nm
M_4	600 nm	2	60 nm
M_5	600 nm	2	60 nm
M_6	600 nm	2	60 nm

Source: Author.

Appendix B. Layout

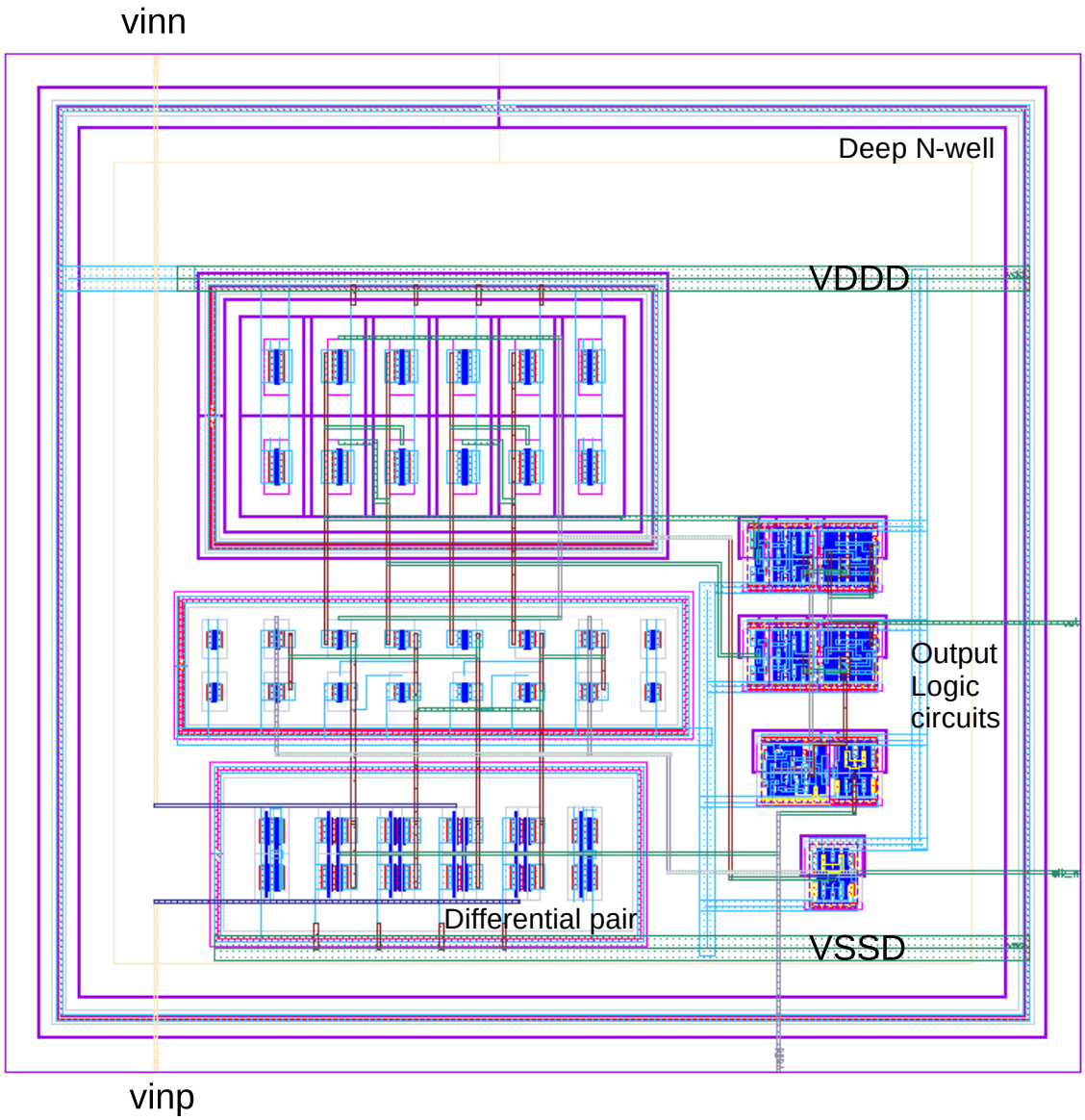
This appendix shows the layout of the circuits designed in this work.

Appendix Figure B.1 – Layout of the bootstrapped switch.



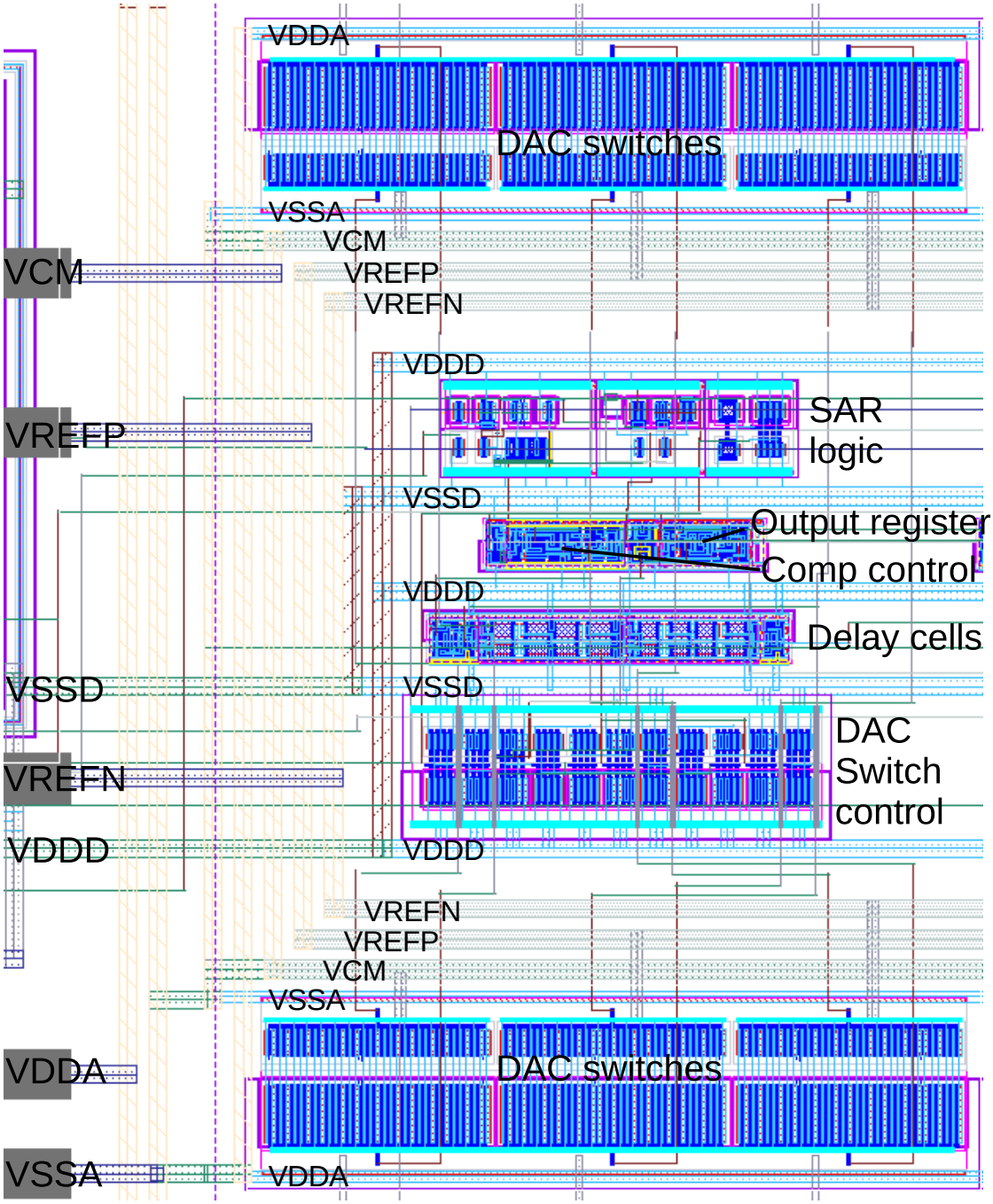
Source: Author.

Appendix Figure B.2 – Layout of the comparator.



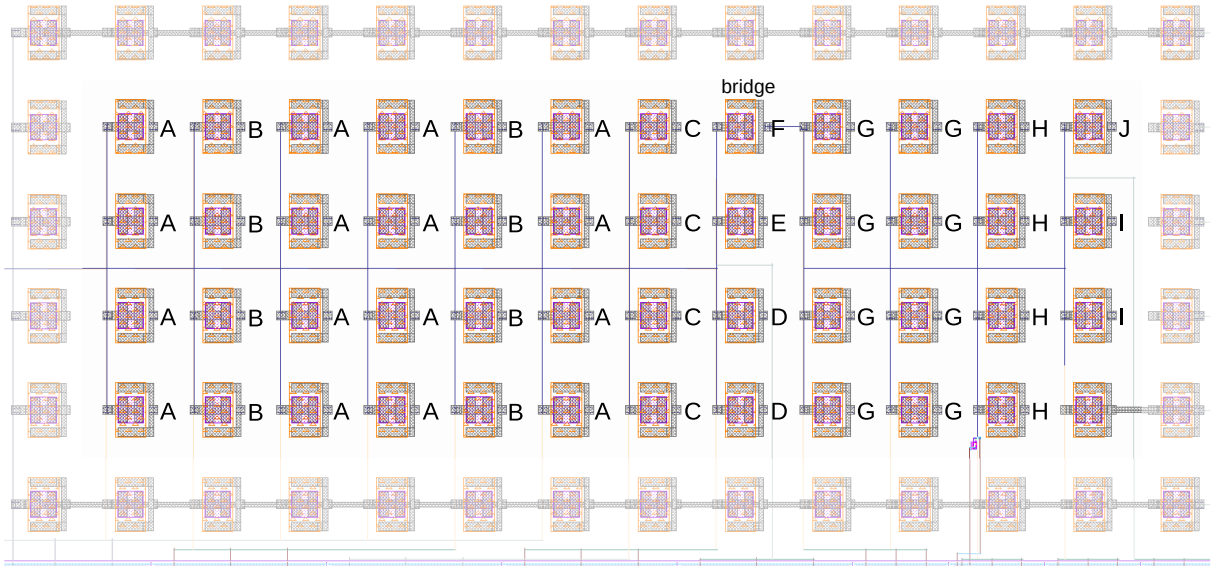
Source: Author.

Appendix Figure B.3 – Layout of the digital circuitry and DAC switches (zoom at the MSB).



Source: Author.

Appendix Figure B.4 – Layout of the differential capacitive DAC (one side).



Source: Author.