INSTITUTO DE PESQUISAS ENERGÉTICAS E NUCLEARES
Autarquia Associada à Universidade de São Paulo

Evaluation of impurities in the Brazilian solar grade silicon and LeTID investigations in p-type multi-Si

DANIEL KNOB

Tese apresentada como parte dos requisitos para obtenção do Grau de Doutor em Ciências na Área de Tecnologia Nuclear - Materiais

Orientador:
Prof. Dr. Humberto Gracher Riella

São Paulo
2019

INSTITUTO DE PESQUISAS ENERGÉTICAS E NUCLEARES

Autarquia Associada à Universidade De São Paulo

Evaluation of impurities in the Brazilian solar grade silicon and LeTID investigations in p-type multi-Si

DANIEL KNOB

Thesis presented as part of the requirements to obtain the Degree of Doctor of Science in the area of Nuclear Technology – Materials

Advisor: Prof. Dr. Humberto Gracher Riella

Versão Corrigida

São Paulo

2019

Como citar:

KNOB, D. ***Evaluation of impurities in the Brazilian solar grade silicon and LeTID investigations in p-type multi-Si***. 2019. 150 p. Tese (Doutorado em Tecnologia Nuclear), Instituto de Pesquisas Energéticas e Nucleares, IPEN-CNEN/SP, São Paulo.
Disponível em: (data de consulta no formato: dd/mm/aaaa)

Ficha catalográfica elaborada pelo Sistema de geração automática da Biblioteca IPEN/USP,
com os dados fornecidos pelo(a) autor(a)

Knob, Daniel
Evaluation of impurities in the Brazilian solar grade silicon and LeTID investigations in p-type multi-Si / Daniel Knob; orientador Humberto Gracher Riella. -- São Paulo, 2019.
150 p.

Tese (Doutorado) - Programa de Pós-Graduação em Tecnologia Nuclear (Materiais) -- Instituto de Pesquisas Energéticas e Nucleares, São Paulo, 2019.

1. Solar Grade Silicon. 2. Multycrystalline Silicon. 3. Solar PV. 4. LeTID. I. Gracher Riella, Humberto , orient. II. Título.

Clara, minha filha, que este esforço seja por um mundo melhor.

Dedico a você e à Luciana.

À Cidinha, Paulo, Tiago, Júlia e bebê, primos e amigos.

Aos meus avós. Miguel, Romilda, Osvaldo e Georgina, em memória.

ACKNOWLEDGMENT

To Igor Martins, lab partner who provided indispensable support for the development of this work.

To Edvaldo Dal Vechio, whose technical support was essential to the thesis, in addition to the moral support.

To Elita F. Urano, for the endless help during the entire work.

To Bent Thomassen, Junjie Zhu from IFE, for the support on laboratory work.

To my father, Paulo José Knob, for the contribution in the work and overall incentive.

To Rune Søndenå, for the joint work and all shared knowledge.

To my Advisor, Humberto Gracher Riella, for the trust, shared knowledge and all the effort on the project.

To IFE (Institute for Energy Technology), for the opportunity of conducting the joint work and for providing lab structure.

To CCN (Centro de Combustível Nuclear) and IPEN for the opportunity and lab structure.

“It is under the greatest adversity that there exists
the greatest potential for doing good, both for
oneself and others.”

Dalai Lama XIV

ABSTRACT

KNOB, D. ***Evaluation of impurities of the Brazilian solar grade silicon and LeTID investigations in p-type multi-Si***. 2019. 119 p. Thesis (Doctorate in Nuclear Technology - Materials) – Instituto de Pesquisas Energéticas e Nucleares – IPEN – CNEN/SP. São Paulo

The cost reductions and the environmental benefits aligned with global concerns about climate change have made solar photovoltaic technology the most installed source of energy in the power sector worldwide. Brazil has the largest know reserves of silicon in the world. Therefore, there is a huge potential for developing a national technology for purifying and manufacturing silicon wafers within an increasingly competitive and efficient photovoltaic industry. The IPEN initiative of investigating the production of metallic silicon and metallurgical route purification required a characterization of samples in different stages of production from quartz to wafer and understanding the characterization methods for silicon wafers taking into account the main defect mechanisms such as light-induced degradation. Metalic silicon is produced in IPEN via magnesiothermal reduction through acid leaching to form a metallurgical grade silicon with relatively low impurities. One more acid leaching step resulted in a specific ultra-metallurgical grade silicon. The same acid leaching was processed in a commercially available Brazilian-made metallurgical grade silicon produced via carbothermal reduction. All samples impurities was measured by ICP-OES. The result is a material with ultra-metallurgical grade silicon content with excess of B and P. While wafer characterization was studied, an extensive investigation was taken on LeTID, which causes remain unknown, at Institute for Energy Technology, Norway. Neighboring high performance mc-Si p-type wafers were tested in different firing process conditions. The effects was investigated in terms of defects activation and a corresponding lifetime degradation and recovery at illuminated annealing. A sample with almost fully suppressed LeTID is shown. A new method have been proposed to separate Boron Oxygen-Light Induced Degradation effects of LeTID, enabling to measure even where it was thought to be fully suppressed. New models for LeTID defect formation and suppression are proposed. Both silicon purification and light-induced degradation characterization in mc-Si studies shows a wide range of research on new production routes that may require tailored processes of crystallization and solar cell manufacturing such as gettering and firing.

Keywords: 1. Solar Grade Silicon. 2. Multycrystalline Silicon. 3. Solar PV. 4. LeTID.

RESUMO

KNOB, D. ***Evaluation of impurities of the Brazilian solar grade silicon and LeTID investigations in p-type multi-Si***. 2019. 119 p. Thesis (Doctorate in Nuclear Technology - Materials) – Instituto de Pesquisas Energéticas e Nucleares – IPEN – CNEN/SP. São Paulo

As reduções de custos e benefícios ambientais alinhadas às preocupações globais com as mudanças climáticas tornaram a tecnologia solar fotovoltaica a fonte de energia mais instalada no setor de energia do mundo. O Brasil possui as maiores reservas conhecidas de silício. Portanto, existe um enorme potencial para o desenvolvimento de uma tecnologia nacional para purificação e fabricação de wafers de silício dentre a indústria fotovoltaica cada vez mais competitiva e eficiente. A iniciativa do IPEN de investigar a produção de silício metálico e a purificação de rotas metalúrgicas exigiu a caracterização de amostras em diferentes estágios de produção, do quartzo ao wafer e a compreensão dos métodos de caracterização dos wafers de silício, levando em consideração os principais mecanismos de defeitos, como a degradação induzida pela luz. O silício metálico é produzido no IPEN através da redução magnesiotérmica através da lixiviação ácida para formar um silício de grau metalúrgico com impurezas relativamente baixas. Mais uma etapa de lixiviação ácida resultou em um silício de grau ultra-metalúrgico específico. A mesma lixiviação foi feita em um silício de grau metalúrgico fabricado no Brasil, disponível comercialmente, produzido por redução carbotérmica. Todas as amostras foram medidas por ICP-OES. O resultado é um material com teores de silício de grau ultra-metalúrgico e excesso de B e P. Enquanto a caracterização do wafer foi estudada, uma extensa investigação foi realizada sobre o LeTID, que tem causas desconhecidas, no Institute for Energy Technology, Noruega. Os wafers vizinhos de mc-Si do tipo-p de alto desempenho foram testados em diferentes condições do processo de firing. Os efeitos foram investigados em termos de ativação de defeitos e uma correspondente degradação e recuperação no lifetime sob recozimento iluminado. Uma amostra com LeTID quase totalmente suprimido é mostrada. Um novo método foi proposto para separar os efeitos de Degradação Induzida por Luz relacionados ao Oxigênio e Boro do LeTID, permitindo até medir onde se pensava que estivesse totalmente suprimido. Novos modelos para formação e supressão de defeitos LeTID são propostos. Tanto a purificação de silício quanto a caracterização de degradação induzida pela luz nos estudos de mc-Si mostram uma ampla gama de pesquisas sobre novas rotas de produção que podem exigir processos personalizados de cristalização e fabricação de células solares, como gettering e firing.

Palavras-chave: 1. Silício Grau Solar. 2. Silício Multicristalino. 3. Solar FV. 4. LeTID.

LISTO F TABLES

Table 1 – Acceptable contamination (C) by impurities calculated for silicon feedstock, wafers and solar cells 36
Table 2 – Chemical specification for solar grade silicon. Data in ppm (weight), except the data followed by (a), which indicates ppm (atomic) 36
Table 3 –Target impurity concentrations in UMG and SoG silicon (all values in ppm_w) 38
Table 4 - Specification of the impurities contained in the solar grade silicon for the production of solar cells according to SEMI PV 49-0613. 39
Table 5 - Studies and data considered according to the manufacturing processes of multicrystalline silicon by the metallurgical route 61
Table 6 - Impurities data obtained by ICPOES; reference for metallurgical, ultra-metallurgical and solar grade silicon. 68
Table 7 - Impurities data obtained by ICPOES for: C - resulted magnesiumthermic silicon leached with HCl (25%) + HF (5%) (50ºC and 6 hours); D - the commercial carbothermic silicon leached with HCl (25%) + HF (5%) (50ºC and 6 hours); reference for ultra-metallurgical and solar grade silicon. 69
Table 8 – Measured resistivity, reflectiveness, mass and calculated thickness of the produced wafers by the different routes. Average lifetime was obtained with the PL equipment 74
Table 9 – Data from each firing profile and calculated maximum normalized BO-corrected degradation (LeTID representative) 100
Table 10 – Model B with LeTID triggering temperature for each firing profile, assuming when the thermal budgets above 600°C value reached 50°C.s. 113
Table 11 – Calculated rate of defect formation and the rate of emptying of LeTID defects reservoir, considered represented by the difference between maximum normalized BOcorrected lifetime degradations under illuminated annealing for each profile divided by the difference between thermal budgets above 600°C. 117
Table 12 – Results for profiles #5 and SBS compared with results from literature 122
Table 13 – Results for profiles #5 and SBS compared with results from literature that performed two sequential firing process with the same sample 123

LIST OF FIGURES

Figure 1 - A simple climate model to a pathway in which net CO_2 emissions (grey line) decline in a straight line from 2020 to reach net zero in 2055. The blue line is a response to a faster CO_2 emissions reduction, reaching net zero in 2040, reducing cumulative CO2 emissions. The purple line shows the response to net CO_2 emissions declining to zero in 2055 with net non-CO_2 forcing remaining constant after 2030 [2]. 1

Figure 2 - Evolutionary development of the electricity generation for the global energy transition from 2015 to 2050. The model is based on hourly resolution for an entire year, the world structured in 145 regions, high spatial resolution of the input RE resource data, and transition steps of 5-year Period. 3

Figure 3 - Evolution of global total solar PV installed capacity 2000-2017 3

Figure 4 -. Seasonal global solar avarage radiation of Brazil 5

Figure 5 - Daytime generation curve of a summer day, of February 2019, including renewable generation curves of hydro, wind and solar sources, fossil thermal and nuclear. a) Real daytime generation curves; (b) daytime generation curves with the hydro generation subtracted by the actual solar PV generation multiplied by a factor of ten (c) daytime generation curves with the hydro generation subtracted by the actual solar PV generation multiplied by a factor of thirty 7

Figure 6 – Schematic of a carbothermal MG-silicon reactor 13

Figure 7 - Metallurgical purification route from MG-Si to SoG-Si, the refining steps consists of a combination of metallurgical techniques 17

Figure 8- Schematic illustration of a directional solidification furnace 20

Figure 9 – (a) polycrystalline silicon bricks (b) polycrystalline silicon wafers 23

Figure 10 – Schematic drawing of a simple solar cell. The absorbed light creates electron-hole pairs, which are extracted at opposite the metal contacts 30

Figure 11 – Schematic drawing of a simple solar cell. The absorbed light creates electron-hole pairs, which are extracted at opposite the metal contacts 31

Figure 12 – Left: Schematic design of a passivated emitter and rear cell (PERC); Right: Schematic design of different rear surface passivation of crystalline silicon solar cells: (a) large area back surface field (BSF), (b) dielectrically passivated bifacial structure, (c) passivated emitter and rear cell (PERC), and (d) passivated emitter, rear locally diffused (PERL)-type cell 32

Figure 13 – Efficiency of the solar cell related with concentration of impurities 34

Figure 14 – Influence of the concentration of impurities on the diffusion length of minority carriers 34

Figure 15 – Metal impurities along the ingot produced by directional solidification 40

Figure 16 – The segregation of dopants and resistivity distribution in an ingot grown from compensated silicon 41

Figure 17 – Series resistance image of a multicrystalline Si cell performed on a BT Imaging LIS-R1 44

Figure 18 – Effective Lifetime of minority carriers from a Photoluminescence Image of a passivated multicrystalline Silicon wafer 45

Figure 19 – Bulk lifetimes of a multicrystalline silicon brick from a photoluminescence image normalized by doping and calibrated with QSSPC 47

Figure 20 – PL image taken on four as-cut mc-Si wafers: (a) a wafer from a center brick with few dislocations, (b) a wafer from a center brick with high dislocation density, (c) a wafer from the impurity rich area at the bottom and (d) a wafer from a corner brick with low dislocation density 48

Figure 21 – Left: average lifetime of intra-grain regions extracted from photoluminescence images in HPMC-Si wafers before and after gettering and firing. Right: harmonic average lifetime extracted from photoluminescence images of the same wafers 50

Figure 22 – Photoluminescence images of various mc-Si wafers selected before and after gettering and hydrogenation. The samples were double sided passivated. A logarithmic color scale is used in the figure. The wafer number of the bottom of the ingot and the corresponding fraction of the height of the ingot, based on the height of the ingot, are shown in the left column. 50

Figure 23 - Lifetime as a function of light exposure for a-Si:H passivated boron doped Cz-Si and FZ-Si 54

Figure 24 - Kersten et al [31] data, illuminated annealing (300W.m^{-2}) in mc-PERC cells at 50°C and 95°C; Voc and Isc mode 56
Figure 25 - Absolute change in effective minority carrier lifetime of mc-Si samples fired at various temperatures as the result of illuminated annealing 57
Figure 26 – Left: BO-LID dark anneal and accelerated light soaking cycles with three state model, observed in Cz-Si. Right: LeTID in mc-si dark anneal and accelerated light soaking cycles with state model including reservoir 58
Figure 27 – Sequential lifetime degradation curves in gettered and fired wafers from 39% height in the ingot. The BO-LID and the LeTID contributions to the total degradation are shown on the left and the right side, respectively 60
Figure 28 - purification route for carbothermic and magnesiumthermic silicon for this study. 62
Figure 29 - Process flow diagram investigating the effects of different Firing Furnace Conditions on LeTID. Wafers was separated in eight groups. 63
Figure 30 – (a) Firing temperatures profiles resulted for the seven groups of wafers that went through firing. (b) Peak temperature zoom in. 65
Figure 31 - PL images of as-cut, gettered and gettered + fired wafers with colored and gray lifetime scales from 0-600µs 71
Figure 32 – Average measured lifetimes with the PL equipment with calibrated by QssPC in as-cut, gettered and gettered + fired wafers. Colored scale PL images shows a selected wafer. 73
Figure 33 - One selected PL image for each firing profile. The image is color scaled, from 0 to 800ms. . 75
Figure 34 – Average lifetime measured with the PL equipment with calibrated by QssPC for each wafer and according to the firing profile. Colored scale PL images shows a selected wafer. 76
Figure 35 – (a) Measured lifetimes for the firing profiles from #1 to #6 and SBS. A blue dash line, serving as a guide for the eye; (b) QssPC lifetime measurements after a 20 minutes dark annealing related with increasing wafer number. 77
Figure 36 – a) ASC and firing process #5 illuminated annealing curves at 150°C, 80mW/cm², logarithmic timescale; b) same as (a) but linear timescale. 79
Figure 37 - Injection dependent lifetime curves, from a wafer from the firing profile #5 at different states using Sinton lifetime tester WCT-120TS. 81
Figure 38 - Degradation and recovery curves under illuminated annealing at 80 mW/cm² and 150°C on wafers fired with profiles #1, #2. #3. #4, #6 and SBS. Repeatability of the measurements is evaluated and wafer number is shown – "a" is the selected area of the wafer 83
Figure 39 – (a) Lower temperatures firing processes (#1, #2, #3, #4) and high temperature firing process (#6) illuminated annealing curves at 150°C, 80mW/cm², logarithmic timescale, compared with #5; (b) Lower temperatures firing processes (#1, #2, #3, #4) and high temperature firing process (#6) illuminated annealing curves at 150°C, 80mW/cm², linear timescale, compared with #5. 85
Figure 40 - (a) Slow Belt Speed illuminated annealing curve at 150°C, 80mW/cm², logarithmic timescale, compared with #1 and #5; (b) Same as (a), but linear timescale; letters "A" and "B" indicates two different recovery rates in the SBS curve. 87
Figure 41 - (a) Normalized τ/τ0 SBS, #1, ASC and #6 illuminated annealing curves at 150°C, 80mw/m²; SBS; (b) same as (a) but linear timescale. 89
Figure 42 - Low light intensity (5 mW/cm²) illuminated annealing curve at room temperature for 72 hours for BO-LID performed on a #5 sample (a) and on a SBS sample (b); the lifetime was approximately 60% and 51% of initial lifetime after 72 hours, respectively. 91
Figure 43 – Lifetime stability in 200 hours measurements in samples from SBS, #1, #5 and #3. In the first 24 hours, samples are under illuminated annealing at 150°C, 80mw/m². After 24 hours, the samples were subjected to the same illumination of 80mW.cm-², but at room temperature 92
Figure 44 – Lifetime stability in 1000 hours measurements in samples from SBS and #6. In the first 24 hours, samples are under illuminated annealing at 150°C, 80mw/m². After 24 hours, the samples were subjected to the same illumination of 80mW.cm-², but at room temperature 93
Figure 45 – Lifetime evolution after dark annealing (DA - 150°C) and illuminated annealing (IA – 150°C, 3.5 suns). SBS and #5 samples previously went through 24 hours at illuminated annealing and 1000 hours at RT and illumination. 94
Figure 46 – (a) Normalized curves for **τBOLID** considered as normalized #1 curve values (BOLID representative); **τmeasured** as #6 normalized curve values; and corresponding calculated #6

τBOcorrected (considered LeTID representative) at 150°C, 80mw/m² illuminated annealing; (b) same as (a) but linear timescale. 95
Figure 47 – (a) Normalized curves for calculated **τBOcorrected** for the groups #2, #3, #4, #5, #6 and SBS at 150°C, 80mw/m² illuminated annealing; maximum **τBOcorrected** degradation occurred at around 30 minutes for all presented groups; #5 and #6 minimum **τBOcorrected** were 0,4 and 0,3; #4 minimum **τBOcorrected** were 1; #2 and SBS minimum **τBOcorrected** were 2 and 4; (b) same as (a) but linear timescale. 97
Figure 48 – (a) Normalized curves for calculated **τBOcorrected** for the groups #2, #3, #4, #5, #6 and SBS at 150°C, 80mw/m² illuminated annealing compared with normalized **τBOLID**; (b) same as (a) but with a normalized scale from 0 to 1. 98
Figure 49 – (a) Normalized maximum degradation $\tau DEG(measured)$ under illuminated annealing for each group of samples related with peak temperature in firing process b) Normalized maximum degradation τDEG ($BO - CORRECTED$) for each group of samples under illuminated annealing related with peak temperature in firing process. 101
Figure 50 – Firing profiles from #1 to #6. Beginning of LeTID defects formation is signed with the blue arrow. The triggering temperature of 640°C is considered. 102
Figure 51 – (a) Firing profiles from #1 to #6. Beginning of LeTID defects formation is signed with the blue arrow. The triggering temperature of 640°C is considered. 103
Figure 52 – (a) Thermal budget for temperatures above 600°C for firing profiles from 1# to #6, the time scale is the time when temperature is higher then 600°C; (b) same as (a), including SBS profile. .105
Figure 53 – (a) Normalized maximum degradation τDEG ($BO - CORRECTED$) for each group of samples under illuminated annealing related with the calculated thermal budget in firing processes above 500°C; (b) Same as (a) but for thermal budget above 600°C; (c) same as (b) but linear scales; (d) same as (c) with a hatched area indicating the loss that the LeTID defect introduces in the material in a firing process with increased thermal budget 106
Figure 54 - Firing profiles from #2 to #6 related with the maximum normalized BO-corrected lifetime degradation, plotted in time. In this proposed Model A is considered that the thermal budget above 600°C is responsible for the increased formation of the defect and that the triggering temperature of the LeTID is fixed at 640°C. 109
Figure 55 –Model A for the formation of the LeTID inside the firing furnace. Firing profile #6 is related with the maximum normalized BO-corrected lifetime degradation. The LeTID trigerring point is at fixed 640°C, the thermal budget above 600°C is signed with the hatched area and the firing zones as Z1, Z2, Z3 and Z4 are indicated with different colors and different set temperatures. 112
Figure 56 - Model B for the formation of LeTID defects inside the firing furnace fro profiles #2, #3, #4, #5, #6 and SBS. Triggering temperature related to a thermal budget above 600°C of 50°C.s. 114
Figure 57 – Calculated rate of defect formation, considered represented by the difference between maximum normalized BOcorrected lifetime degradations under illuminated annealing for each profile divided by the difference between thermal budgets above 600°C, using data from Table 9. Rate of emptying of LeTID defects reservoir is considered equal to the rate between #5 and SBS. 118
Figure 58 – Model 1 for the emptying of the LeTID defects reservoir inside the firing furnace, considered as a function of the thermal budget above 600°C. 119
Figure 59 – Model 2 for the emptying of the LeTID defects reservoir inside the firing furnace, considered as begging after the cooling ramp pass through the LeTID triggering temperature. 121
Figure 60 – Simulated firing profiles according to the applicability of model 1 (a) or model 2 (b). As the zones of the firing furnace are fixed, to reach the proposed parameters for the firing profile, the speed of the belt is close to that of the SBS profile, of 260 $cm.min^{-1}$. Set temperatures for each zone of furnace are proposed values. The real repercussion of these temperatures in the profile are not regarded. 125
Figure 61 – Summary for the overall proposed LeTID defect mechanism for formation and emptying reservoir for the studied SBS sample. 127

SUMMARY

1 INTRODUCTION 1

1.1 Objectives 11

2 BIBLIOGRAPHIC REVIEW 12

2.1 From silica to solar modules 12

2.1.1 From Quartz to Metallurgical grade Silicon 12

2.1.2 From Metallurgical to Solar Grade Silicon 16

2.1.2.1 Silicon purification routes 16

2.1.2.1 Ingot production 19

2.1.3 From Ingot to Modules 22

2.2 Photovoltaic Basics, Fundamentals and Solar Cell Structures 26

2.2.1 Photovoltaic effect 26

2.2.2 Solar cell concept 26

2.2.3 Charge carrier lifetime 27

2.2.4 Solar cells designs 30

2.3 Impurities, characterization of c-Si and recombination sources 33

2.3.1 Impurities effects on c-Si solar cell performance 33

2.3.2 Characterization of solar grade Silicon 35

2.3.3 Characterization of impurities in c-Si ingots 40

2.3.4 Characterization techniques for c-Si ingots and wafers 41

2.3.4.1 QssPC Lifetime measurements 42

2.3.4.2 Photoluminescence Images 43

2.3.4.3 Series resistance measurements with PL 44

2.3.4.4 Lifetime measurements with PL 44

2.3.4.5 PL Calibration with QssPC 45

2.3.4.6 PL characterization of mc-Si Ingots and Wafers 46

2.3.5 Recombination Sources on mc-Si 48

2.4 Light Induced Degradation on silicon 53

2.4.1 BO-LID in P-type Cz-Si 54

2.4.2 BO-LID and LeTID in P-type mc-Si 55

3 MATERIALS AND METHODS 61

3.1 ICP-OES impurities measurements of Brazilian quartz, MG-Si and UMG-Si 61

3.2 Characterization of commercially available mc-Si wafers 62

3.2.1 Investigations on LeTID 63

4 RESULTS AND DISCUSSION 67

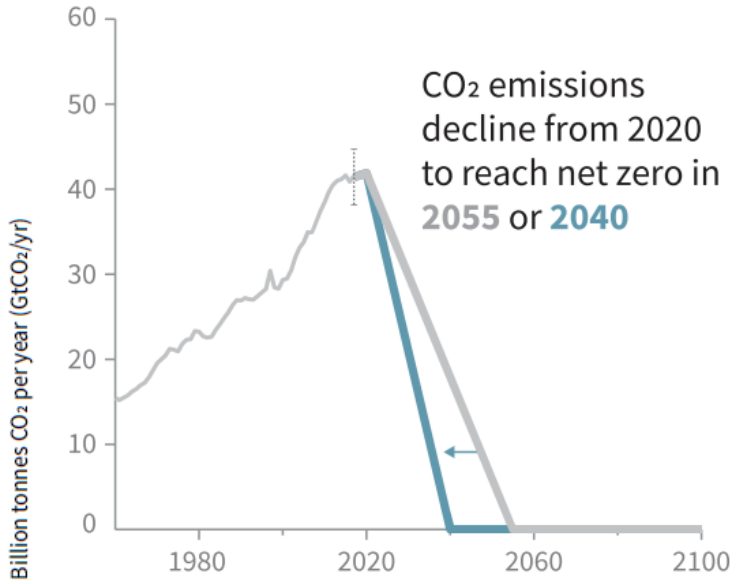
4.1 ICP-OES impurities measurements of Brazilian quartz, MG-Si and UMG-Si 67
4.2 Characterization of commercially available mc-Si wafers 70
4.2.1 Investigations on LeTID 73
4.2.1.1 PL images and QssPC measurements for each Firing Profile 74
4.2.1.2 Lifetime evaluation under illuminated annealing for different firing profiles 78
4.2.1.3 A method proposed for LeTID and BO-LID separation 94
4.2.1.4 The Firing Profile curves investigation on LeTID formation/suppression mechanisms 99
5 CONCLUSION 128
REFERENCES 130

1 INTRODUCTION

The continued cost reductions and the environmental benefits, aligned with global concerns about climate change, have made solar photovoltaic technology (PV) the most installed source of energy in the power sector worldwide [1]. The increasing investments in renewable energy are tracking more and more the global full potential of PV.

According to the special report on global warming impacts of 1.5°C from the Intergovernmental Panel on Climate Change (IPCC) [2], limiting global warming to 1.5°C would require rapid and far transitions in land, energy, industry, buildings, transport, and cities. The global net human-caused emissions of carbon dioxide needs to reduce to about 45% from 2010 levels by 2030, reaching 'net zero' around 2050. Figure 1 shows a stylized pathway from 2019 CO_2 emissions to a net zero emission in 2055 or 2040. These emission reduction paths would result in a higher probability of limiting warming to 1.5°C.

Figure 1 - A simple climate model to a pathway in which net CO_2 emissions (grey line) decline in a straight line from 2020 to reach net zero in 2055. The blue line is a response to a faster CO_2 emissions reduction, reaching net zero in 2040, reducing cumulative CO2 emissions. The purple line shows the response to net CO_2 emissions declining to zero in 2055 with net non-CO_2 forcing remaining constant after 2030 [2].



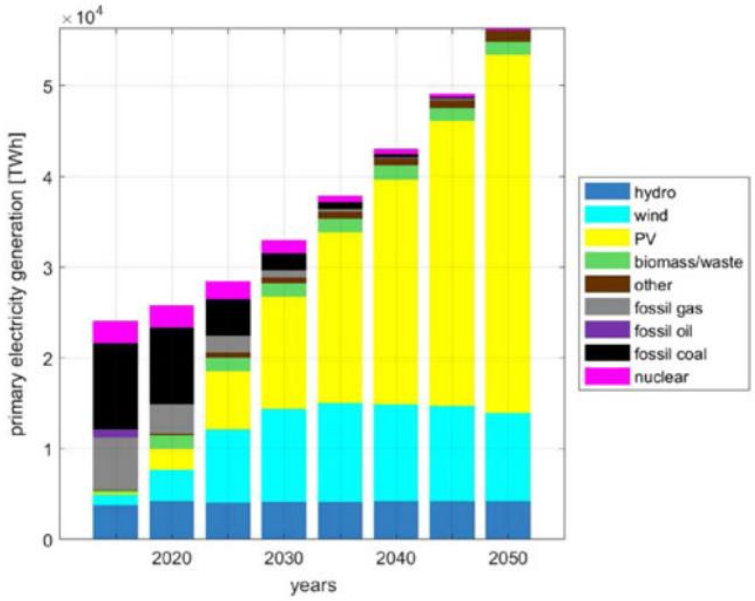
Source: IPCC [2]

The IPCC report on the impacts of global warming of 1.5°C [2] is part of the task to consolidate the Paris Agreement [3], which entered into force in November of 2016. The report forecasts 70–85% renewables for electricity supply in 2050. Any remaining emissions would need to be balanced by removing CO_2 from the air. According to C. Breyer et al. [4], a very deep decarbonzation towards 100% renewables in the power sector between 2040 and 2050 is possible, taking technical, economic, and societal constraints into account, and is the resulting least cost energy system with the greatest societal welfare, thus, providing energy system resilience. By using renewables, huge amounts of currently required subsidies for fossil fuels and nuclear risk are phased out. Carbon dioxide level is increasing in 2019, though. In May 2019, is expected to peak around 415 parts per million [5], mainly due to the persistent worldwide increased use of fossil fuels.

The power sector has the most potential to ensure the achievement of the Paris Agreement, since other sources of greenhouse gas emissions are even more difficult to phase out, such as from agriculture, cattle farming, industries, and parts of the transportation sector [4]. Electricity is evolving to be the basis of the energy systems in this century, due to high technical efficiency, comparable low cost, and the availability of respective power-to-heat, power-to-water, power to-hydrocarbons and a directly or indirectly electrified transport sector. Hydrogen production via solar photovoltaic-electrolysis is a simple and feasible technology [6] and a common view for the decarbonization of the transport sector [7], [8], [9].

In C. Breyer et al. [4] energy system transition model, solar PV and batteries will evolve as the most important power technologies globally, complemented by wind energy and mainly existing hydropower as shown in Figure 2. In addition, gas turbines are the most valuable and flexible balancing technology on a time scale of days to months and will gradually evolve from fossil to renewable gas. The cumulative PV capacity will hit 19 TW by 2050, representing 40% of world electricity production. About 30% of this capacity will be installed in homes or commercial rooftops, while the remaining 13.3 TW will come from large-scale systems, mainly single-axis tracking PV power plants on the ground, which will represent 0.3% of the earth's surface. About 50 TWh of storage capacity will handle the variable power generation. The continuous cost decline of solar PV and battery systems combined with excellently distributed solar resources and high modularity are main factors for the PV dominance.

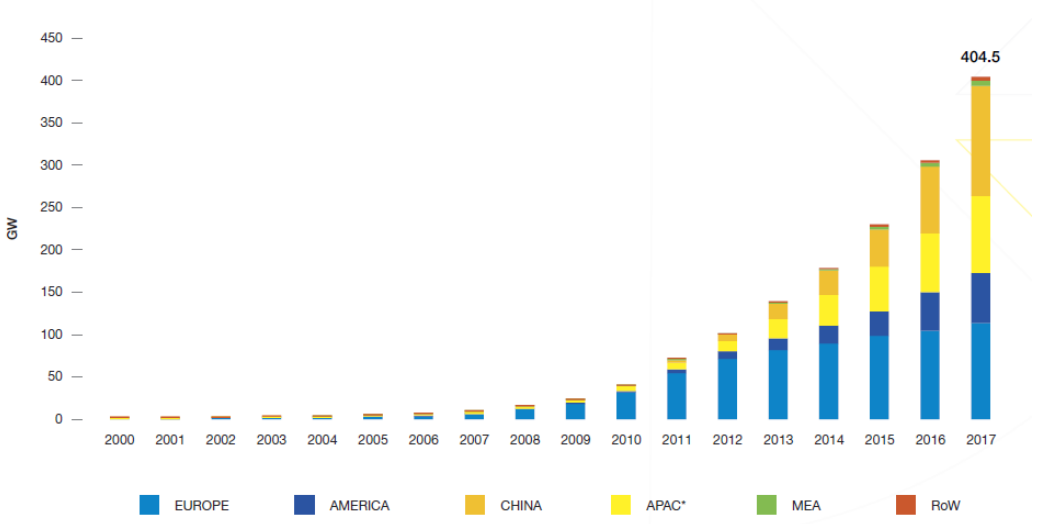
Figure 2 - Evolutionary development of the electricity generation for the global energy transition from 2015 to 2050. The model is based on hourly resolution for an entire year, the world structured in 145 regions, high spatial resolution of the input RE resource data, and transition steps of 5-year Period.



Source: C. Breyer et al. [4]

Photovoltaic solar energy has become the fastest growing power generation source in the world [1]. Figure 3 shows the growing of global total solar PV installed capacity from 2000 to 2017. In 2017, 98 GW were added to photovoltaic solar power generation capacity, thus surpassing the new installed capacity of new fossil fuels and nuclear combined. Once led by Germany, China promoted the rapid growing of the PV market. India and United States stand out as the next largest markets until 2022.

Figure 3 - Evolution of global total solar PV installed capacity 2000-2017



* APAC – Pacific Asia and Central Asia Excl. China
Source: Inrtersolar Europe

According to Intersolar Europe [1], in the reference scenario, between 2018 and 2022 is expected the addition of approximately 400 GW of new photovoltaic capacity worldwide. Even in OPEC future scenario with greater participation of fossil fuels in the energy matrix, the growth in demand for the use of photovoltaic solar energy is well established. OPEC World Oil Outlook [10] estimates that, by 2040, the global use of renewables, mainly PV and wind, is projected to be five times higher compared to 2015.

The solar photovoltaic industry has become a global giant, with an increasing production rate that, in 2018, was 100 GW per year. Further opportunities are expected in research, manufacturing, services and the corresponding development of energy systems, electric mobility and energy storage.

Accordingly to J. Jean [11], it is possible to achieve 25 TWp in photovoltaic capacity until 2050 without major material constraints. The total amount of key elements required to satisfy 100% of global electricity demand with today's wafer-based PV technology is up to 60 Mt of silicon. It would be enough to achieve just over the target of 69% of the global electricity generation proposed by C. Breyer [4]. Still, PV production technologies are rapidly becoming even more efficient, requiring less amount of feedstock per Wp of photovoltaic capacity. The recycling of silicon in silicon photovoltaic modules should also be further relevant within the passing years [12].

According to the Brazilian Ministry of Mines and Energy (MME) [13], Brazil has the largest know reserves of silicon in the world with approximately 78 Mt of quartz. Therefore, there is a huge potential in the exploitation of this resource with clear benefits to the local economy and global environment. To this end, a national technology for purifying and manufacturing silicon wafers for an increasingly competitive and efficient photovoltaic industry must be fully developed. Quartz is currently produced and exported by Brazil in the metallurgical grade. The transformation of this metallurgical grade silicon into solar and/or electronic grade requires a purification process that would add high value to the mineral [14].

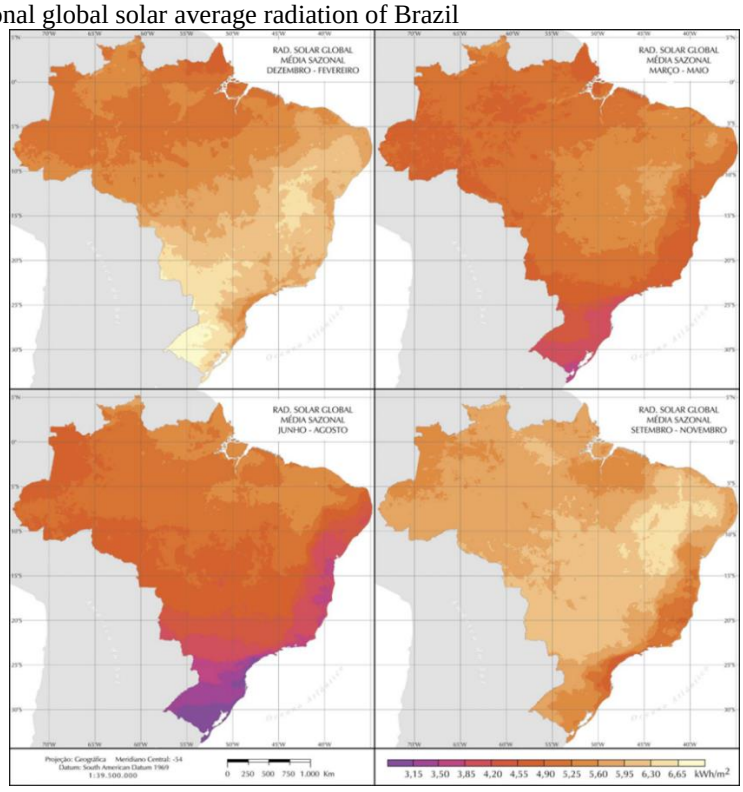
According to Brazilian national electrical system operator (ONS)[1], 71.8% of the energy generation in the National Interconnected System (SIN) in 2018 was hydroelectric, 16.7% thermal fossil and biomass, 8.3% wind, 2.7% nuclear and 0.5 % solar. The installed capacity of photovoltaic solar energy in December 2018 was 1,78

[1] www.ons.org.br

GW. Still, the potential positive impacts of the growth of PV generation in the national energy mix have not yet been fully studied and discussed.

The annual electricity peak demand in Brazil has been reported for the all regions in accordance with the thermal discomfort caused by heat waves during the afternoons [15]. The increased maximum instantaneous demand and a water scarcity scenario and power loss by depletion of reservoirs at the end of the dry seasons have required an increase in the consumption of fossil fuel sources for thermoelectric generation with high operating costs. An analysis on the demand side taking into account the solar supply shows that the implementation of photovoltaic solar energy in the southern region would cause greater impact in reducing the annual daytime peak demand among all regions. In December, January and February (Figure 4), the solar radiation levels in the south are the largest in Brazil and, in addition, exactly in this period, the region imports electricity from Southeast and Midwest regions. A large quantity of solar photovoltaic generation in the southern region will have a positive impact for the Brazilian electricity system. PV solar energy therefore has a reliable intermittence; it is a highly dispatchable source of energy if considering the characteristics of the electric energy demand in Brazil [15] and in several other countries [4].

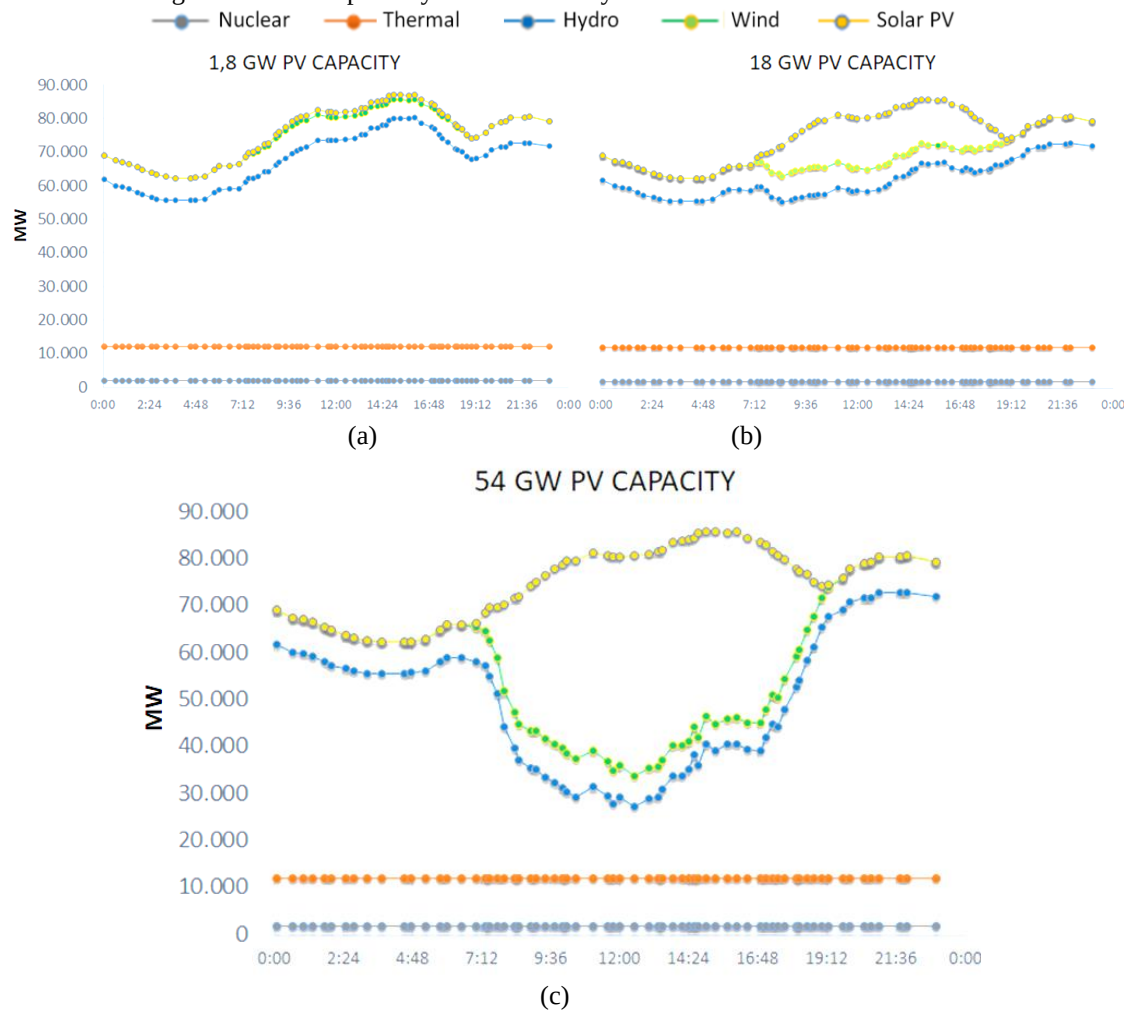
Figure 4 -. Seasonal global solar average radiation of Brazil



Soure: E. Pereira et al. [16]

In a changing paradigm of Brazilian electricity generation, which once used the hydro energy as the priority energy source and should then use it as a backup source [17], solar and wind power generation capacity should be dimensioned to act in synergy with the other renewable sources ensuring the progressive reduction in fossil fuels consumption and water supply. In Figure 5, one daytime generation curve of a summer day, of February 2019, is presented, including renewable generation curves of hydro, wind and solar sources, fossil thermal and nuclear. In Figure 5(a) is shown the real daytime generation curves, with a peak demand at around 3:40 pm (summer time). In Figure 5(b), the hydro generation is subtracted from the actual solar PV generation multiplied by a factor of ten. In Figure 5(c), the hydro generation is subtracted from the actual solar PV generation multiplied by a factor of thirty. It is possible to observe the impact that solar generation can provide for the national electricity system. With an installed capacity increase from 1.8 GW to 18 GW, PV become a “shield” for the daytime peak, and further to 54 GW, solar energy will mainly positively affect hydro generation, saving water from reservoirs during the day, improving the management of water supply.

Figure 5 - Daytime generation curve of a summer day, of February 2019, including renewable generation curves of hydro, wind and solar sources, fossil thermal and nuclear. a) Real daytime generation curves; (b) daytime generation curves with the hydro generation subtracted by the actual solar PV generation multiplied by a factor of ten (c) daytime generation curves with the hydro generation subtracted by the actual solar PV generation multiplied by a factor of thirty



Source: D. Knob, P. J. Knob and H. G. Riella [18]

According to the ONS[2], there were, in February 2019, 111 GW of installed hydro capacity, 30 GW of wind and 1.8 GW of solar PV. Peak demands on summer days are the highest of the year [15], at around 3:00 p.m. (summer time), where instant demand is close to 90 GW. With 0.5% of the energy generated in the day, solar photovoltaic generated 1.5% of the instant demand at peak time. Therefore, the highest load factor among the renewable sources in the peak time of the day, at 3:43 pm, is the solar photovoltaic, with approximately 80%, followed by hydropower, with 60% and wind with 20%.

[2] www.ons.org.br

According to C. Breyer et al. [4], photovoltaic solar energy can generate 63% of the demand for electric energy in Brazil in 2050. This corresponds to about 400GW of installed capacity, considering a conservative average annual global solar radiation in Brazil equivalent to 5.00 $kW.m^{-2}$. In PDE2027 plan [19], the Brazilian Energy Research Office (EPE) estimates that solar PV will reach a cumulative installed capacity of 21GW by 2027. In the report Distributed Energy Resources 2050, EPE and MME estimates 101GW of capacity from micro and mini distributed generation in 2050 in Brazil for the upper scenario. PV generation above 50% in the electricity mix by 2050 has not yet been stipulated comprehensively by the MME. Clearly, there is a potential for the solar energy in the Brazilian electricity system to be the largest share among all other forms of energy. All of this requires more ambitious planning from the Brazilian MME to ensure a fossil-free electricity sector by 2050.

In terms of material type, crystalline silicon (c-Si) PV modules accounted for 95% of the global annual PV market in 2017 [20]. There are two main categories: monocrystalline (mono-Si) and multicrystalline (multi-Si) [21]. Fine films accounted in 2010 for 13% of global production of PV modules [22] and for 4.5% in 2017 [20]. There are three main groups: amorphous silicon (a-Si) and microamorph (a-Si / μc-Si), Cadmium-Tellurium (CdTe), and Copper-Indium-Selenide (CIS) and Copper-Indium-Galium-Selenide (CIGS) [21]. New PV concepts aim to obtain ultra-efficient solar cells through advanced materials and/or new conversion concepts and processes such as advanced thin films and organic cells, PV Concentrator (CPV).

The most commonly used material in photovoltaic cells is multicrystalline silicon (multi-Si) [23]. Since 2005, multi-Si maintained relatively constant market shares [24] until 2009 [25], competing directly with mono-Si. From 2009 to 2016 it increased its share, but the trend stopped in 2017 [20], when mono technology started to grow relatively after manufacturers began switching towards lower processing cost and higher yield diamond-wafer technology while processing equipment suppliers began offering tools for low-cost high-efficiency cell designs [1].

The silicon crystallization market is dependent on the price of the raw material and the efficiency gap between the multi and mono crystalline silicon. Low prices favor the production of highly efficient monocrystalline silicon. However, new solar cell technologies continue to reduce the efficiency gap between the two. However, future cell concepts with increasing efficiencies favor the use of monocrystalline silicon. Nearly all mono cell lines in 2018 were capable of producing Passivated Emitter rear

Contact (PERC). The technology brings 0.5-1 percentage efficiency improvements with little more cost [1]. In the case of multicrystalline silicon cells, which is the target of the interests of this thesis, the LeTID (Light and elevated Temperature-Induced Degradation) is the specific object of investigations. Its causes remain unknown [26]. Understand and contain the LeTID is seen as essential, as is most evident and cause greater loss of efficiency in the PERC solar cell structure compared to its predecessor in the industry, the aluminum back surface field (Al-BSF). Avoiding LeTID for the p-type mc-Si is crucial for its survival in the future market for increasingly efficient solar cells.

The impact of impurities on solar cell and module performance increases for advanced cell architectures even for n-type substrates [27]. If the cell efficiency cannot be maintained, then the advantage of the feedstock low cost is lost due to quality degradation. Thus, is observed a raise in the demand for high quality quartz, specifically low in boron and phosphorus.

For photovoltaic solar industry, impurities concentrations for solar grade silicon (SoG-Si) are well below the concentrations of impurities found in metallurgical grade silicon (MG-Si). Therefore, purification processes of silicon metallurgical grade to ultra-metallurgical grade silicon (UMG) are necessary [28]. However, impurities for solar grade silicon may be at higher levels than the impurity levels required for electronic grade silicon (EG-Si). From the PV industry, the production of a less expensive and less pure solar grade silicon, adapted for the photovoltaic market, has emerged. For this end, the metallurgical route purification of silicon with less strict control of impurities enables the processing of solar cells with a satisfactory photovoltaic conversion efficiency. In addition, there are more metals impurities in multicrystalline Silicon compared with single crystal Silicon due to less pure coating and crucible materials, even with significant improvement by the materials suppliers. Still, the manufacture of multicrystalline silicon of high performance (HPMC-Si) is successfully done in the industry, and the object of investigations [29].

Typically, manufacturers of raw materials Solar Grade Silicon qualify their products by controlling contained chemical impurities. However, the electron activity of some impurities may be dependent on their chemical configuration or their physical distribution in the crystal (complexed with other impurities, dissolved in the matrix or agglomerated). These effects can be investigated by the electronic properties of the crystallized silicon and are therefore used as a measure of the quality of the raw material. Structural and electronic quality can be measured by optical inspection, lifetime, traps

density and by photoluminescence in silicon wafers [30]. The demands on quality control systems are growing in parallel with the PV market. Advanced characterization techniques play an important role in the offline characterization of samples at different stages of processing, which is indispensable for process optimization and material qualification.

The characterization and qualification of silicon wafers must take into account the main mechanisms of light-induced degradation in solar cells. The study on LeTID in multicrystalline silicon encompasses the understanding of steps subsequent to the manufacture of the wafers: gettering, passivation and firing or hydrogenation. The hydrogen contained in the passivation layers, despite deactivating various defects contained in multicrystalline silicon, can activate the LeTID defect, which will result in a loss of efficiency of the photovoltaic cell in the field that can reach 10% relative [31]. In partnership with the IFE of Norway, we have conducted a series of experiments to investigate the possible causes of LeTID, to understand the quality of the multicrystalline silicon used by the industry; the possible routes for deactivation of defects; and wafer characterization methods.

In Brazil, the promising photovoltaic market demand numerous initiatives that are being articulated to insert photovoltaic solar energy significantly in the country's energy mix. Keeping this in view, CCN of IPEN had the initiative in investigating the production of metallic silicon via magnesiothermal reduction and metallurgical route purification, qualified for the photovoltaic industry. This initiative requires a characterization of samples in different stages of production necessary for the validation of processes from quartz to wafer.

In this work, we perform an acid leaching in the material resulting from the magnesiothermal reduction, produced in IPEN, to form a MG-Si with relatively low impurities. The conditions of the acid leaching was taken from best results from the extensive work conducted by R. Ramos [32]. On more acid leaching step with HCl + HF in this resulting magnesiothermal reduced/acid leached material was proceed, using the conditions given in Ref. [33] aiming further purification of the MG-Si to a specific UMG-Si. In addition, the same HCl + HF acid leaching was performed in a commercially available Brazilian-made metallurgical grade silicon produced via carbothermal reduction. All samples impurities from each processing step, was measured by ICP-OES. The results was analyzed and compared to the state of art on literature [27]. We further conducted a study on BO-related LID and LeTID on mc-Si, in IFE, Norway. We used

neighboring HPMC-Si p-type wafers that were prepared and tested in different firing process conditions, i.e. different temperatures and furnace belt speeds. The effects of the different firing furnace conditions on subsequent LeTID was investigated in terms of defects activation and a corresponding lifetime degradation. An extensive investigation was taken on LeTID degradation and recovery mechanisms, seeking to eliminate or take more into account possible causes and solutions to suppress, partially suppress or overcame the defect. In addition, we have proposed a new method to separate BO-LID effects of LeTID during the characterization of the material, enabling to find and measure LeTID even where it was thought to be fully suppressed. The Tine Uberg Nærland et al. [34], [35], [36], Rune Søndenå et al. [37], [38], Tim Niewelt et al. [26] studies was the main references on LID to this thesis.

1.1 Objectives

Evaluation of silicon impurities after the reduction and purification processes and characterization of multicrystalline silicon wafers taking into account the main defect mechanisms such as LeTID.

Specific objectives:

- Analyzes different routes for the production of multicrystalline silicon wafers from quartz to ultra-metallurgical grade silicon,.
- Evaluation of impurities of the Brazilian solar grade silicon production,
- Investigate LeTID by wafer characterization after applying different Firing Furnace Conditions in commercially available p-type multi-Si wafers.
- Investigate possible causes and solutions to suppress, partially suppress or overcame the LeTID defect and a method to separate BO-LID effects from LeTID.
- Investigate metrics and propose models for the LeTID defect formation and suppression.

2 BIBLIOGRAPHIC REVIEW

2.1 From silica to solar modules

Silicon has been the dominant material in the photovoltaic industry and this is the trend for the coming decade [20], [1]. It is an abundant material that enables the projected growth of the PV installed capacity even in the most challenging scenarios of complete replacement of fossil fuels [11] in ever-growing electric power sector. In this chapter, a review of the manufacture of photovoltaic modules based on crystalline silicon, mainly the multi-crystalline silicon (mc-Si) is presented. The processing steps for the production of silicon-based photovoltaic modules from quartz can be divided into: production of metallurgical grade metal silicon; refining of metallurgical grade silicon via chemical or metallurgical routes to produce silicon grade solar; crystallization; wafer manufacturing; solar cell manufacturing; manufacturing of modules.

This work focus the bibliographic review on multicrystalline silicon material, manufactured via directional solidification from UMG feedstock. Multicrystalline silicon has a simpler, cheaper and less energy-intensive production. However, its survival on the PV industry must depend on constant advances in the conversion efficiency of photovoltaic cells produced with this material. For this, the LeTID, that is the most detrimental degradation seen in mc-Si PERC cells under the operating conditions of its photovoltaic modules in the field, must be overcome. This chapter will introduce the manufacturing process steps, therefore, especially for the multi-Si production and the implications of impurities from the feedstock and the contaminations within the processes.

2.1.1 From Quartz to Metallurgical grade Silicon

Quartz is one of the most abundant minerals [39]. It is found in nature in numerous forms [9]. The high purity quartz, for example, has become a strategic mineral with applications in high-tech industries [39] that include semiconductors, high temperature lamp tubing, telecommunications and optics, microelectronics and solar silicon applications.

The specifications used by producers of iron-silicon and metallic silicon in relation to Quartz are chemical and physical (particle size). The chemical criterion is related to the content of impurities, especially elements such as Al, Ti, B, P, Fe and Ca. A part of the nobler elements (e.g. Al and Ca), stays in metallurgical silicon, while the

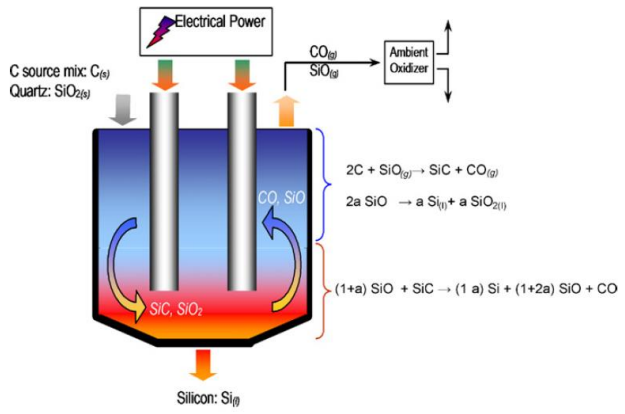
volatile components leaves through the exhaust system in manufacturing [41]. The requirements for very high-grade silica, low in iron, can be met where the iron content of the silica sand is naturally low or can be lowered sufficiently and economically through processing [42].

The most common and costless method of producing metallurgical grade silicon (MG-Si) is the carbothermic reduction of silica in a conventional electric arc furnace. Schei, Tuset and Tveit [41] provided a more comprehensive view of the chemical reactions and phases that occur in the process, as well as its commercial applications and other aspects related to this production route for metallic silicon. The reaction between SiO gas and carbonaceous materials are addressed by Myrhaug [43]. The carbothermal process is based on the reduction of quartz by carbon at temperatures above 1900°C, using coke, semi-coke or petroleum coke as a reducing agent. The carbothermic reduction reaction is in reaction (01):

$$SiO2(s) + 2\,C(s) \leftrightarrow Si(l) + 2\,CO(g) \qquad (01)$$

In industrial production, quartz chips with good purity, ranging in size from 10 to 100 mm, are usually used [44]. The load is heated by an intense electric arc supported between the tip of three submerged electrodes and the base of the electric furnace, as in Figure 6 [45]. The liquid silicon metal is extracted from the bottom of the oven and mixed raw materials are loaded on top. The gases escape from the top and quickly react with oxygen in the atmosphere. One of the main parameters, affecting the final yield of carbothermic process, is the quality of quartz raw material [19].

Figure 6 – Schematic of a carbothermal MG-silicon reactor



Source: S. Ranjan et al. [45]

Metallurgical silicon can also be produced through a metalothermic reduction. The chemical treatment consists of the reduction of a mineral substance (oxide or halide) by the use of a metal as a reducing agent as in reaction (02),

$$MeX + Me' = Me + Me'X, \quad (02)$$

where MeX is the oxide to be reduced, X may be: oxygen, chlorine or fluorine, therefore an oxide or a halide, Me' is the reducing agent, Me is the reduced metal and Me'X is the oxide formed through reaction [46]. The advantaged of this process is that Me'X product does not present itself in the gaseous physical state. Yet, the metalothermic reduction is commonly employed when the metal to be extracted has a strong tendency to form carbides by the carbothermic reduction operation.

The metalothermic reduction is usually exothermic. The greater the affinity of the reducing agent for oxygen, the more exothermic will be the reaction. Reactions can only be completed with an initial ignition. When the melting point of the metal produced is high, the reaction product is in the form of a solid 'porous' agglomerate, bringing all the components together [46]. Among the available metalothermic reactions, the metals that can reduce silicon oxide to metallic silicon are Ti, Al, Mg and Ca. The most indicated are Mg and Ca because of the value and ease of solubilization of the formed oxide [32]. Ti has a high market value. Aluminum reduction, on the other hand, has the disadvantage of forming of mullite ($Al_6Si_2O_{13}$) and Al^2O_3 as reaction products, both difficult to leach [27].

The magnesiothermal reduction process is based on the Mg in gaseous form reducing the quartz forming Si and MgO. This reaction occurs between temperatures of 400 and 1000°C. The reaction is expressed by (03) [47],

$$SiO_{2(s)} + 2Mg_{(g)} \leftrightarrow 2MgO_{(s)} + Si_{(s)}. \quad (03)$$

Intermediate reactions can occur in the initial stages, with the formation of Mg_2Si (magnesium silicate). This by-product also reduces silica according to reactions (04) and (05) [47],

$$SiO_{2(s)} + 4Mg_{(g)} \leftrightarrow 2MgO_{(s)} + Mg_2Si_{(s)} \quad (04)$$
$$\Delta G^o \ (900\ ^oC) = -308{,}5\ kJ/mol$$

$$Mg_2Si_{(s)} + SiO_{2(s)} \leftrightarrow 2MgO_{(s)} + 2Si_{(s)}. \quad (05)$$
$$\Delta G^o \ (900\ ^oC) = -181{,}8\ kJ/mol$$

The excess of the Mg reagent in the reduction further produces the Mg2 Si phase through the consumption of elemental silicon according to reaction (06) [47],

$$Si_{(s)} + 2Mg_{(g)} \leftrightarrow Mg_2Si_{(s)}. \quad (06)$$
$$\Delta G° \ (900\ °C) = -63{,}4\ kJ/mol$$

The phases formed during the magnesiothermic reduction indicate the possible species that need to be leached [32]. The leaching process involves the dissolution of one or more solid reagents from a matrix or the matrix itself (often porous), using a solvent which may be acidic or basic, i.e., leaching agent. A numerous parameters can directly influence the speed and yield of the process: particle size; porosity of the solid; solvent; temperature; shaking [32].

The overall dissolution process is controlled by the chemical reaction in the surface of the material according to (07) [48]:

$$MgO_{(s)} + 2H_{(aq)}^{+} = Mg_{(aq)}^{2+} + H_2O_{(l)}. \quad (07)$$

The chemical reactions in the surface involve the transfer of magnesium cations and oxygen anions from the solid to the solution in which the cations will be hydrated. The transfer of anions will involve protonation or hydroxylation reactions, on the surface of the solid, to form water [48].

R. Ramos [32] studied this hydrometallurgical technique called acid leaching, which was evaluated to reach to a valid method for dissolution of MgO by HCl while at the same time refine the silicon. A metallic Si with 99.66% purity was obtained, which is higher than common metallurgical grade material, but yet with high rates of Boron. The study found an optimum point in the acidic leaching, which is 3M HCl, 50ºC and 60min.

Metallurgical grade silicon has an average of 98 to 99.5% Si and, as impurities, about 1200 ppm of aluminum, 4000 ppm of iron, 1600 to 3000 ppm of calcium [44]. The levels of boron and phosphorus are not controlled, but are generally in the range of 20 to 60 ppm. This silicon is the feedstock material for the refining processes to obtain solar grade silicon (SoG-Si). MG-Si is contaminated with trace elements of metals such as Fe, Al, Ti, V, B and P and compounds like SiC, SiN, and SiO2, for example [19].

The metallurgical grade silicon from the carbothermic reduction of silica in electric furnaces is available in the market with a typical purity of 96 to 98%, and can reach up to 99.5% [44].

2.1.2 From Metallurgical to Solar Grade Silicon

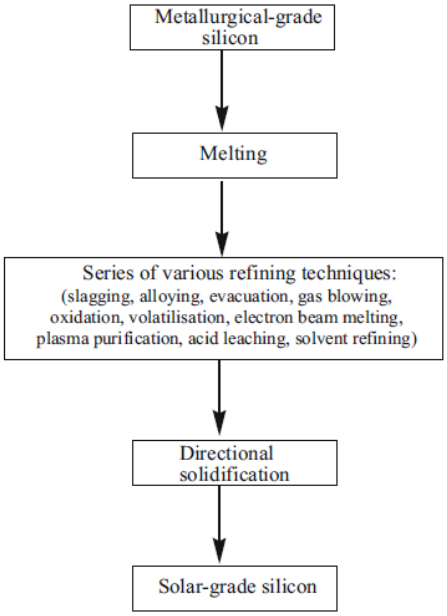
The silicon feedstock with an acceptable purity level for the production of PV module is referred to as solar grade silicon (SoG-Si). SoG-Si is generally less pure than the polysilicon used for the electronics industry. The silicon crystallinity derived from the reduction processes does not provide sufficient lifetimes for electronic devices such as solar cells and integrated circuits. The so-called lifetime is one of the most important material parameters for the silicon solar cell [24]. It describes the average time that the minority carrier takes to recombine and defines solar cell output parameters such as maximum voltage and current. Refining and crystallization techniques aim to provide a silicon crystal with high lifetime and consequently high photovoltaic conversion efficiency.

2.1.2.1 Silicon purification routes

There are two main methods for producing solar-grade silicon, the metallurgical and the chemical routes. Purification techniques using the chemical route in a first step are the creation of silane gases (SiH) and, in a second step of a deposition process using the Siemens process or the process by a fluidized bed reactor [24], both applied on a large scale in the industry. Metallurgical purification route and compensation processes are alternatively used to achieve solar grade purity. This route advantages are the reduced cost and energy consumption, complexity and operational problems related to the chemical route.

The metallurgical purification route consists of a combination of metallurgical techniques, as shown in Figure 7 [49]. A single metallurgical refining process is commonly not sufficient to lower the impurity level to solar-grade silicon specifications due to the presence of numerous impurities with different chemical and thermodynamic properties.

Figure 7 - Metallurgical purification route from MG-Si to SoG-Si, the refining steps consists of a combination of metallurgical techniques



Source: F. Chigondo [49]

The refining process consists of several refining steps, each one responsible for lowering a certain number of impurities to finally meet the purity requirements. The techniques include slagging, gas blowing, evacuation, formation of volatile species and oxidation of impurities, zone refining, electron beam melting, acid leaching, plasma, alloying and solvent refining, crystallization and directional solidification [49]. These refining steps can also be described as ultra-metallurgical grade silicon (UMG-Si) manufacturing processes. UMG-Si is therefore considered as further purified MG-Si, to average purity levels of 6N [27]. The advantage to improve metallurgical processes to achieve an acceptable purity level for PV production is to avoid the need for the costly chemical purification processes.

The hydrometallurgical process, acid leaching, is one of the possible steps of refining to upgrade the metallurgical grade silicon and it is the subject of numerous studies that seek efficiently removing of impurities from silicon [50], [51], [52], [53], [33]. This process is also relevant to a range of applications besides solar PV. F. Ebrahimfar and M. Ahmadian [33] investigated the effects of hydrochloric acid, hydrofluoric acid, sulfuric acid, nitric acid in combination with each other as a solvent for purification of MG-Si, and the effects of temperature and particle size of MG-Si. The results indicated that the highest purity of MG-Si was achieved by an HCl (25%) + HF

(5%) acid leaching. A particle size of 53µm, a temperature of 50°C for 6h resulted in high efficiency and purity (99.96%) of MG-Si.

Directional solidification is the key process in the metallurgical purification route as it removes most of the impurities with low segregation coefficients. The segregation coefficient is the ratio of an impurity in the solid phase to that in the liquid phase [49]. Impurities with high segregation coefficients like P (0.35), B (0.8) Al (0.3) and C (0.05) are removed by the other techniques.

Several refining routes are chosen depending on the manufacturer [27]. In Photosil process, the silicon purification is vertically integrated, from the selection of raw materials for the metallurgical silicon to the crystallization of multicrystalline Ingots using purified UMG solar silicon [54]. The drastic selection of the raw materials (quartz, wood, charcoal, etc.) allows producing a metallurgical silicon with a relatively low boron and phosphorus contents. After the quartz reduction in an electrical arc furnace process, the liquid of metallurgical silicon is poured into a vessel for a metallurgical segregation to remove mainly metallic impurities and a part of phosphorus. The obtained silicon is called UMG-1, which is melted in an induction furnace and subjected to a second segregation process. The so obtained solid UMG-2 silicon is then purified in an induction furnace, with an argon plasma gas with O_2 and H_2 as reactive gases able to volatilize impurities with large segregation coefficients such as B, C, Al, etc. The purified silicon is rapidly solidified preferentially in a directionally way to lower again the total amount of impurities. Due to the oxygen introduced into the plasma, and the use of a graphite crucible, the silicon is contaminated by oxygen and carbon. An average solar cell conversion efficiency close to 15% was obtained with this material, which is very sensitive to LID, showing an efficiency loss exceeding 1% absolute in certain cases [54].

Elkem process involves pyrometallurgical refining by adding a calcium containing compound to molten silicon [27]. The steps are: smelter for MG-Si production; slag treatment to remove B; acid leaching to reduce P and other metallic impurities; directional solidification for further removal of impurities; and post treatment by cleaning the bricks with acids [55], [56].

The State University of Campinas (UNICAMP) developed a study using electron beam melting principle that consists in the generation of a beam of free electrons that are accelerated towards a target conductor such as a metal [57]. An interaction occurs at the point of action of the beam with the atoms of the material, converting the electron beams kinetic energy into other forms of excitation energy. It is a high vacuum

processing, which allows the elimination of elements whose vapor pressures are higher than that of silicon and uses a refrigerated copper crucible, which does not contaminate the silicon. A 99.9995% purity silicon is obtained.

Ultrapure quartz and carbon black enables the possibility of direct carbothermic reduction followed by unidirectional solidification, which is studied by SOLSILC and SPURT projects. This process consumes four times less energy than Siemens process. The residual carbon in the final product originated from the reduction process is a disadvantage [57].

2.1.2.1 Ingot production

The crystallization step, or the ingot production, can also be considered the last silicon-refining step. Subsequent steps such as gettering further moves impurities to grain boundaries while the firing step passivates defects by hydrogenation. Thus, there are impurities that can still be removed, overcame or passivated from the silicon ingot after crystallization.

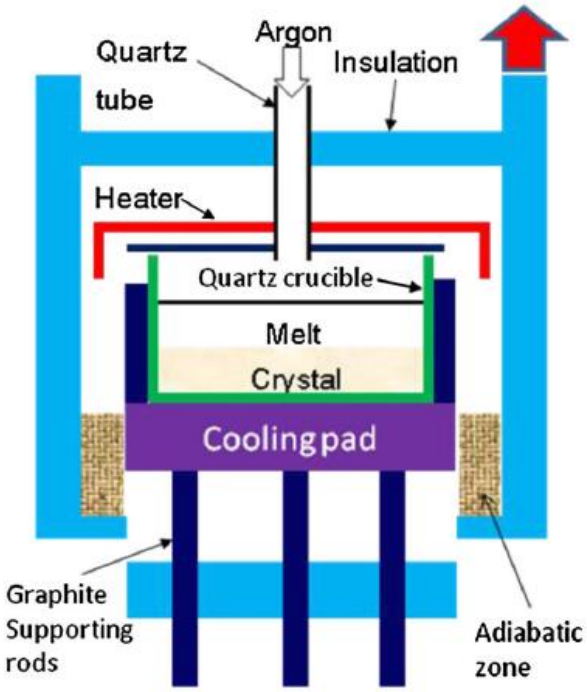
During crystal growth, the impurity profile and material quality are significantly affected. New impurities are introduced, and existing impurities are redistributed [27]. One of the challenges in the photovoltaic industry is the improvement in the quality of the silicon ingot during the growth process, especially in the directional solidification method (DS) [58], [59], [60]. Thermal effects, impurities, rotation speed, heat zone design and others affect crystal quality, resulting in stress, point defect, twins, dislocation, and grain. Impurities and grain boundaries can combine to create defect lusters. The effects of impurities and defects are specially convoluted with feedstock and solar cell manufacturing [27].

The Czochralski method is one route of silicon crystallization. It consists of manufacturing a large cylindrical block of monocrystalline silicon (mono-Si or Cz-Si), minimizing crystalline defects [24]. Quartz with high purity polysilicon and calculated amounts of B or P dopant is melted into an amorphous silica crucible with a crystallographic oriented single crystal seed [27].

The directional solidification of silicon is another silicon crystallization method, which results in the multicrystalline silicon (mc-Si) material. Silicon is feed into a silica crucible and gradually solidified so that metal impurities with a low coefficient of segregation, such as Fe, Al, Ti etc., segregate into the liquid phase and concentrate in the last solidified part. This last part is then discarded, as well as the part in contact with the

crucible, contaminated by oxygen from silica [61]. The contamination as well as the oxygen content in the metal can be reduced if the solidification is carried out under vacuum. The schematic of the DS system is shown in Figure 8 [62]. Typically, crystallization begins at the bottom of the crucible, reducing the temperature below the melting temperature of the silicon (1412°C). The heating zone is slowly moved upward so that the liquid silicon is always above the ingot, the top area being the last to solidify at the end of the process. Crystallization is controlled by displacement of the temperature gradient [61].

Figure 8- Schematic illustration of a directional solidification furnace



Source: Y. M. Yang [62]

Single crystal silicon (sc-Si) grown by the Czochralski method is essentially dislocation free, while the mc-Si inherently has grain boundaries and dislocations. The dislocations multiply driven by the thermal stress generated during solidification and expansion stress due to the rigid crucible [62]. In addition, there are more metals impurities in mc-Si compared with sc-Si due to less pure coating and crucible materials, even with significant improvement by the materials suppliers. Overcoming structural imperfections that affects final solar cell performance, such as high dislocation densities, random crystalline orientations, electrically active grain boundaries, grain boundaries

with parasitic impurities such as metals, silicon nitride, silicon carbide, etc., is the main objective for the further technology development of directional solidification [29].

There are crystallization processes that do not provide perfect single crystal silicon blocks, but seek a good quality material and a high yield of the process. The production of ingots where a fraction grows as monocrystalline (mono-like) by the addition of monocrystalline seeds tiled at the bottom of the furnace crucible. However, concerns regarding an increase in the density of dislocations in ingots of the so-called mono-like persisted [63]. The mono-like was gradually replaced by the high-performance multi-crystalline (HPM) silicon, which consists of small-grain mc-Si ingot grown on incubation Si seeds with fine grains, which results in smaller dislocation clusters than observed in mono-like Si ingots [64] .

The High-performance multi-crystalline (HPM) silicon wafers became a dominating product on the photovoltaic market as they ensure significantly higher conversion efficiency and power output of solar cells and solar modules in comparison to conventional multi-crystalline silicon products and mono-like, while utilizing the same equipment and method of directional solidification [29]. HPMC-Si final material properties is characterized by small grain sizes, high quantities of random grain boundaries, low densities of dislocation clusters and shortly dislocation clusters [65]. The improved performance of HPMC-Si material is noticed even with no upgrades of solar cell or solar module designs [29].

Controlling grain boundaries and dislocations is necessary to ensure the ingot quality in DS. Y. Yang et al [62] found that through nucleation and grain control, is possible to mitigate the multiplication of the dislocations. The small initial grains and the high percentage of non-coherent grain boundaries seemed to be beneficial to the stress relaxation during ingot growth. G. Stokkan et al [65] proposed that the decisive mechanism for the reduced dislocation density is the termination of dislocation clusters during growth by the interaction with random angle grain boundaries. T. Hiramatsu et al [66] confirmed that simple temperature modification with heat insulators is effective for controlling the nucleation sites and growth direction of dendrite crystals.

I. Buchovska [29] has shown that seeding a high-purity polycrystalline silicon chunks produced by Siemens method can be successfully used in directional solidification with cheaper feedstock of lower purity. Two ingots were grown in an industrial DS furnace using the same high-purity poly-Si seeding process. Siemens polycrystalline silicon was utilized as feedstock for the first ingot and a cheaper solar grade silicon for

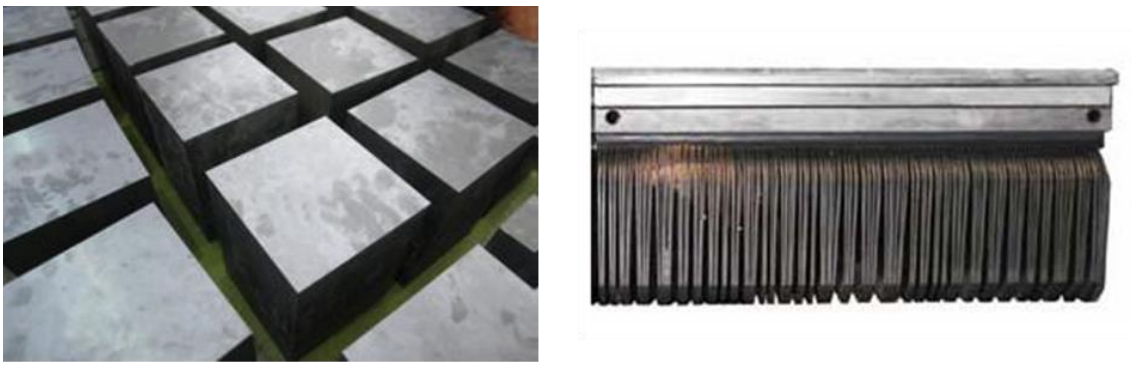
the second. The second process was not optimally adjusted for SoG-Si in respect to melting features, cycle time for seeding and crystallization behavior due to higher impurities content. The first ingot resulted in an average conversion efficiency of the solar cell of 18.46% while the second, 18.29%. A previous experiment with heterogeneous nucleation on a rough silica crucible bottom using only fine polycrystalline silicon as feedstock followed by a slightly different cell manufacture process, showed a smaller resulted average conversion efficiency of only 18.08%. With these results, a potential way for cost reduction of HPMC-Si material was given, even more when combined with adapted solar cell manufacturing processes.

2.1.3 From Ingot to Modules

After crystallization, the crystallized silicon ingots are cut into bricks and then cut into wafers, which are then used in the manufacture of solar cells [24]. Most bricking and wafering tools use wire saw machines in suspension slurry. Other techniques, however, uses diamond wires for both bricking and wafering.

The top and bottom of the ingot are cut and reinserted in the crystallization process. After this, the ingots are cut into bricks with typical dimensions of 400 to 500 mm (Figure 9,a) and are then loaded into the wafers cutting machine (Figure 9, b). In this wafering process, a single stainless steel wire of typically 180 μm in diameter and kilometers in length is moved in a suspension of abrasive paste and passes through the brick. Approximately 30% of the silicon is lost as dust [67]. The wafers standard dimensions are 156 x 156 mm, 120 μm thick.

Figure 9 – (a) polycrystalline silicon bricks (b) polycrystalline silicon wafers



(a) (b)

Source: Meyer Burger Technology AG[3]

Despite the rapid progress in wafer manufacturing, it is still under intense development, mainly driven by choosing the cutting technique of the future - diamond wire or abrasive. Other objectives such as cost reduction and thinner wafers are also being investigated [68]. The main challenges on wafer production consist of reduction of kerf loss and kerf fine recycling, lowering cost, thin wafers handling and processing, unified incoming wafer specifications and standards [27].

The wafer surface needs to be cleaned in order to remove the organic contaminants from the c-Si wafer surfaces. This can be proceed ultrasonically at room temperature (RT) with a 12% NaOCl solution for five minutes. The surface damages on wafers can be removed through isotropic etching with a concentrated solution of NaOH in de-ionized water. The surface texturing can be performed by asymmetric etching of front surface of the wafers, in a dilute alkaline solution [69].

In p-type Si solar cell processing, the n–p junction is formed by high concentration P in-diffusion from a gaseous, liquid, or solid source [70] that leads to formation of n-type emitter at the top surface of the wafer [69]. Fast diffusing metal impurities, such as iron, nickel, and copper from silicon feedstock material or introduced, during ingot growth and solar-cell processing, can be gettered from grains with low-dislocation densities, increasing the minority carrier lifetime in these regions [71]. However, the average effective lifetime has still been observed to decrease in the central region of a silicon block of industrial quality material with initially low impurity levels, which can be related to strong activation of recombination at the grain boundaries after

[3] www.meyerburger.ch

gettering [72]. In regions with high dislocations clusters, the gettering process is minimally effective, meaning that the impurity gettering cannot overcome the limits imposed by the crystallographic defects in high dislocation densities areas [73]. Dissolved metal point defects or metal-silicide precipitates may segregate to the dislocation strain field and/or bind to the dislocation core, creating deep-level recombination centers that are additional energy barriers to gettering and detrimental to solar-cell performance [71].

Light reflection as well as electronic defects at the front surface are strongly minimized with an anti-reflection coating (ARC) by Plasma-enhanced chemical vapor deposition process (PECVD), depositing a thin hydrogenated SiNx layer that passivates the silicon surface [69].

The firing process promotes the contact formation between the screen-printing of silver paste and the bulk silicon surface by penetrating the ARC. This is a well-established process for forming front and rear electrodes [74]. This firing temperature profile requires a drying step with temperatures below 400 °C, a step with temperatures between 475 and 600 °C that melts the glass frit and sinters the silver, and a short spike with a temperature between 600 and 900°C. During the contact firing, the concentration of dissolved iron in the wafer bulk is increased, decreasing bulk lifetime [75].

Gettering and firing are the main processes used to reduce the impact of defects and improve the performance of mc-Si materials in the solar cell manufacturing [71]. However, the atomic hydrogen in-diffusion, from a SiN*x*:H coating layer, during the firing process shows a less effective lifetime improvement as dislocation density increases. Therefore the importance of removing dislocations sizes and quantity to further improve mc-Si solar cell performance.

A crystalline silicon solar cell outputs a voltage of about 0.5 volts. Therefore, individual cells are generally interconnected to produce an effective voltage for practical application. In addition, the interconnected solar cells are encapsulated for protection, and a solar module is produced. The solar module can be used directly for electricity generation or be incorporated into the photovoltaic systems [76].

The last defect that can be observed on c-Si solar modules in field operation conditions is the light induced degradation (LID). LID can be affected by feedstock quality (impurity concentration); base resistivity and net doping; and by numerous steps in the manufacturing process such as crystallization (defect and doping distribution), wafering and cleaning (surface contamination), cell process (defect diffusion, gettering

effects), passivation and cell design [27]. LID mitigation is increasingly relevant to the new high efficiencies cell structures [77]. Boron oxygen related LID (BO-LID) is commonly the most detrimental LID seen in Cz-Si [35] and Light and elevated Temperature-Induced Degradation (LeTID), in mc-Si [26].

2.2 Photovoltaic Basics, Fundamentals and Solar Cell Structures

The solar photovoltaic energy generation takes place through a solar cell, designed to take advantage of the photovoltaic effect in the semiconductor materials, transforming light directly into electric energy. The mostly used material is Silicon. The photovoltaic effect, the solar cell concept, the charge carrier lifetime and the solar cell designs are discussed in this chapter.

2.2.1 Photovoltaic effect

The photovoltaic effect is explained by a quantum theory [78]. There are two bands of energy in semiconductors that electrons possess the valence band and the conduction band. The bands are separated by a range of energies called band-gap, which electrons are not allowed to have. Photons are considered as package of energy and depends on the frequency of the light, which can, for example, be detected by the human eye in the form of colors. The photons from a specific fraction of the light spectrum has a higher energy then the band-gap. The electrons excited by this photon can be conducted from the valence band to the conduction band where they are free to move. An excited hole therefore appears in the valence band.

2.2.2 Solar cell concept

The solar cell architecture uses the electronic respond of semiconductors to the photovoltaic effect in order to convert the sunlight directly into electricity. To do so, the excited electron in the conduction band and the excited hole in the valance band needs to be forced into opposite directions by negatively doping one side, for example, of a positive doped silicon forming a p-n junction. The silicon is a four-valent element. The boron is a three-valent element. When silicon is doped with boron, mobile holes are created in the substitutional boron dispersed in the crystalline silicon structure, which is called p-doped, or p-type. Phosphorous is a five-valent element and creates an excess of electrons, thus, forming a negative doped material, or n-type. The electrons from n-type layer diffuse through the junction to the p-type layer, leaving behind a narrow layer positively charged due to the lack of electrons. Holes diffuses in the opposite direction, leaving a layer negatively charged. The resulting p-n junction is a depletion region with an electric field creating a barrier against a further flow of electrons and holes, actually forming a so-called rectifying diode. If electrodes/contacts are placed on oppose sides of

the electric field, electricity can be produced when the photons from sunlight have enough energy to create electron-hole pairs [34].

2.2.3 Charge carrier lifetime

In doped material, there is an excess of one type of carrier, holes or electrons. This carrier in high concentration is called majority carrier. There is, although, always a low concentration of holes in the material type with excess of electrons (n-type). Equally, a low concentration of electrons is still present in the material type with excess of holes (p-type). This carrier in low concentration is called minority carrier. When light exposure generates carriers, the excess carrier concentration is given by the balance between generation of electron-hole pairs and recombination of annihilation of the pairs. In constant temperature and in dark, a solar cell is at thermal equilibrium where the density of electrons and holes is constant. Under illumination the total number of minority carriers, electrons, in p-type Si increases (same for holes in n-type Si), given by (08) [34]:

$$n = n_0 + \Delta n \tag{08}$$

where n is the number of electrons; n_0 is the initial number of electrons; and Δn is the excess minority carrier concentration often referred to as injection level. Excess minority carriers will eventually recombine, giving its energy and falling back to the valence band, eliminating a hole. If the excess minority carrier concentration is divided by the rate of its recombination (R), the minority carrier recombination lifetime (τ_n) is obtained, as in (09):

$$\tau_n = \frac{\Delta n}{R} = \frac{\Delta n}{\frac{d\Delta n}{dt}} \tag{09}$$

The rate of carrier generation (G) minus the recombination rate (R) gives an electron continuity expression, as in (10):

$$G - \frac{d\Delta n}{dt} = \frac{\Delta n}{\tau_n}. \tag{10}$$

By rearranging, the lifetime is obtained (11):

$$\tau_n = \frac{\Delta n}{G - \frac{d\Delta n}{dt}}. \quad (11)$$

which is considered as the basis for measuring effective lifetime: when the external generation source is removed, the excess carrier will recombine and the excess carrier density as a function of time will be given as in (12):

$$\Delta n(t) = \Delta n_0 \exp\left(-\frac{t}{\tau_n}\right) \quad (12)$$

where $\Delta n_0 = G\tau_n$, that is, the excess carrier density before the removal of external generation [34].

The inverse measured effective lifetime τ_{eff} is given by the inverse sum of the individual lifetime contributions from different recombination sources as in (13) [34]:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{rad}} + \cdots \quad (13)$$

where τ_{Auger} is lifetime limited by the Auger recombination; τ_{SHR} is the lifetime limited by the Shocley Read Hall (SRH) recombination and τ_{rad} is the lifetime limited by the radiative recombination. Those are the main physical mechanisms sources of recombination [79]. The occurrence and strength vary with the carrier injection level.
The radiative recombination is weak and often neglected in silicon material. Auger Recombination is an electron and a hole recombination which gives the excess energy to a second electron or hole instead of emitting light [80]. This second electron then thermalizes back down to its original energy. Auger recombination ultimately limits the lifetime and efficiency, it is although more relevant at high carrier concentrations caused by heavy doping or high-level injection.

The Shockley Read Hall recombination is related to defect concentrations such as impurities. The defect concentration is directly related to the lifetime as in (14):

$$\tau_{SRH} = \frac{1}{v_n \sigma_n N_t} \quad (14)$$

where τ_{SHR} is the electron lifetime, v_n is the mean thermal velocity of the electron, σ_n is the capture cross-section of the defect and N_t is the concentration of the defect [34].

Deep levels traps in the silicon bandgap region, caused by defects and impurities, increases the recombination impact, called SRH recombination. Shallow traps states are in the band edges and are mainly occupied by one type of charge carriers. The charge can be release back to its original band by thermal activation [34]. Deep level traps capture carriers of opposite polarities recombining them. Charge carriers recombining before they are collected do not contribute to the power output of the solar cell device, negatively impacting the conversion efficiency [81]. Therefore, is possible to predict the impact of impurities on the solar-cell performance based on the concentration of electrically active impurities and its recombination parameters.

In no compensated silicon, resistivity ρ measurements of the material correspond to the dopant inverse concentration. However, in compensated wafers, the direct conversion from resistivity to net doping is not possible without taking to account the mobility dependence on ionized dopant scattering and carrier–carrier scattering [81]. A material with low resistivity of 0.2-0.3 Ω.cm has been shown to produce high quality single crystal silicon solar cells. However, for lower quality cast mc-Si, this optimum resistivity increases owing to a dopant-defect interaction, which reduces the bulk lifetime at lower resistivity [82]. Bulk resistivity of 1-5 Ω.cm is commonly seen in solar cells. Although, 16 Ω.cm was proved feasible in n-type material [83]. The positive effects of compensation on recombination are discussed by Coletti et al [81], as well as the concept of using compensation to produce heavily doped feedstocks for solar cell and the accompanying problems of no uniform resistivity profiles along compensated mc-Si ingots.

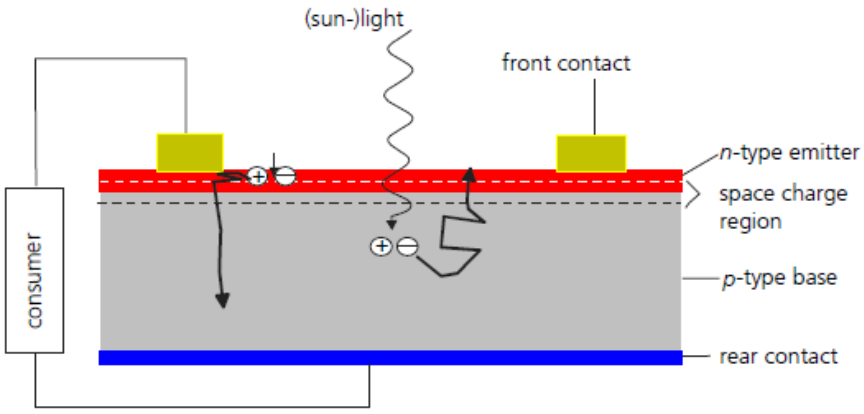
The partially bonded Si atoms at the surface, called as dangling bonds, induces an almost continuous band of defect levels within the energy band gap. This problem is referred as surface recombination velocities (SRV) [34].

The lifetime of minority charge carriers measures indicates the electrical performance in a silicon solar cell [84]. The lifetime, especially in bulk silicon, represents an important parameter of the electronic material, which strongly affects the voltage and maximum current output of a solar cell [24].

2.2.4 Solar cells designs

A simple cell concept for a *p*-type crystalline silicon solar cell is presented in Figure 10 [80], which shows an n-type emitter layer in the front surface, thickness of 0.2-2 µm, and a *p*-type base layer, thickness of 50-500 µm. The incident light creates electron-hole pairs. The carriers cross the depletion region of the pn-junction where they are converted from minority carriers to majority carriers. The electrons are collected at the metal contacts on the front contact and are delivered at the rear contact, producing electrical power.

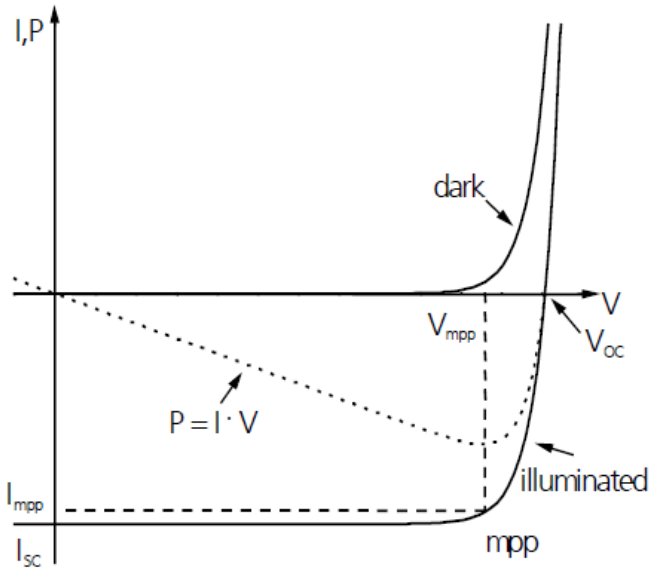
Figure 10 – Schematic drawing of a simple solar cell. The absorbed light creates electron-hole pairs, which are extracted at opposite the metal contacts



Source: O. Schultz [80]

The complete *I-V* curve of a solar cell is illustrated in Figure 11 [80]. The power at maximum power point (mpp) is described by the product of open-circuit voltage (V_{oc}) and short-circuit current (I_{sc}) multiplied by the fill factor. The efficiency is defined as the ratio of power at maximum power point and the incident power of photons usually measured under standard testing conditions (25 °C, 1000 W/m^2, spectrum AM1.5g[1]).

Figure 11 – Schematic drawing of a simple solar cell. The absorbed light creates electron-hole pairs, which are extracted at opposite the metal contacts



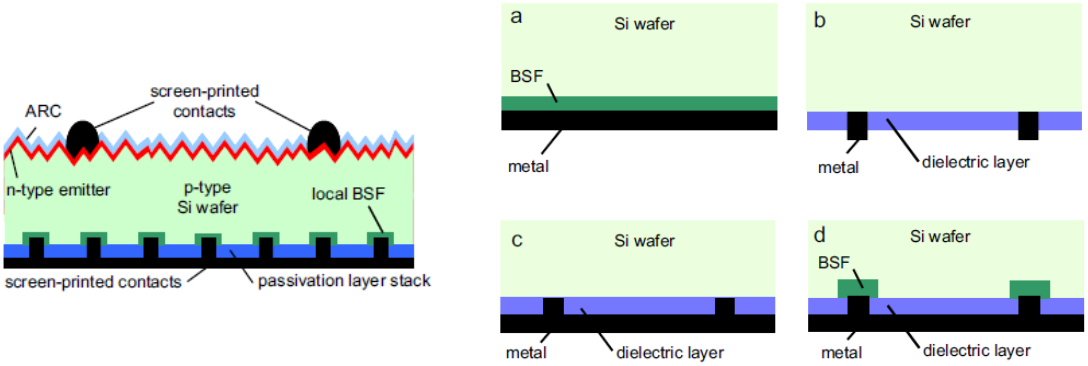
Source: O. Schultz [80]

To maximize the fill factor of a solar cell, the series resistance should be as low as possible whereas the shunt resistance should be as high as possible. Dark saturation current needs to be low. The minority carrier diffusion length should be maximized. This requires not only well-passivated surfaces but also a high minority carrier lifetime in the bulk. The result is a low dark saturation current and high value of V_{OC} and j_{sc}. The contribution of the bulk resistivity to the series resistance can be minimized by a higher base doping, which decreases the minority carrier lifetime by increasing Auger recombination, which leads to a compromise, between the different loss mechanisms, that has to be found in a well-designed cell structure [80].

Rear surface passivation of silicon was first used as a homojunction to suppress the minority carrier concentration, referred to as a "back surface field" (BSF), across the full back surface [85], schematically shown in Figure 12 (Right-a). A passivation of the rear surface by a dielectric film deposited via PECVD in combination with local evaporated contacts on bifacial cells, as in Figure 12 (Right-b). The so-called "passivated-emitter and rear cell" (PERC) is a cell with dielectric passivation with local lithographically defined contact openings and a full-area metallization on the rear surface (Figure 12-Right-c). The increase in reflectivity of the rear surface of the PERC solar cell (Figure 12-Left) increases the number of photons that can be absorbed and transformed into more electricity production. The respective cells referred to as "passivated emitter, rear locally diffused" PERL-type introduced a local back surface field at the contact areas,

formed by a local diffusion through a lithography-defined oxide mask and substantially lowering the recombination at the contacts (Figure 12-Right-d).

Figure 12 – Left: Schematic design of a passivated emitter and rear cell (PERC); Right: Schematic design of different rear surface passivation of crystalline silicon solar cells: (a) large area back surface field (BSF), (b) dielectrically passivated bifacial structure, (c) passivated emitter and rear cell (PERC), and (d) passivated emitter, rear locally diffused (PERL)-type cell



Source: A. Metz et al. [85]

2.3 Impurities, characterization of c-Si and recombination sources

According to Signeur et al [27], one of the PV industry challenges is controlling the type and concentration of impurities in the silicon feedstock while maintaining or reducing cost. Crystal growth techniques introduces new impurities as well as redistributes impurities existing within the polysilicon depending on growth technique, the furnace geometry, the heating scheme, and individual segregation coefficients of the various impurities. The entire manufacturing chain is up to improvement because defects can evolve from one process to another, from quartz reduction to ingot growth, wafering, cell fabrication. Avoiding losses seen in solar modules such as Light-induced Degradation (LID) demand the use of advanced techniques to increase solar cell performance and reduce costs.

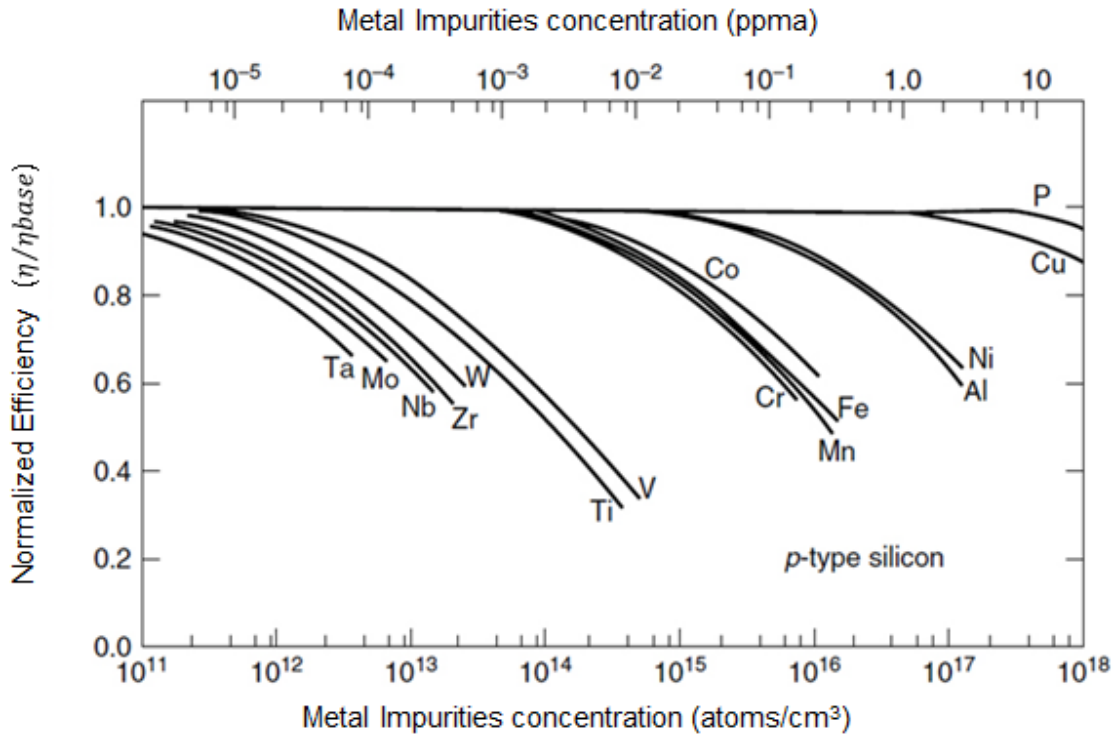
In this chapter are extensively discussed: impurities effects on silicon solar cell performance, characterization of solar grade silicon, characterization of solar grade silicon, characterization of impurities in c-Si ingots, characterization techniques for Silicon ingots and wafers, recombination Sites on mc-Si Wafers and the Light-Induced Degradation on silicon. More emphasis was given on the topics related to multicrystalline silicon material, directional solidification and in studies, which enables the production of photovoltaic cells with higher levels of impurities and / or doping.

2.3.1 Impurities effects on c-Si solar cell performance

Impurities play a vital role in silicon solar cells. Impurities such as boron and phosphorus, in small amounts, are desirable to ensure the electrical characteristics necessary for the production of energy in the silicon solar cell. Other impurities, however, have detrimental effects on solar cells, leading to the formation of defects and favoring the formation of dislocations, which act as deep energy level centers of recombination affecting the mechanical and electrical properties, as well as diminishing the performance [25], [86], [87].

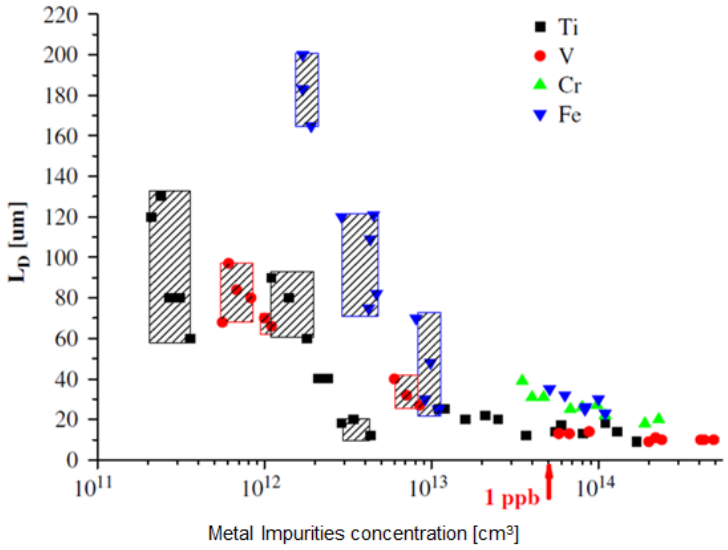
In the 1970s and 1980s, Hopkins et al [88], [89], [90] and S. Pizzini et al [91] did the first systematic investigations on the influence of metal impurities on the silicon in the diffusion length of the minority charge carriers. The effect of the metal impurities on the silicon solar cells is illustrated in Figure 13 where normalized efficiency of solar cell degradation for different metal impurities concentrations is shown, and in Figure 14, the influence of the concentration of impurities on the diffusion length of minority carriers.

Figure 13 – Efficiency of the solar cell related with concentration of impurities



Source: A. Luque and S. Hegedus [44]

Figure 14 – Influence of the concentration of impurities on the diffusion length of minority carriers



Source: S. Pizzini [28]

Several studies have explored metallurgical routes to processing solar cells with a satisfactory photovoltaic conversion efficiency based on less stringent impurities control [92], [93], [57], [94], [95], [96]. Depending on the various characteristics of the material, among which is the resistivity of doped silicon (i.e. doping level); this influence on efficiency can appear at different levels for each type of impurity.

Most reliability challenges such as shunts, crystallographic defects, cracks and LID are related to impurities from feedstock and from processes with high stress conditions such as in ingot growth [27]. Shunts are localized short circuits in the PN-junction area or at the edge resulting in reverse currents, junction breakdown, and hot spots, divided into material-induced, process-induced, and field-induced. Cracks are related to thermal stress, O, C or N precipitates, ingot, and brick shaping. Point, line, planar and bulk defects are typical crystallographic defects caused by interstitial or substitutional impurities, dislocations created under high stress conditions, precipitates, lattices, clusters.

The UMG mono-Si material, whether p-type (B-doped) or n-type (P-doped), suffers from LID due to compensation [27]. The compensated material, with high B and P content, needs further investigations on detrimental effects causing LID, in a comparison of upgraded-metallurgical grade silicon solar cells having identical boron, oxygen and carbon but different compensation levels, the BO-related degradation is found more severe when the compensation is stronger [97]. Same relation between doping and LID is not as detrimental in UMG mc-Si, but still, the material is significantly affected by BO-related LID.

2.3.2 Characterization of solar grade Silicon

Although some impurities may reduce cell performance at extremely low concentrations, others may be tolerated at higher levels. The detrimental role of metal impurities in photovoltaic applications has been extensively considered in studies by Geerligs et al. [98], Dubois et al [99], [100], Hofstetter et al [101] and Coletti et al [102], the latter within the Crystal Clear project.

The results between these studies varied considerably [103]. As an example, in order to obtain a maximum permissible content of Fe and Ti in the feedstock to obtain a 2% loss over an electronic grade feedstock, Geerligs [98] proposes 0.07 ppm_w of Ti and 2.5 ppm_w of Fe. Hofstetter [101] calculates the impurities thresholds for Ti, Cr, Fe and Cu in the raw material, wafers and solar cells. The results are in Table 1, showing a high tolerance for iron in the raw material. Dubois et al. [99], [100] have shown that an iron content of about 2 ppb does not decrease the conversion efficiency of mono-and multicrystalline solar cells, but that a higher tolerance limit depends on a efficiently iron gettering and passivation by hydrogenation. The results indicate that the limit of contamination of the raw materials is determined for the growth process of specific silicon

crystal and for a given impurity, since the removal of impurities depends on the yield of the segregation of this process. In addition, the hydrogenation and gettering processes may play an important role in the relaxation of impurities [28].

Table 1 – Acceptable contamination (C) by impurities calculated for silicon feedstock, wafers and solar cells

Element	$C_{feedstock}$	C_{wafer}	$C_{solar\ cell}$
Ti	0,022	$2,7 \times 10^{-4}$	$2,7 \times 10^{-4}$
Cr	0,026	$4,8 \times 10^{-4}$	$4,7 \times 10^{-4}$
Fe	12,5	0,010	$9,7 \times 10^{-3}$
Cu	4,6	0,046	$5,9 \times 10^{-3}$

Source: J. Hofstetter et al. [101]

The solar-grade silicon analyzes presented in Table 2 by the Crystal Clear project are related to the results of a meeting held in 2008. The typical analyzes of three manufacturers can be considered as a guide, rather than a formal specification [52].

Table 2 – Chemical specification for solar grade silicon. Data in ppm (weight), except the data followed by (a), which indicates ppm (atomic)

	Supplier company 1	Supplier company 2	Supplier company 3
B	0,05	0,45	1,5
P	0,1 (a)	0,6	4 (a)
Al	0,05 (a)	5 (a)	5 (a)
Fe	0,05	5	
Cu	0,01	1	Fe+Cu+Ni+Cr = 5
Ni	0,01	1	
Cr	0,05	1	
Ti	0,005	0,05	0,05
Na	0,01 (a)	0,01 (a)	Na+K = 0,01 (a)
K	0,01 (a)	0,01 (a)	
Zn		2	
Ca			
C	5	30 (p), 1 (m)	
O	5 (p), 1 (m)	20 (p)	

(p) - mc-Si (m) - mono-Si

Source: CRYSTAL CLEAR [102]

To account for the so-called compensated materials, a task dedicated to the Crystal Clear project [102] has reached three categories of solar grade silicon (SoG-Si), with maximum impurity levels discussed as independently as possible of the solidification process.

The first category, non-doped, with very few contaminants (<0.1 ppm_a) can be used as EG-Si, adding the desired dopant and neglecting the other. Metallic impurities are below a few percent of ppm_w.

The second category, compensated, has two doping elements, in equilibrium in the lower part of the ingot, but in such a weak amount that it can be used without much modification of an ingot and cell manufacturing process. Metallurgical routes result dopants are generally [B] <0.5 ppm by weight and [P] <1.5 ppm by weight, and metals less than 1 ppm by weight (for fast diffusers) or 0.05 ppm_w (for slow diffusers, such as Ti). Fe and Al appear to be tolerated up to 5 ppm by weight. O and N in general are not specified because they are added to silicon material during crystallization with coated crucibles.

The third category, highly compensated, would require major changes in the process, such as special solidification eventually under agitation, better gettering and treatments to suppress LID. It is still being investigated. Dopants should remain below 4 ppm_a to maintain a reasonable yield on the directionally solidified ingot and the metal impurities should remain below 5 ppm by weight for the gettering process to function properly, but the actual limits will depend on the chosen solidification process, and the after-process adaptations. Therefore, higher limits of impurities for solar grade silicon were proposed in recent articles [103].

In 2002, D. Sarti and R. Einhaus [12] proposed a metallurgical route to produce solar grade silicon. Consists of a pre-purification step to enhance the material from MG-Si to UMG-Si, followed by a plasma purification. Table 3 summarizes the target impurity values for both, UMG silicon, and SoG silicon after plasma purification. Those targets was closely meet by the prototype purification processes. The obtained SoG silicon was subjected to a standard directional solidification process to produce multicrystalline silicon ingots, from which 100 cm^2 screen printed solar cells were produced. The un-purified UMG silicon is also solidified and subjected to a screen-printing solar cell process, adapted and optimized with respect to the specific material properties. These processes are described in detail in [14]. The plasma purified material resulted in a best efficiency cell of 12.2%. In comparison, the non-purified UMG silicon wafers gave a best solar cell efficiency of 10.0%.

Table 3 –Target impurity concentrations in UMG and SoG silicon (all values in ppm_w)

Impurities	MG-Si	UMG-Si	SoG-Si
Ti	200	< 5	< 1
Al	100-200	< 50	< 2
Fe	2.000	< 150	< 10
Ca	500-600	< 500	< 2
Cr	50	< 15	< 1
P	20	< 15	< 5
B	40	< 30	< 1
O	3000	< 2000	< 10
C	600	< 250	< 10

Source: D. Sarti and R. Einhaus [12]

Seigneur et al [27] presented a list of the accepted, specified, and/or achieved levels of impurities for UMG silicon from various feedstock routes, and the accepted EG-Si, respectively. The list shows that the range of values is diverse, showing that there are numerous possible routes with different levels of impurities for the manufacturing of solar cells. The most diverse values are often of projects in which the purification route is vertical, from the quartz or MG-Si to the silicon ingot.

The standard of the semiconductor industry is in charge by SEMI - Semiconductor Equipment and Materials International, a global industry association of the supply chain of the micro and nano-electronics industries. The SEMI standard PV49-0613 (Test Method for the Measurement of Elemental Impurity Concentrations in Silicon Feedstock for Silicon Solar Cells by Bulk Digestion, Inductively Coupled-Plasma Mass Spectrometry) is used as one of the methods of characterization of the silicon used by the solar cells manufactures [44]. The inductively coupled plasma (ICP) mass spectrometry (MS) technique measures the concentration of metal impurities contained in the sample. ICP-MS, sample is dissolved into liquid form, is then vaporized, ionized in a plasma torch and analyzed in a quadrupole mass spectrometer [104], [105].

The SEMI PV 49-0613 is divided in four purity ranges categories, being the first category (I) with the highest degree of purity and the fourth (IV), with the lowest purity. The categories are grouped and quantified according to the type of elements, as acceptors,

donors, transition metals/post-transition metals and alkaline/earth alkaline as can be seen in Table 4 [44].

Table 4 - Specification of the impurities contained in the solar grade silicon for the production of solar cells according to SEMI PV 49-0613.

General Characteristics						
CATEGORY			I	II	III	IV
Manufacturing method			CVD, metallurgical refining and others			
Acceptors			B, Al			
Donors			P, As, Sb			
Transition Metals and Post Transition			Ti, Cr, Fe, Ni, Cu, Zn, Mo			
Alkaline and Earth-alkaline			Na, K, Ca			
Chemical Characteristics						
CONCENTRATION			I	II	III	IV
Acceptor Ions	L	ppba	≤ 1	≤ 20	≤ 300	≤ 1000
	T			± 5	± 20	± 150
Donor Ions	L	ppba	≤ 1	≤ 20	≤ 50	≤ 720
	T			± 5	± 10	± 150
Oxygen		ppma	NS	NS	NS	NS
Carbon		ppma	≤ 0,3	≤ 2	≤ 5	≤ 100
TCTM	L	ppba	≤ 10	≤ 50	≤ 100	≤ 200
TCAEA	L	ppba	≤ 10	≤ 50	≤ 100	≤ 4000

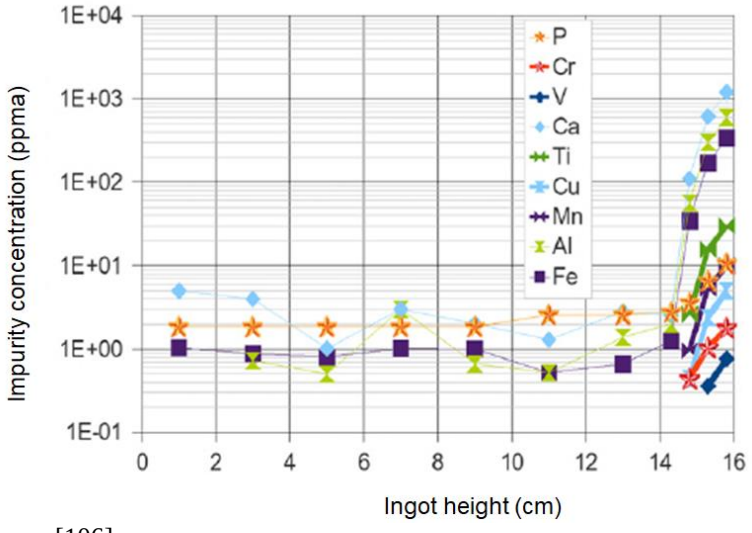
Where:
TCTM – Total concentration of transition metals;
TCAEA – Total Concentration of Alkaline and Earth-Alkaline;
L – Limit;
T – Tolerance;
NS – Not specified.
Source: A. Luque [44]

2.3.3 Characterization of impurities in c-Si ingots

The manufacturing chain of processes for solar cell production and the aimed photovoltaic conversion efficiency affects the level of acceptable impurity for the wafers, which, then, defines the acceptable level of impurities in silicon feedstock for the solidification. In industry, the main crystallization processes are the Czochralsky method and Directed Solidification [54]. The crystallization stage provides another level of purification due to segregation phenomena that concentrate a large amount of impurities in the last liquid phase (removed after Czochralsky growth) or the last solidified material (cut and removed from top of ingots).

The segregation for metallic impurities can be seen in Figure 15 [106] that shows metal impurities along the ingot produced by directional solidification. Some impurities are not or are hardly eliminated because of their segregation coefficient close to one (B, O) or not sufficiently low (P) or because precipitate rapidly (C). Among the metals, some diffuse rapidly in the solid silicon (Cu, Fe, Ni, etc.) and some slowly (Ti, Al, etc.). The processing stage of the solar cell easily collects (getter) the fast diffusers; they are therefore acceptable at higher concentration than slow diffusers with the same electroactivity.

Figure 15 – Metal impurities along the ingot produced by directional solidification

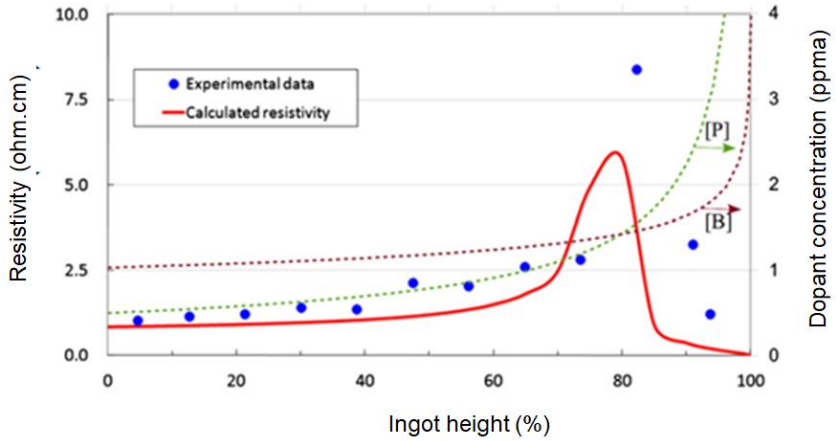


Source: Y. Delannoy [106]

The slow segregation of B and P must be precisely controlled to achieve the wafer resistivity target, which depends on the excess of contaminant atoms per volume unit compared to the other. An excess of B will result a semiconductor of the p-type, an excess

of P will result in n-type. In order to achieve a resistivity for solar cells of approximately 1 Ωcm, this excess of dopant must remain in a fraction of ppm_a. An excess of several ppm_a is feasible if the dopants compensate each other, as shown in Figure 16. This cannot be maintained throughout the entire ingot because of the differential segregation between P (0.35) and B (0.8) which causes the upper part of the ingot to become unusable due to a type change (n-type) with a low resistivity. A resistivity target to the bottom of the ingot and an ingot yield goal (i.e. the position of the type change) will impose the initial concentration of B and P on the silicon feedstock prior to solidification in this case of compensated material.

Figure 16 – The segregation of dopants and resistivity distribution in an ingot grown from compensated silicon



Source: Y. Delannoy [106]

2.3.4 Characterization techniques for c-Si ingots and wafers

Normally, the manufacturers of raw material for Solar Grade silicon qualify their products by the control of the contained chemical impurities. However, the electron activity of some impurities may be dependent on their chemical configuration or their physical distribution in the crystal (complexed with other impurities, dissolved or agglomerated). These effects can be investigated by the electronic properties of crystallized silicon and are therefore used as another measure of the quality of the raw material [107]. Structural and electronic quality can be measured by optical inspection, lifetime, traps density and photoluminescence.

Advanced characterization techniques play an important role in cost reduction. First, the offline characterization of the samples at different stages of

processing is indispensable for the development of good yield processes [30]. Characterization tools are also applied in-line in each manufacturing step.

In this chapter is discussed the characterization techniques especially for mc-Si ingots and wafers, with more emphasis on the implications of impurities on feedstock and its detrimental effects among the chain of processes, from ingot grow to solar cells.

2.3.4.1 QssPC Lifetime measurements

The lifetime measurement is relevant since the minority carrier lifetime is a strong function of the excess carrier density (i.e., of the injection level). Lifetime information that is relevant for the operation of the solar cell is therefore measured under conditions that are equivalent to the operation conditions of the cell in the sun.

The QSSPC technique is used for lifetime measurements, resistivity and saturation current. The lifetime measurement is proceed in two different modes: Carrier lifetime based on the measurement of the photoconductance under quasi-steady-state or quasi-transient illumination [34]. In QSSPC equipment, the sample under illumination generates electron hole pairs, a reference solar cell measures the light intensity and a coil connected to a radio frequency bridge records the increase of the conductance in the sample.

Photoconductance ($\Delta\sigma_{ph}$) and generation rate (G) are the main measured values in the QSSPC. G is determined as a function of incoming flux $\emptyset_{ph}$, as in equation (15) using a referend photocell with known properties:

$$G = \frac{\emptyset_{ph} f_{abs}}{W} \tag{15}$$

where f_{abs} is the share of photons thar are absorbed, determined by the optical properties of the sample, and W is the thickness of the sample X.

$\Delta\sigma_{ph}$ is the difference between dark conductance and elevated conductance due to photogenerated carriers. $\Delta\sigma_{ph}$ is measured inductively by a coil that converts the voltage output in conductivity. The relation between $\Delta\sigma_{ph}$ and the photogenerated carrier concentration is given by equation (16) [108]:

$$\Delta\sigma_{ph} = qW(\mu_n + \mu_p)d\Delta n \tag{16}$$

where μ_n and μ_p are the electron and hole mobility, respectively. The mobility is function of doping, temperature and injection level.

Lifetimes in microsecond regime are essentially measured in steady state [109], [79]. The excess minority carrier density is calculated from $\Delta\sigma_{ph}$, then the effective lifetime under quasi steady state mode, can be expressed as in equation (17):

$$\tau_{eff} = \frac{\Delta\sigma_{ph}}{q\emptyset_{ph}f_{abs}(\mu_n+\mu_p)}. \quad (17)$$

The effective lifetime under transient mode, more commonly used to measure lifetimes in millisecond regime, can be expressed as in equation (18):

$$\tau_{eff} = \frac{\Delta\sigma_{ph}}{qW(\mu_n+\mu_p)\frac{d\Delta n}{dt}}. \quad (18)$$

2.3.4.2 Photoluminescence Images

In luminescence images of silicon samples, the surface of the sample is excited to emit luminescence and a camera is used to get an image. Images by electroluminescence require electrical contacts and therefore are only applicable to already processed solar cells and modules. Due to simplicity, it is widely used for inspection of modules [30]. Photoluminescence (PL) images uses optical excitation, which allows the application of a wide range of samples, including bricks, as cut wafers and partially processed wafers. In the application of photoluminescence images, contact with the sample is avoided, which is an important practical aspect for productive line applications, for example, in terms of measurement speed and in terms of reducing the risk of mechanical damage in the sample.

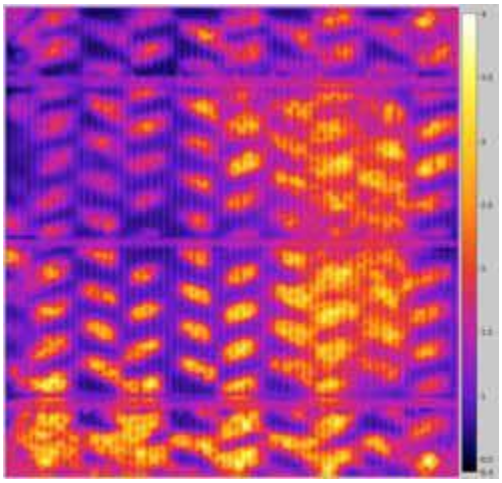
Specific applications of luminescence images have been developed aiming the extraction of parameters of materials and devices from single or multiple luminescence images under different operating and/or measuring conditions [24], [110], [111], [112], [113]. T. Trupke, et. al. [30] studied different lifetime of minority carriers image characterizations and serial resistance imaging for which photoluminescence imaging is adequate as a quantitative measurement technique, within a review of

photoluminescence imaging applications in silicon bricks and in-line quality control of as cut wafers.

2.3.4.3 Series resistance measurements with PL

Any luminescence image taken with current flow between contacts, in principle, can quantify the series resistance of the material [30]. Figure 17 shows an image of resistance series of a multicrystalline silicon cell with a method implemented in the BT Imaging LIS-R1 tool. The color bar represents the resistance series ($\Omega.cm^2$).

Figure 17 – Series resistance image of a multicrystalline Si cell performed on a BT Imaging LIS-R1



Source: T. Trupke et al. [30]

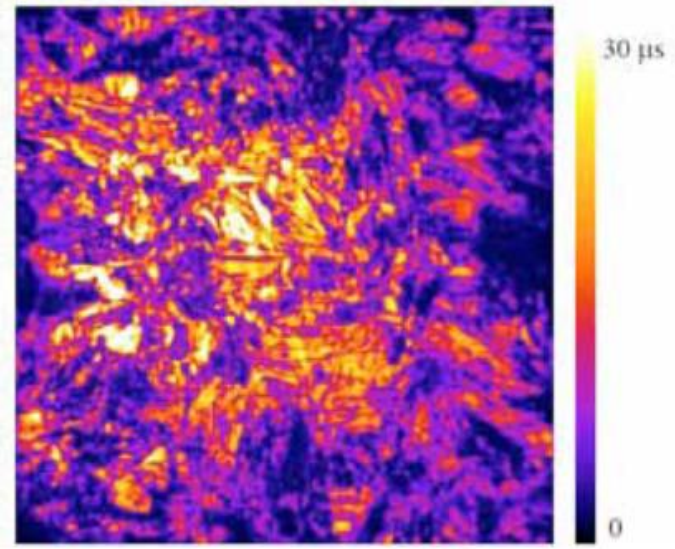
A number of other luminescence series resistance imaging techniques can be applied, including electroluminescence-based techniques and the comparison of luminescence images with lock in thermography data [30]. Photoluminescence images for series resistance allows a significantly more accurate separation of the series resistance effects from the minority carrier lifetime variations, and measures the serial resistance in operation conditions equivalent to the maximum power point.

2.3.4.4 Lifetime measurements with PL

Lifetime information is measured under conditions equivalent to the operating conditions of the cell when exposed to the sun. Typical industrial solar cells operate at excess density of charge carriers in the order 10^{13}-10^{14} cm^{-3}. Photoluminescence images can measure lifetime of minority carriers for these excess densities [30], [110]. An example of a calibrated lifetime image is shown in Figure 18.

The effective lifetime of minority carriers is observed by a photoluminescence image of a passivated multicrystalline Silicon wafer. The effective lifetime vary from zero to 30 µs. Most of measured higher lifetime values are due to intra-grain areas.

Figure 18 – Effective Lifetime of minority carriers from a Photoluminescence Image of a passivated multicrystalline Silicon wafer



Source: T. Trupke et al. [30]

2.3.4.5 PL Calibration with QssPC

The interpretation of the photoluminescence signal in terms of minority carrier lifetime needs to take into account that the spontaneous emission rate and, thus, the measured signal is not determined only by the excess minority carrier density (Δn), but also by the doping network. In addition, the fraction of the rate of spontaneous emission that escapes and can therefore be measured as a photoluminescence signal also strongly depends on the optical properties of the sample. A separate calibration is therefore required for each different type of sample. Calibration by comparison with quasi-steady-state photoconductance (QSSPC) is considered the most accurate calibration approach [7].

A. Giesecke et al [110] proposes an adequate average spatially resolved lifetime measurements in materials such as multicrystalline upgraded metallurgical grade silicon, which frequently feature relatively low lifetimes, high trap densities, and several material parameters that are not predictable or measurable such as charge carrier mobility and net dopant concentration. The proposed luminescence based lifetime imaging

technique, requires no information about material parameters, and is based on a calibration of a wafer photoluminescence image through a precise lifetime determination of a part of this wafer via quasi-steady-state photoluminescence. Carrier mobility, net dopant concentration, and surface morphology does not affect the lifetime determination. Lifetimes down to the timescale of a microsecond can be measured.

2.3.4.6 PL characterization of mc-Si Ingots and Wafers

Different types of defects can be observed in silicon ingots produced by directional solidification. Deep levels in the silicon band gap are established by point defects introduced by impurities, dislocations, stacking faults and grain boundaries. Thus, all the defects have an impact on the time of recombination of the minority carriers (lifetime) [24]. The SRH theory allows the determination of a SRH recombination lifetime if the concentration and capture cross sections of the relevant defect level is known [81]. Modern solar cell architectures may, however, respond differently to impurities.

The photoluminescence images on the sides of the silicon bricks after directional solidification can give a measure of the crystallization process and feedstock material quality in relation to bulk lifetime, doping, grain structures and dislocations [4].

The measured photoluminescence signal is determined by the effective lifetime τ_{eff}, which is generally affected by both bulk and surface recombination [30], and can be expressed in a simplified way as in (19):

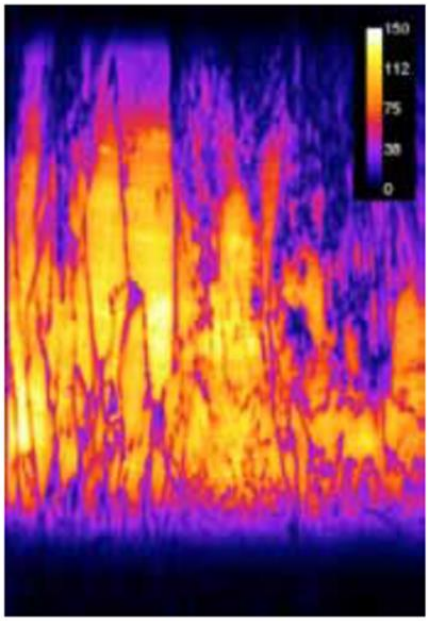
$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surface}} \qquad (19)$$

Effective lifetime measurements on as cut wafers can be strongly affected or completely dominated by the surface recombination component for bulk lifetime exceeding about 10 μs [30]. Effective lifetimes in a brick show significant variation up to very large bulk lifetime values of several milliseconds, allowing a transfer function to be calculated that converts measured effective lifetime to bulk lifetime.

Calibrated photoluminescence image of the side of a typical mc-Si brick, boron doped, 25 cm high, 6 x 6 inch (15.24 x 15.24 cm), prior to wafering, is seen in Figure 19. Dark bands with strong reduction of the photoluminescence counting rate are seen in the lower and upper part of the brick and near the left margin. These bands

represent regions that have severely reduced bulk lifetime due to the high concentration of impurities, such as oxygen, carbon, transition metals, diffusion of impurities from the crucible walls to the ingot, segregation from the bottom up during crystallization and diffusion from the top during cooling [30]. The image also shows the distribution of efficiency limiting structural defects, such as the dislocations. An area of high density of dislocations is seen in the upper right corner of the brick. These dislocations are of particular importance as they remain as defects that limits the efficiency in the finished cells.

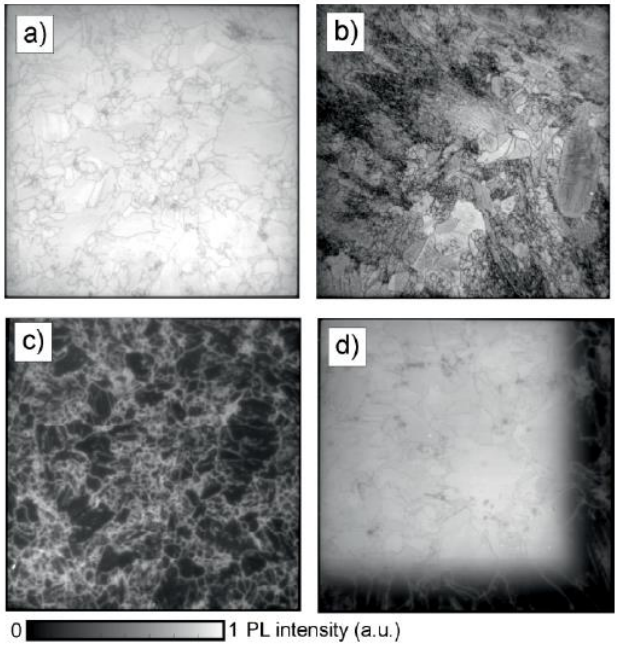
Figure 19 – Bulk lifetimes of a multicrystalline silicon brick from a photoluminescence image normalized by doping and calibrated with QSSPC



Source: T. Trupke et al. [30]

Photoluminescence images of as cut wafers can be used by manufacturers for quality control and classification. It allows the detection of regions of efficiency-limiting impurities near the edges of the wafer, the identification of top and bottom wafers with low bulk lifetime and areas with high dislocation density, which strongly correlates with the final performance of the cell. Figure 20 shows four typical examples of wafers from different bricks positions and/or ingot heights. All dark areas in these images are indicative of highly recombination active regions [114].

Figure 20 – PL image taken on four as-cut mc-Si wafers: (a) a wafer from a center brick with few dislocations, (b) a wafer from a center brick with high dislocation density, (c) a wafer from the impurity rich area at the bottom and (d) a wafer from a corner brick with low dislocation density



Source: T. Trupke et al. [114]

2.3.5 Recombination Sources on mc-Si

The limitations on energy conversion efficiency in mc-Si solar cells are mainly caused by charge carrier recombination due to crystal imperfections such as dislocations, grain boundaries and impurities [115]–[117]. Therefore, an further understanding of the defects in mc-Si may significantly contribute to the improvement of mc-Si solar cells towards equivalence with monocrystalline solar cells [118], [119].

H. Sio et al [120] presented an evaluation of the electronic properties of a p-type multicrystalline silicon ingot before and after gettering and firing enables a prediction of the final cell performance. The wafers of different positions of the ingot are analyzed in terms of defects and average lifetimes. Figure 21 (left) shows the intra-grain regions average lifetimes of a HPMC-Si wafer extracted from photoluminescence images before and after the gettering and firing processes. Before any processing, the intra-grain lifetime is higher in the middle of the ingot and gradually decreases towards the bottom and top. This is due to the higher concentration of impurities near the top and bottom of the ingot due to the segregation of the liquid phase and the diffusion from the crucible during the solidification. The gettering step significantly increases the lifetime of the intra-grain regions. The benefits are particularly noticeable in the wafers towards the top

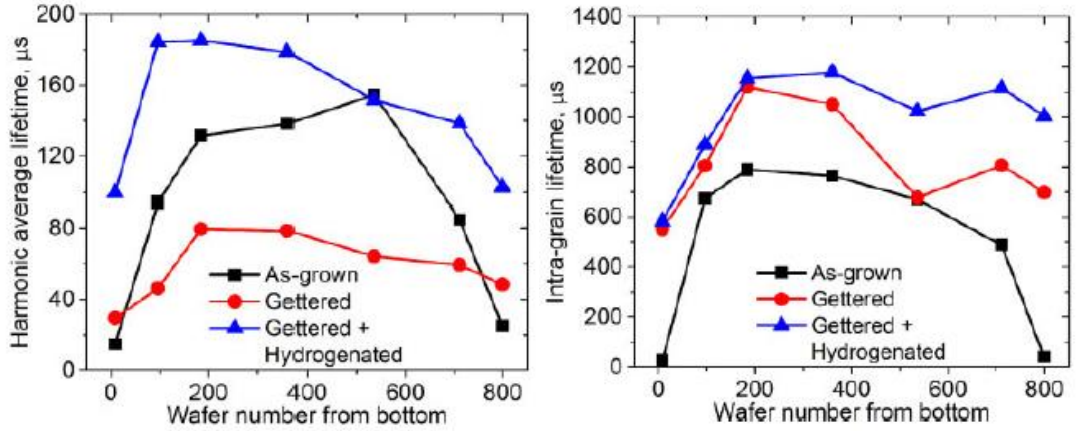
and bottom of the ingot, where the average lifetime intra-grain increases more than tenfold, from less than 50 μs in the as cut state to more than 500 μs, becoming comparable to the intra-grain lifetime of the wafers from the middle of the ingot. This suggests that gettering is efficient in the segregation of impurities for lower-quality mc-Si wafers. Intra-grain lifetime is further improved after a subsequent firing (hydrogenation) step, reaching 1 ms or above. It should be noted that the intra-grain lifetime in mc-Si wafers after gettering and hydrogenation are somewhat comparable to the lifetimes reported in Cz-Si even after the deactivation of the boron-oxygen complex (BO-LID), suggesting that it is unlikely that the efficiency potential of the mc-Si cell is limited by the recombination of carriers in the intra-grain regions.

Figure 21 (right) shows the impact of gettering and firing on the average lifetime of the HPmc-Si wafers. The harmonic mean is used to represent the overall lifetime because it provides a closer estimate of the quality of the material to predict the final performance of the cell [120]. Compared to the simple arithmetic mean, the harmonic mean is more affected by the low life regions of the samples, such as grain boundaries and dislocations. Comparing both graphics from Figure 21 (right and left), it can be observed that total lifetime of the material is strongly limited by recombination in crystal defects, given the high intra-grain lifetime (> 600 μs). Perhaps unexpectedly, the lifetime of most wafers, except those close to the upper and bottom of ingot, degrade after gettering. The reduction of the average harmonic lifetime after gettering is due to the activation of grain boundaries during the process. The application of a subsequent firing step can significantly improve the overall lifetime, mainly due to its ability to passivate the grain boundaries. The relatively inactive grain boundaries after firing also allow for the benefits of gettering in the intra-grain regions, further improving overall lifetime.

Figure 22 shows photoluminescence images of the selected HPMC-Si wafers [120]. The active grain boundaries of recombination appear in the images as dark lines, while dislocations appear as dark clusters. The ingot shows a continuous increase in grain size with increasing ingot height. While the average grain size of the bottom wafers is small, the grain structure of the top wafers is similar to those observed in conventional mc-Si. The grain boundaries in the as cut wafers from the middle of the ingot tend not to have active recombination before any thermal process, while the top and bottom ones are already active. The gettering increases the recombination activity of most grain boundaries. The exact underlying mechanism is not yet fully understood. The change in

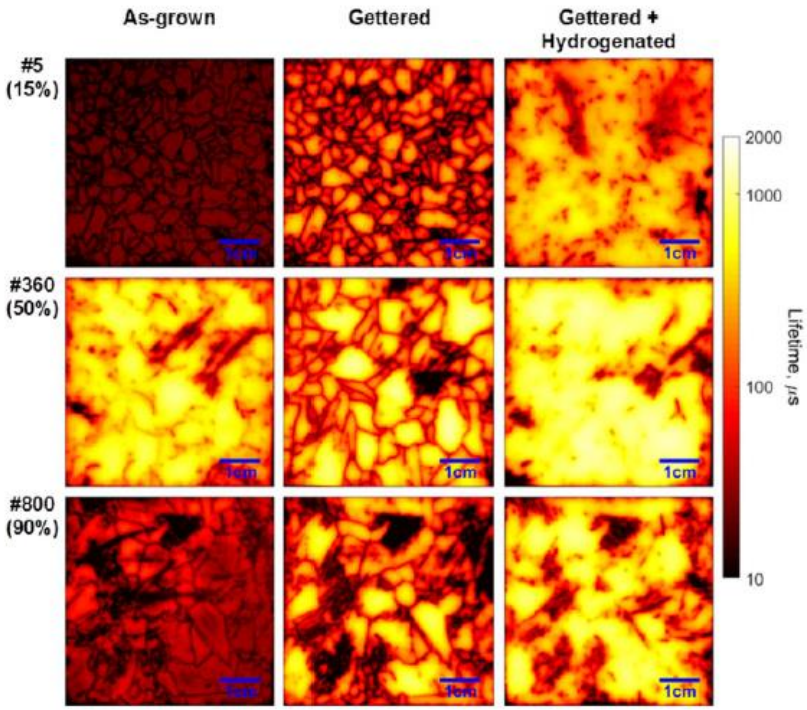
recombination activity might be related to the presence of metals, as evidenced by a change in precipitate distribution on the extended defects [121].

Figure 21 – Left: average lifetime of intra-grain regions extracted from photoluminescence images in HPMC-Si wafers before and after gettering and firing. Right: harmonic average lifetime extracted from photoluminescence images of the same wafers



Source: H. Sio et al [120]

Figure 22 – Photoluminescence images of various mc-Si wafers selected before and after gettering and hydrogenation. The samples were double sided passivated. A logarithmic color scale is used in the figure. The wafer number of the bottom of the ingot and the corresponding fraction of the height of the ingot, based on the height of the ingot, are shown in the left column.



Source: H. Sio et al [120]

The firing step (hydrogenation) proves to be very effective in passivation of grain boundaries and to neutralize detrimental influence of the gettering, regardless of the position of the ingot [120]. This is confirmed in Figure 22, where most of the dark lines shown in the images disappear after firing. However, the influence of hydrogenation is not as effective in dislocations. The dislocations agglomerates are still observed in Figure 22 after hydrogenation. The results suggest that the mechanism of recombination of the dislocations may be different in relation to the grain boundary.

Hallam et al. [122] propose that advanced hydrogenation processes can ensure adequate passivation, controlling hydrogen charge states, enabling higher efficiency devices to be fabricated with wafers produced from the UMG silicon.

Metallic impurities in the material results in a dependence between the bulk minority carrier lifetime and the injection level that follows the Shockley–Read–Hall recombination theory. Modeling of this dependence gives information on the fundamental electron and hole lifetimes, with the former typically being considerably smaller than the latter, for p-type silicon [109]. The mc-Si crystallization by directional solidification method in a quartz crucible, feed with polycrystalline Si chunks, causes relatively high concentrations of especially transition metal impurities such as Fe, Ni, Cu, and Cr to be incorporated within the material. These impurities may be present in different states, *e.g.*, interstitially dissolved, as metal-silicide nanoprecipitates, or as larger micronized particles, potentially causing severe degradation of the performance of the device if not properly controlled during cell processing [70]. The multiple impurities are of interest for the use of alternative feedstock materials such as upgraded metallurgical silicon (UMG-Si). A detailed knowledge about the interaction between crystal defects and impurities and their influence on solar cell parameters is essential [123].

The effects of impurities on silicon material properties can be separated in two aspects: the minority-carrier lifetime affected by the concentration of electrically active impurities [81]; and the coexistence of impurity contamination and crystallographic defects, causing incorporation of metal clusters into structural defects during growth [70]. Transition metal impurities such as iron, copper and chromium enhance the net recombination of minority carriers within the bulk material or negatively influence the emitter region. S. Reipe et al [124] studied the incorporation mechanisms and limits of tolerable amounts of impurities in solar silicon by simulating the use of UMG feedstock with intentionally addition of typical transition metal impurities. It was found that only high levels of contamination of transition metals in the range of 20 ppm_a

in the melt result in significant higher impurity levels in the middle of the ingots. Strong interactions in the precipitation of different species are also found. Feedstock containing 1-2 ppma of the investigated metal impurities were found able to yield solar cells with efficiencies up to 16%.

Significant efficiency reduction in the wafer lifetime correlates to the regions of high precipitate density and shading. The reverse bias characteristic of cells from these regions show areas of high local current flow identified as ohmic shunts. The IV-characteristics indicate material induced shunts caused by SiC filaments [18]. Additionally, SiC precipitates can introduce dislocations and stress into the silicon matrix. Since there is always a certain amount of transition metals in the melt due to the influence of the crucible, these metals inevitably decorate microstructural defects and can form metal precipitates. In combination with residual stress around these defects, high recombination activity occurs resulting in low lifetime.

The interstitial carbon centers are highly mobile above room temperature and form complexes with the remaining substitutional carbon, oxygen, boron and various other impurity atoms [81]. The residual stress in silicon resulting from the growth process is believed to play a role in the formation of SiC precipitates, which can lead to strong ohmic shunts [27]. These carbon centers are highly mobile above room temperature and form complexes with the remaining substitutional carbon, oxygen, boron and various other impurity atoms. Oxygen is a lower diffusivity impurity, compared to metallic impurities, is then more difficult to eliminate by the segregation effect. Tajima et al [113] demonstrated the presence of a dislocation-related component and a component due to oxygen precipitates in a broad deep-level photoluminescence (PL) band in multicrystalline Si. The presence of grown-in oxygen precipitates, whose amount depends on the thermal history of each ingot, are associated with deep energy levels in the bandgap, and therefore become recombination centers for minority carriers [81].

Carrier lifetimes can, in principle, be increased by adding compensating dopants [81]. Dubois et al [125] demonstrated experimentally this behavior in multicrystalline silicon. Compensated silicon have used, however, solar-grade feedstocks that also contain other metal impurities, masking the impact of compensation. Compensation can reduce the recombination activity of impurities in silicon by reducing the net doping. However, if the dopant atoms form part of a recombination active defect, such as boron-oxygen related LID, additional dopant atoms could result in a higher concentration of defects [81].

2.4 Light Induced Degradation on silicon

Light induced degradation is an observed degradation in the solar module performance under field operation conditions due to carrier injection [27], [77]. The main lifetime reducing defects, induced by impurities are: the formation of boron–oxygen (B–O) complexes, showing an increased LID with the net doping but not with total boron concentration; the interstitial iron formed when iron–boron pair (Fe–B), which dissolves up on carrier injection; the low concentration of interstitial Cu; the hydrogen induced degradation (HID) and/or H-B pairs, which was recently proposed as responsible for the light and elevated temperature induced degradation (LeTID) [126].

In 2012, Tine U. Nærland et al [36] developed a new approach to investigate light induced degradation (LID) effects in boron-doped silicon. By studying spatial variations in LID resulting from localized carrier excitation, the generation of the boron-oxygen complexes is directly related to the presence of excess minority carriers. The results also shows that very low concentrations of minority excess carrier densities are sufficient to generate the defects.

Lindroos and Savin [77] reviews four decades of LID studies in both electronic- and solar-grade crystalline silicon, mainly on the properties and the defect models of boron-oxygen LID and copper- related LID. Although several advances, industrial silicon solar cells still suffer from different types of light-induced efficiency losses. The review also presented current techniques for LID mitigation and summarizes recent observations of severe LID in modern multicrystalline silicon solar cells, commonly referred to as LeTID.

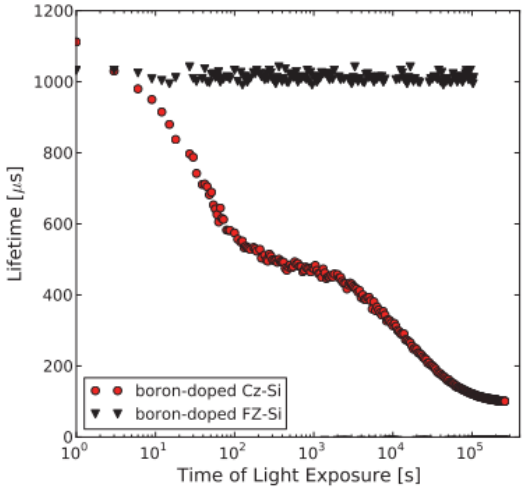
One of the main concerns about UMG-Si is the LID reliability. K. Petter et al [127] compared the performance, over a time span of up to almost three years, between SoG/UMG-Si and systems and modules produced with EG-Si. Short-term degradation may slightly be influenced by the silicon feedstock. No additional degradation in the long term caused by bulk related defects such as boron-oxygen complexes and interstitial iron was observed.

LeTID in p-type high performance multicrystalline silicon (hpmc-Si) is found to be activated at firing temperatures above an activation point [128] if passivated with hydrogen rich layers [129]. Thus, LeTID is seen as more related to the manufacturing processes then to the feedstock quality.

2.4.1 BO-LID in P-type Cz-Si

Light induced degradation (LID) reduces the solar cell efficiency through the generation of metastable defects. This is an inherent problem in boron-doped Czochralski silicon (Cz- Si). Tine Uberg Nærland in the PhD Thesis [34] extensively studied this topic developing characterization methods for the BO-related defect. Figure 23 shows a BO-LID measured in a B-doped Cz-Si with oxygen concentration above 1ppm. A boron doped Cz-Si sample degradation at light exposure is compared with a boron doped FZ-Si sample in the same conditions. FZ-Si contains no oxygen and it is not expect to degrade in light, so it used as a reference to rule out other possible degradation mechanisms. The degradations first observed as a fast initial exponential decrease of the minority carrier lifetime, followed by a second slower decay [77], which dominates the degradation.

Figure 23 - Lifetime as a function of light exposure for a-Si:H passivated boron doped Cz-Si and FZ-Si



Source: Tine U. Nærland [34]

The temperature and the carrier injection conditions can impact the degradation rate and the normalized defect density of the fast and the slow recombination centers [77]. Full dissociation of both fast and slow defects is observed after annealing at 200°C in the dark [6]. In Cz-Si, the metastable defects completely deactivate by applying simultaneous illumination and annealing at 65–210°C [130], [131]. After regeneration, further illumination causes no severe defect formation. However, annealing at 200°C for one hour is sufficient to completely destabilize the regenerated lifetime [132]. Therefore, a subsequent illumination will once again lead to the full BO-LID defect formation. The BO-LID is classified as metastable, with a three state defect model [133]. Beside light

and heat treatments, boron-oxygen related LID traditional mitigation is due to producing a silicon with lower concentration of boron and oxygen [77].

2.4.2 BO-LID and LeTID in P-type mc-Si

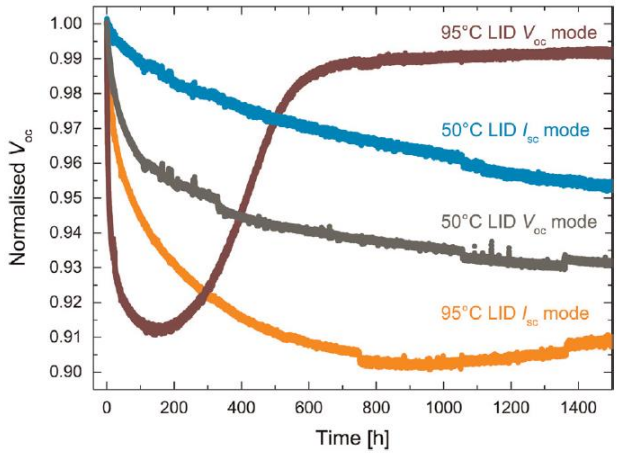
Boron doped multicrystalline silicon is reported to be affected mainly by two lifetime degradation mechanisms, the light induced degradation caused by boron-oxygen-complexes (BO-LID) and the light and elevated temperature induced degradation (LeTID) [134]. The effect of iron-boron pair splitting on the minority carrier lifetime can be suppressed if interstitial iron is efficiently removed in the gettering process.

P-type mc-Si light induced degradation was first reported as a long time scale severe drop in cell efficiency in photovoltaic modules at operation conditions in the field that could not be explained and exceeded the effects of iron contamination or boron-oxygen defects [135]. It was referred to as light and elevated temperature induced degradation (LeTID) [31] and also called carrier induced degradation [136]. Numerous investigations about LeTID are trying to understand the degradation mechanism and the possible impurities that causes or influences the degradation [26], [129], [137]–[140].

LeTID is commonly evaluated by the degradation behavior of the minority charge carrier lifetime in wafers [141], [142], [143], [144], [77], or the performance of cells [145], [140], [31], using illumination at an elevated temperature. Figure 24 shows the Kersten et al [31] data for mc-PERC cells degradation after illumination at 300W.m^{-2}, at different temperatures of 50°C and 90°C, for V_{oc} and I_{sc} mode. A significant Voc degradation at 95°C in Voc mode of 10% after approximately 150h can be observed. PERC cells in Isc mode, i.e. slower injection level, shows a slower degradation. LeTID is accelerated by higher temperature or higher injection level. After the maximum degradation, a regeneration effect starts. After 1000h at 95°C in Voc mode, the PERC cells are almost completely recovered.

Understanding and restraining LeTID is seen as essential as it is more evident and causes greater efficiency loss on the passivated emitter rear contact solar cell structure (PERC) compared to its predecessor in the industry, the aluminum-back surface field (Al-BSF) cell [146]. Power degradation of above 10% after several hundred to thousand hours was measured in mc-PERC cells [31]. Avoiding LeTID for p-type mc-Si is crucial to its survival among increasingly efficiency solar cells in the photovoltaic industry [147].

Figure 24 - Kersten et al [31] data, illuminated annealing (300W.m^{-2}) in mc-PERC cells at 50°C and 95°C; Voc and Isc mode



Source: Kersten et al [31]

A common consensus of the root cause of LeTID has not been settled [147], [26]. LeTID in p-type high performance multicrystalline silicon (HPMC-Si) was found to be activated at firing temperatures above an activation point [128] on the presence of hydrogen rich passivation layers [129]. LeTID, first discovered in p-type HPMC-Si, has later also been observed in p-type float zone Si [26], [148], p-type mono-like Si, p-type Czochralski Si [149] and n-type HPMC-Si [144] under the same process conditions.

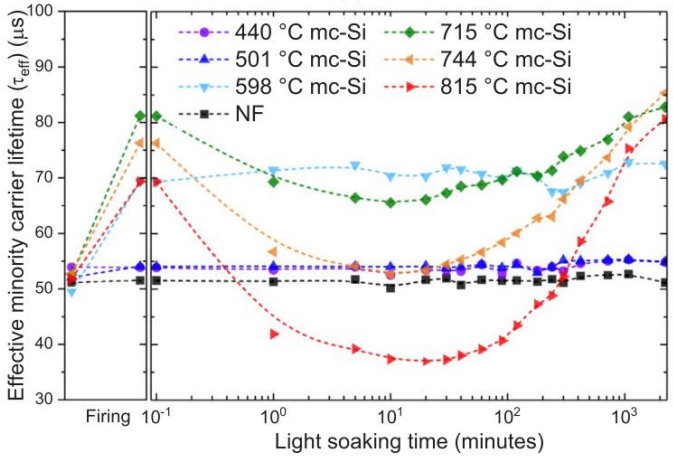
The firing process was found to greatly modulate the concentration of LeTID related defects [150]. Lower firing peak temperatures could prevent LeTID from been activated [151], however, these temperatures around 650°C may not be feasible in the industry as contact formation after silver screen printing requires peak firing temperatures of around 800°C. According to Eberle et al [152], LeTID defects can be virtually suppressed even at higher peak temperatures of 850°C, although it is unknown whether this is related to a longer residence time in the firing furnace or to the ramp-up and cool-down slower rates. Co-firing with rapid heat and light treatment may lead to the near-solution of LeTID [151], but it may bring problems to contacts depending on the co-firing conditions [75].

LeTID is primarily associated with a bulk defect [15]. Metal impurities involvement on degradation causes is unlikely, since there is low metal content in FZ-Si, but still LeTID is observed. Although, even not directly related to the cause, metal contaminants, dislocations, grain size and other defects may affect the extent of LeTID [146]. The thickness of the sample [153], the thermal history of processes [154], or the fraction of ingot height [147] can also be relevant to LeTID extent. Therefore, using

neighboring wafers, i.e. same ingot and same fraction of ingot height, is a solution for comparing light induced degradation behaviors on different heat and/or surface treatments.

One of the possible LeTID causes is the formation and subsequent dissolution or evolution of a recombination-active H complex [8]. Hydrogen is known to passivate defects in silicon [126], among them, grain boundaries, dislocations, BO and possibly FeB pair defects. Excess of hydrogen into the bulk, on the other hand, can be related to the LeTID activation [155]. D Chen et al [149] demonstrate a degradation and recovery of bulk minority carrier lifetime, in samples with hydrogen rich passivation layers, induced by either illuminated or dark annealing in mono- and multicrystalline silicon and a modulation in the magnitude of degradation varying the firing temperature conditions. Figure 25 shows the effective minority carrier lifetime extracted at an injection level of $\Delta n = 9.1\times10^{14}$ /cm^3, as a function of illuminated annealing time for mc-Si samples. The degradation extent was highly dependent on the peak firing temperature. A recovery was also observed. The recovery of all samples was complete after approximately 15 hours.

Figure 25 - Absolute change in effective minority carrier lifetime of mc-Si samples fired at various temperatures as the result of illuminated annealing



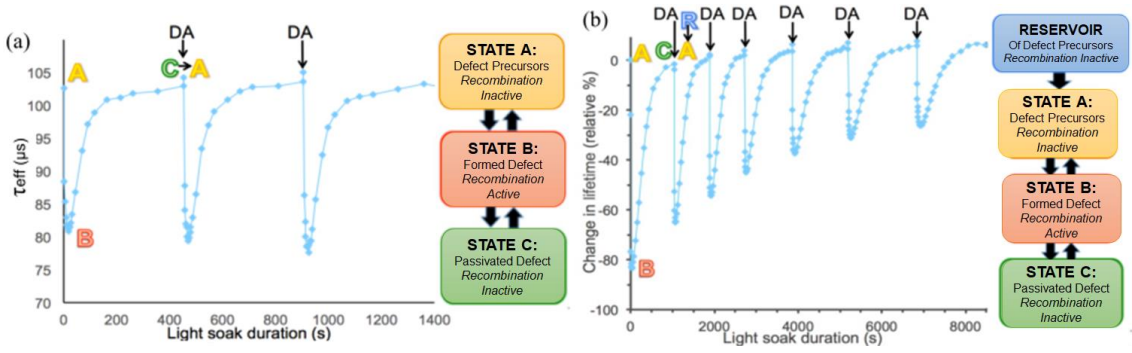
Source: D Chen et al [149]

Accordingly to studies from A. Cielsa, Prof. Stuart Wenham et al. [126], LeTID is proposed to be explained by a hydrogen induced degradation (HID). In his view, the mechanisms for lifetime changes in Figure 25 can be explained as following: the left side of Figure 25 shows lifetime increases after firing. With increasing temperatures until 715°C, more hydrogen is released into the silicon from the dielectric layer for better passivation, thus, the lifetime increases. Further increased temperatures

actually result in less improvement in lifetime after firing, as the excessive amounts of hydrogen start to have a detrimental effect, and higher degradation at illuminated annealing. Thermal history of silicon may therefore also have an influence on the amount of hydrogen in the silicon bulk and on its charges states and, consequently, on the activation or deactivation of LeTID. Therefore, heat and illumination treatments in co-firing processes that possibly change the hydrogen content into the silicon bulk and hydrogen charges, respectively, are under investigation [151], [156], [146] aiming to ensure a material free of light degradation regardless of its process history.

There is one important difference between the BO related LID and the LeTID. In Figure 26 [126] is presented the BO-LID dark anneal and accelerated light soaking cycles with three state model (left), LeTID at same induced cycles with a resulting different state model including a reservoir (right). BO-LID three-state defect model [133] is described as: A) recombination inactive defect precursors; B) recombination active defect; C) recombination inactive passivated defect. The resulted material can return to state A through a dark anneal and show a completely repeatable degradation cycles. A similar dark anneal process on a sample regenerated after LeTID do not return the same pattern. The extent of degradation decreases with each successive dark annealing-light soaking cycle, as shown in Figure 26 (right). The addition of a reservoir state that feeds into state A and gets depleted over time was modeled [157].

Figure 26 – Left: BO-LID dark anneal and accelerated light soaking cycles with three state model, observed in Cz-Si. Right: LeTID in mc-Si dark anneal and accelerated light soaking cycles with state model including reservoir



Source: A. Cielsa, Stuart Wenham et al. [121], C. Chan et al. [152]

The second possibly less detrimental degradation mechanism expected in HPMC-Si, the boron-oxygen related light induced degradation (BO-LID), can activate boron-oxygen complexes as recombination sites under illumination, reducing the

minority charge carrier lifetime [158], [35]. A recovery of the lifetime at illuminated annealing towards the initial lifetime value to a metastable state [159] is also expected. The impact of the BO-LID degradation on the open circuit voltage (V_{OC}) is reported to be minimal in current solar cells structures based on HPMC Si wafers [154], [160], and it can be separated from LeTID by an initial light soaking at room temperature prior to the illuminated annealing. The two degradation mechanisms seems to show a combined recovery [161], [134], however.

Evaluation of the LeTID with the simultaneous presence of BO-LID as well as extended crystal defects, such as grain boundaries, in p-type HPMC-Si wafers, must take into account the contributions of these different defects to the measured effective lifetime. The effective lifetime in silicon wafers is given as the inverse sum of the individual lifetime contributions, as shown in equation (20):

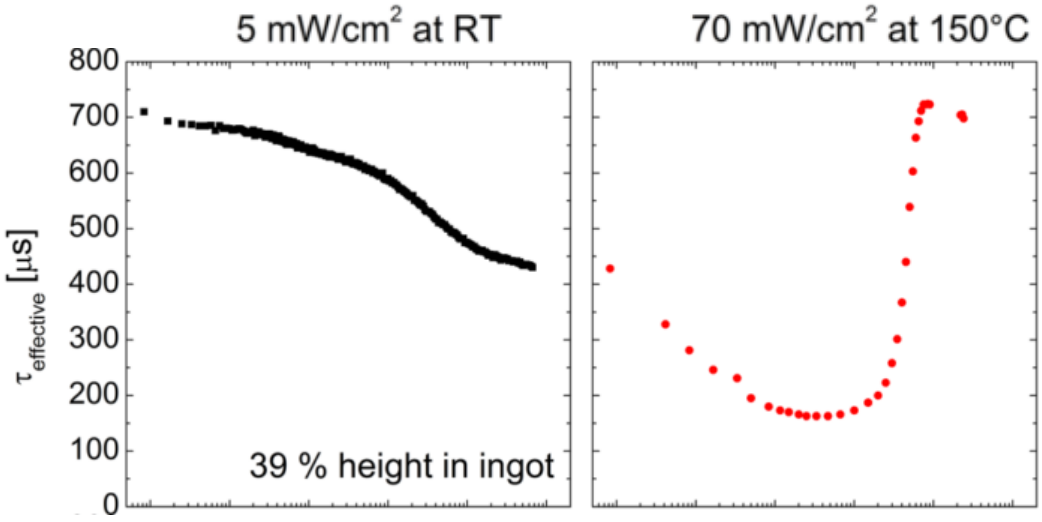
$$\frac{1}{\tau_{effective}} = \frac{1}{\tau_{LeTID}} + \frac{1}{\tau_{BOLID}} + \frac{1}{\tau_{crystal\ defects}} + \frac{1}{\tau_{others}} + \frac{1}{\tau_{surface}} \tag{20}$$

where the main contributions to the effective lifetime are τ_{LeTID}, τ_{BOLID}, and $\tau_{crystal\ defects}$. Contributions from τ_{others} and $\tau_{surface}$ are not influenced by illumination and the contributions are considered minor compared to the former three due to efficient gettering and surface passivation. The bulk defects contributions to the lifetime are more visible when evaluating the minority carrier lifetime in surface passivated wafers as $\tau_{surface}$ is minimized. Significant contributions from the τ_{BOLID}, and the $\tau_{crystal\ defects}$ are however expected, especially prior to full activation of the LeTID defect.

R. Søndenå et al. [134] reported that a separation of the BO-LID and the LeTID degradation mechanisms might be necessary since BO-LID contribution to total measured degradation was found not negligible. Boron-oxygen related LID is visible in wafers that have gone through a gettering process and a simulated firing process with a hydrogen rich ARC present. LeTID defects, occurring under illumination at elevated temperatures was not observed in ungettered wafers and had been activated in wafers subjected to a firing process. Figure 27 shows the separated BO-LID (left) and the LeTID (right) contributions to the total degradation in sequential lifetime degradation curves in gettered and fired wafers from 39% height in the ingot. First, a low intensity illumination at RT to measures the BO-related LID, where LeTID is expected to be extremely low. A

second illuminated annealing at 150°C and 70mW/cm^2 is proceed after 72 hours, when the BO-LID is fully activated.

Figure 27 – Sequential lifetime degradation curves in gettered and fired wafers from 39% height in the ingot. The BO-LID and the LeTID contributions to the total degradation are shown on the left and the right side, respectively



Source: R. Søndenå et al. [134]

In Figure 27 is observed that after about one hour of illumination at 70mW/cm^2, 150 °C, the minority carrier lifetimes starts to recover. This regeneration process is assumed to be a combined effect where both BO- and LeTID-defects are deactivated [134]. The combined recovering of BO related LID and LeTID is under investigation in recent literature. A possible involvement of cross-passivation between hydrogen, H-B pairs and BO are taken into account, which could result in three different mechanism of regeneration when both defects are activated, and when one or another defect is completely or almost completely suppressed [126], [161]. The BO passivation through hydrogen was firstly studied for the Cz-Si material [162], [132], [163].

3 MATERIALS AND METHODS

In this thesis, two main themes were emphasized: silicon purification and light induced degradation (LID) characterization in multicrystalline silicon. Both seen as crucial because, combined, they provide an important amount of information about the quality of the material. It is also among these themes that several opportunities are found for new production routes investigations. The table 5 presents the investigations and considered data according to the manufacturing processes of multicrystalline silicon by the metallurgical route.

Table 5 - Studies and data considered according to the manufacturing processes of multicrystalline silicon by the metallurgical route

	Process	**Study**	**Data to characterization**
Quartz	-	Quartz characterization	Impurities
MG Si	Reduction	MG-Si characterization	Impurities
SoG Si	Purification	UMG-Si characterization	Impurities
Wafer *(comercial)*	Ingot growth +wafering	Wafer characterization	Lifetime PL images LID

Source: Author

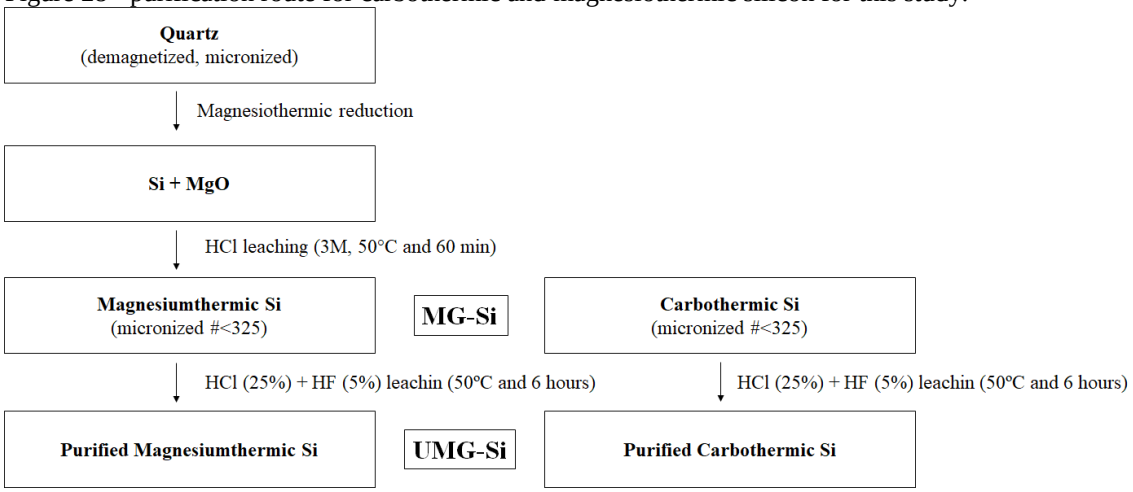
3.1 ICP-OES impurities measurements of Brazilian quartz, MG-Si and UMG-Si

To measure the Brazilian quartz acquired in IPEN and to investigate the purification route of acid leaching, the raw material used this high purity granulated quartz that goes through washing and sorting; micronization; and magnetic separation. For the reduction of Quartz into metallic silicon, magnesiothermic reduction were processed at IPEN laboratory. The resulting material is Si with MgO, which was then HCl leached following similar parameters from R. Ramos work on magnesiothermic reduction [32]. Items 2.1.1 and 2.1.2 describes the processes and characterizations techniques involved in this topic.

Another route is taken into account, the carbothermic reduction. A carbothermal silicon was acquired. The silicon chunks was micronized providing a metallic silicon powder.

Both magnesiothermic and carbothermic silicon was subjected to a leaching in HCl + HF solution following similar parameters from Ebrahimfar and M. Ahmadian work [33]. The objective was to understand the purification capacity of this process, also provide a view for subsequent process, such as Directional Solidification. The impurities content in the materials resulted from processes are measured with ICP-OES and compared with the literature [32], [33] and [12]. Figure 28 shows the purification route for carbothermic and magnesiothermic silicon. The magnesiothermic and the carbothermic silicon was micronized and selected in a shank with #<325. The particle size was chosen smaller as possible, in accordance with Ebrahimfar and M. Ahmadian [33] that shows higher purification yield with smaller particle sizes.

Figure 28 - purification route for carbothermic and magnesiothermic silicon for this study.



Source: author

3.2 Characterization of commercially available mc-Si wafers

Before LID and LeTID investigations photoluminescence images calibrated by QssPC were performed with wafers prepared for this study: as-cut, gettered and gettered + fired (standard firing process). Colored and grayscale lifetime scales, measured by PL equipment, from 0-600µs, were chosen. Both shows different characteristics in the same wafer.

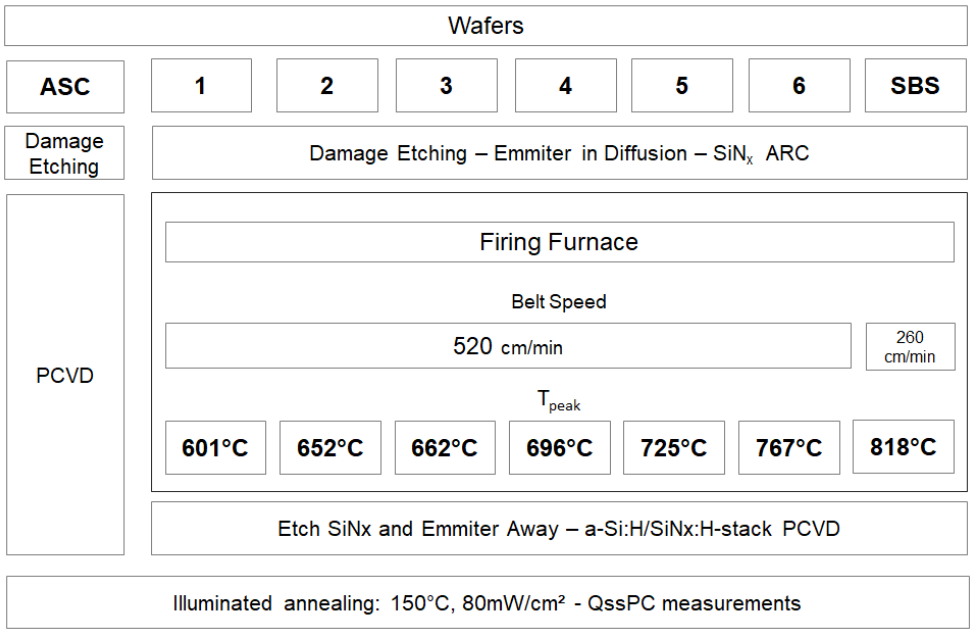
3.2.1 Investigations on LeTID

Commercially available p-type high performance multicrystalline (HPMC) silicon wafers were used to study the effects of different firing temperature profiles on minority carrier lifetime degradation induced by light and elevated temperatures. Neighboring wafers from about 25% of the ingot height, with approximately 1 Ω-cm resistivity are taken from a center brick of a G5 ingot.

Wafers were separated in eight groups, among which all eight groups were subjected to the initial damage etching in a HNA-solution (HF, nitric acid, acetic acid) as well as the final surface passivation, according to Figure 29. The first group of wafers (ASC) did not go through any additional high temperature steps. The other seven wafer groups went through a two-sided $POCl_3$ emitter in diffusion in a tube furnace, a dual side deposition of a hydrogen rich SiN_x anti-reflective coating (ARC), and simulated contact firing, without metal paste screen-printing and contact formation.

Different belt furnace conditions were used for all seven wafer groups. After the different firing profiles, the ARC and phosphorus emitter layers were etched away in new NHA-solution. An a-Si:H/SiNx:H-stack surface passivation layer was deposited by plasma enhanced chemical vapor deposition (PECVD) on both sides of the wafers [121] on all eight groups of wafers. Surface recombination velocities of less than 5 cm/s are routinely obtained using this process [111].

Figure 29 - Process flow diagram investigating the effects of different Firing Furnace Conditions on LeTID. Wafers was separated in eight groups.

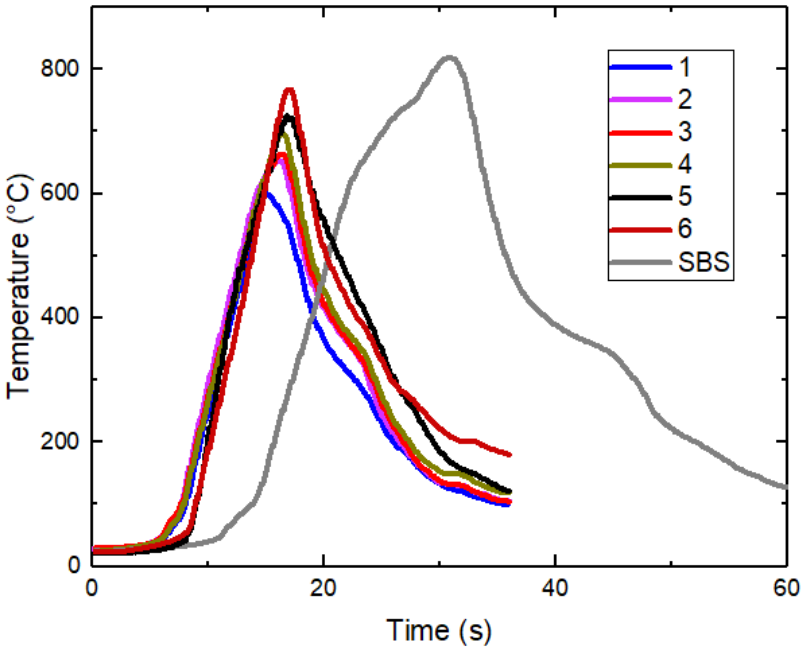


Source: Author

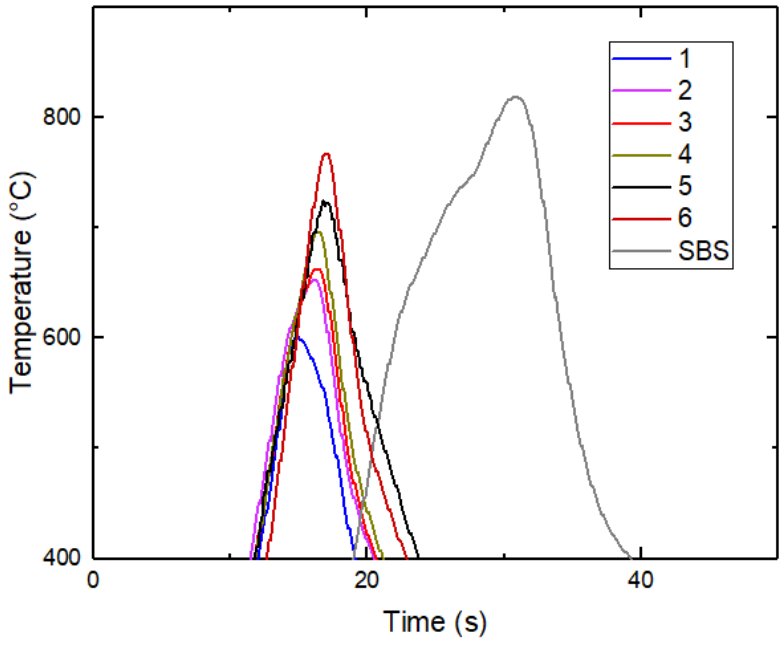
The simulated firing process was performed in a belt furnace with four temperature zones. The peak temperature (T_{peak}) was varied by adjusting the temperature setting of the last zone. Peak firing profiles temperatures ranging from 601°C, 652°C, 662°C, 696°C, 725°C, and 767°C with a belt speed of 520 cm/min used on process #1 through #6, respectively. The slow belt speed (SBS) process was performed using a belt speed of 260 cm/min, and temperature settings corresponding to that of process #5. Process #5 also corresponds to the firing process used in the lab scale production of Al-BSF solar cells at Institute for Energy Technology.

The temperature profiles measured using a thermocouple are shown in Figure 30. The cooling rate between the peak temperature and 400°C differ only slightly, with values close to 50°C/s for process #1, #5, and SBS, and close to 60°C/s for process #2, #3, #4, and #6. While the cooling rate of the SBS samples is comparable to the other samples, the heating rate differ. Using the standard belt speed, the samples were heated from 400°C to peak temperature at between 60 to 85°C/s, while at slow belt speed the heating rate is 35°C/s. For comparison, we defined a thermal budget as the integral in time of the temperature curve above 600°C. The slow belt speed, with an 819°C peak temperature, resulted in a total of 12 seconds of exposure above 600°C, compared to 4 seconds in the profile #6. The thermal budget varied considerably, ranging from almost zero to 100°C.s, 120°C.s, 190°C.s, 310°C.s, up to 800°C.s for process #1, #2, #3, #4, #5, and #6, respectively, while 1550°C·s for the SBS. All processing temperatures were kept below 230°C for the ASC wafers.

Figure 30 – (a) Firing temperatures profiles resulted for the seven groups of wafers that went through firing. (b) Peak temperature zoom in.



a



b

Source: Author

Approximately the same areas on neighboring wafers were evaluated in this study to minimize the quality variations from crystal defects normally observed in multicrystalline wafers. Injection dependent minority carrier lifetimes were measured using quasi steady-state photoconductance technique (QssPC), with a Sinton lifetime

tester WCT-120TS. Reported lifetime values are extracted at $\Delta n \approx 0.1 \times p_0$, corresponding to an injection level, Δn, of approximately 1.5×10^{15} cm^{-3}.

Prior to the degradation study all wafers were subjected to 200°C dark annealing (DA) for 20 minutes to obtain higher initial lifetimes [144]. The potential effect of this dark annealing on LeTID were considered negligible due to the short time [149]. The degradation upon illuminated annealing was determined by heating the sample to 150°C on a hotplate with simultaneous illumination with an intensity of approximately 80mW/cm² using a LED lamp. The samples were moved to the QssPC for lifetime measurements at room temperature at different time intervals. As samples from the same group exhibited reproducible degradation curves, a representative wafer from each group were selected for comparison with other groups.

4 RESULTS AND DISCUSSION

4.1 ICP-OES impurities measurements of Brazilian quartz, MG-Si and UMG-Si

Table 6 presents the data of impurity determination obtained by ICP-OES analyses of: micronized and demagnetized granulated quartz; A - magnesiothermic silicon leached with HCl (3M, 50ºC and 60 min); B - the commercial carbothermic silicon. In addition, is shown reference data from Ramos of a magnesiothermic silicon leached with HCl (3M, 80ºC and 120 min) and a reference data of main elements purity for metallurgical-grade silicon.

The impurities measurements for the demagnetized micronized quartz shows low level for all elements, especially B and P with <2,0ppm and 17ppm ± 1, respectively. Comparing with reference data for UMG-Si from D. Sarti and R. Einhaus [12] , it is possible to consider that this is raw material with good quality. Unfortunately, the impurity measurements for the magnesiothermic silicon leached with HCl (3M, 50ºC and 60 min) shows a considerable increase in the amount of impurity between processes, namely B (from <2,0ppm to 3493ppm), Mg (from 5,2ppm to 33424ppm), Mn (from 96,pm to 613ppm) and Na (from 2ppm to 2421ppm). These impurities have been introduced into the silicon material during magnesiothermic reduction, mainly from the introduced Mg material with extra impurities and from the crucible.

The micronized commercial carbothermic silicon impurities measurement indicates that impurities introduction may also have occurred during the carbothermic reduction. The amount of measured iron is high (5831ppm) and it may have been introduced during the carbothermal reduction process, but it may also have originally come from a lower quality raw material. Most impurity contents of the elements from micronized commercial carbothermic silicon are higher compared with the magnesiothermic silicon leached with HCl. This can be explained by the magnesiothermic silicon HCl leaching process, which is done mainly to remove MgO, but promotes further purification of the silicon material. It may also relate to a lower quality raw material used in the commercial carbothermic reduction.

The impurity data from the R. Ramos experiment [32], whose HCl leaching parameters were set at 3M, 80º C and 120 min, revealed fractions found in magnesium at about 2032 ppm, an boron element with 897 ppm. Ramos experiment lead to a silicon with lower impurity levels compared with both magnesiothermic silicon leached with

HCl and micronized commercial carbothermic silicon, due mainly to the longer time and higher temperature in the HCl leaching. Still, the Ramos experiment showed a high magnesium content, which means that the leaching conditions were not enough to carry out the MgO product from the previous process of magnesiothermic reduction.

Comparing the impurity levels in Table 6 from magnesiothermic silicon leached with HCl and micronized commercial carbothermic silicon with the impurities commonly found in the commercial MG-Si [12], it is observed that the values are in accordance with a metallurgical grade silicon, with the most exception of Boron which exceeded by far the reference.

Table 6 - Impurities data obtained by ICPOES; reference for metallurgical, ultra-metallurgical and solar grade silicon.

	Demagnetized micronized quartz	**(A) magnesiothermic silicon leached in HCl (3M, 50°C, 60 min)**	**(B) Micronized carbothermic silicon (commercial)**	**REF [32] magnesiothermic silicon leached in HCl (3M, 80°C, 120 min)**	**REF [12] MG-Si**
Zr	16,9 ± 0,9	98 ± 4	22,6 ± 0,6	4,0	
Li	4,1 ± 0,2	2,0 ± 0,7	< 0,5	0,5	
Na	22 ± 4	2421 ± 25	15 ± 4	49,5	
Ti	109 ± 6	93 ± 8	308 ± 8	21	200
Al	18,5 ± 0,7	118 ± 20	262 ± 9	239	200
K	2,91 ± 0,09	14,9 ± 0,1	2,6 ± 0,2	25	
Fe	209 ± 7	88 ± 24	5831 ± 121	6,0	2000
Ba	1,72 ± 0,07	< 1,0	14,4 ± 0,5	1,0	
Ca	< 4,0	9,2 ± 0,5	252 ± 8	5,6	600
Cr	2,5 ± 0,3	32 ± 2	622 ± 63	2,6	50
Co	< 1,5	< 1,5	< 1,5	1,5	
Mg	52,2 ± 0,7	33524 ± 214	66 ± 3	2032	
Mn	9,6 ± 0,2	613 ± 40	70 ± 2	9,6	
Sr	< 2,0	< 2,0	18,0 ± 0,7	2,0	
Sn	64,1 ± 0,8	34 ± 5	< 2,0	5,4	
Cu	< 1,0	21 ± 2	19,5 ± 0,7	3,0	
V	< 2,0	< 2,0	9,2 ± 0,2	2,0	
B	< 2,0	3493 ± 162	2590 ± 110	897	40
P	17 ± 1	24,0 ± 0,5	45 ± 6	5,4	20
TOTAL		**40591,60**	**10151,30**	**3389,90**	
% purity*		**0,9594084**	**0,9898487**	**0,996606**	

Source: Author

Table 7 presents the data of impurity determination obtained by ICP-OES analyses of: C- magnesiothermic silicon leached with HCl (25%) + HF (5%) (50ºC and 6 hours); D - the commercial carbothermic silicon leached with HCl (25%) + HF (5%) (50ºC and 6 hours). In addition, is shown reference data from reference [12] of main elements purity for ultra-metallurgical and solar-grade silicon.

The impurities measurements for the magnesiothermic silicon leached with HCl (25%) + HF (5%) shows a lower level for all elements compared with previous

purification process (magnesiothermic silicon leached with HCl showed in Table 6). The most exception of Boron that showed a large increase in content, from 3493ppm to 7531ppm. The magnesium content decrease from 33524ppm to only 3ppm, showing a high MgO removal from the material. Fe and Sn also showed an increase in content, which suggest a slight contamination between processes. P content didn´t change between processes.

The impurities measurement from the micronized commercial carbothermic silicon leached with HCl (25%) + HF (5%) indicates that overall impurities has been slightly better removed from this material, showing a similar or better impurity level in each element. Excess iron showed an important decrease, from 5831ppm to 36,2ppm. Boron content showed a large increase in content, from 2950ppm to 7230ppm.

Comparing the impurity levels in Table 6 from (C) and (D) with the impurities commonly found in the commercial UMG-Si and SoG-Si [32], it is observed that the values are in accordance with a ultra-metallurgical grade silicon, with the most exception of Boron which exceeded by far the reference. Phosphorous content also exceeded the UMG-Si reference by a factor of 3.

Table 7 - Impurities data obtained by ICPOES for: C - resulted magnesiothermic silicon leached with HCl (25%) + HF (5%) (50ºC and 6 hours); D - the commercial carbothermic silicon leached with HCl (25%) + HF (5%) (50ºC and 6 hours); reference for ultra-metallurgical and solar grade silicon.

	(C) magnesiothermic silicon leached in HCl and HCl (25%) + HF (5%)	**(D) carbothermic silicon leached in HCl and HCl (25%) + HF (5%)**	**REF [32] UMG-Si**	**REF[12] SoG-Si**
Zr	4,35 ± 0,03	1,2 ± 0,1		
Li	0,74 ± 0,05	< 0,5		
Na	618 ± 43	556 ± 18		
Ti	51,5 ± 0,3	4,1 ± 0,3	5	1
Al	31 ± 4	30,5 ± 0,3	50	2
K	4,4 ± 0,6	< 2,0		
Fe	165 ± 14	36,2 ± 0,7	150	10
Ba	< 1,0	< 1,0		
Ca	5,3 ± 0,3	9 ± 2	500	2
Cr	1,9 ± 0,1	< 1,0	15	1
Co	< 1,5	< 1,5		
Mg	< 3,0	22 ± 4		
Mn	76 ± 3	2,63 ± 0,05		
Sr	< 2,0	< 2,0		
Sn	203 ± 1	32 ± 3		
Cu	< 1,0	< 1,0		
V	< 2,0	< 2,0		
B	7531 ±515	7723 ± 12	30	1
P	42 ± 3	40 ± 2	15	5
TOTAL	**8744,69**	**8469,13**		
% purity*	**0,99125531**	**0,99153087**		

By subtracting the amount of impurities from the total sample analyzed, it is possible to calculate an approximately final percentage of silicon purity, that is, 95,94% for (A), 98,89% for (B), 99,12% for (C) and 99,15% for (D). Results of purity are slightly lower then the obtained by Ramos, with a result of 99.66% purity. However, the high Boron content in the resulting materials itself is responsible for the insufficient purity for the material to be considered UMG-Si. Reaching a Boron content of 50ppm, for example, materials (C) and (D) would achieve a purity of 0.9987% and 0.9999%, respectively. Therefore, a process for Boron removal, such as slagging, is necessary for the materials to reach an ultra-metallurgical grade purity. After a successful slagging, the ultra-metallurgical grade silicon can already be used in the manufacture of solar cells. For this, the material can be processed in the directional solidification furnace, since the process itself is a purification step. Other impurities such as Fe can also be further removed in the gettering process.

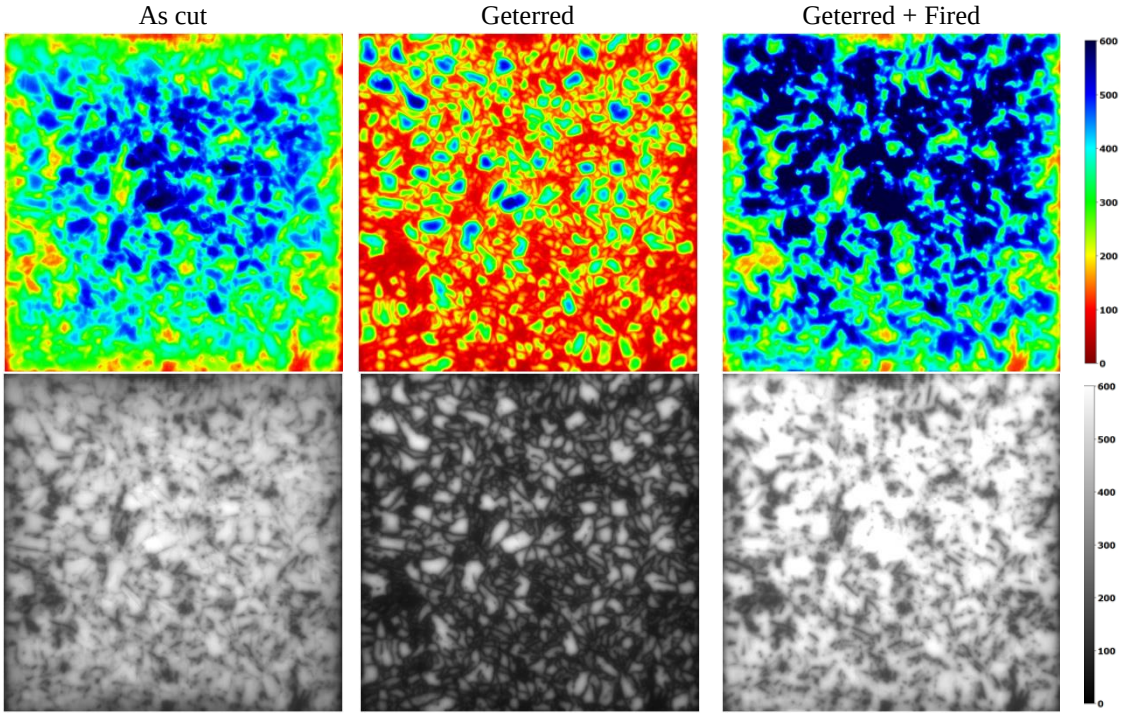
4.2 Characterization of commercially available mc-Si wafers

The PL images of the as-cut (a), gettered (b) and gettered + fired (c) is shown in Figure 31. In as-cut wafers PL images, it is possible to observe in the colored scale that there are a number of intra-grained regions with high lifetimes, between 500 and 600µs. There are other grains, at the edges of the wafer, with intra-grain regions showing lifetimes between 300-400µs. Lastly, low lifetime regions in yellow and red that appear to be intra-grains or a specific crystallographic defects. In the gray scale PL image of the as-cut wafer, it is seen in fact that there are crystallographic defects, marked as dark scratches, caused by the disordered crystallographic growth, providing active regions for recombination of the minority charge carriers, thus reducing the lifetime.

In the gettered wafer, a drop in the lifetime is seen in the vast majority of points in the PL image. At first, this seems counter intuitive. Even the intra-grain regions are affected by a decrease in lifetime, and it is possible to see some smaller blue areas in the PL color image, with lifetimes between 500-600µs, which in as-cut wafer were larger and more numerous. Much of the wafer lifetimes points, as red and yellow, are between 100-300µs. In the gray scale PL image, it is possible to better observe the cause of the decrease of the lifetime. Grain boundaries, previously almost imperceptible in the as-cut wafer image, are now strongly enhanced showing low lifetimes. With this, we replicate

the results presented by H. Sio et al. [120], showing this lifetime decrease between as-cut and gettered samples. As discussed by H. Sio et al. [120], the grain boundaries considerably increase their active recombination due to the diffusion of the impurities contained in the intra-grain regions towards the boundaries, during the gettering process. Thus, the grain boundaries retain a greater amount of impurities, and this grain boundary-impurity binding generates a highly active region for recombination, which negatively affects even the lifetime in the intra-grain region.

Figure 31 - PL images of as-cut, gettered and gettered + fired wafers with colored and gray lifetime scales from 0-600µs



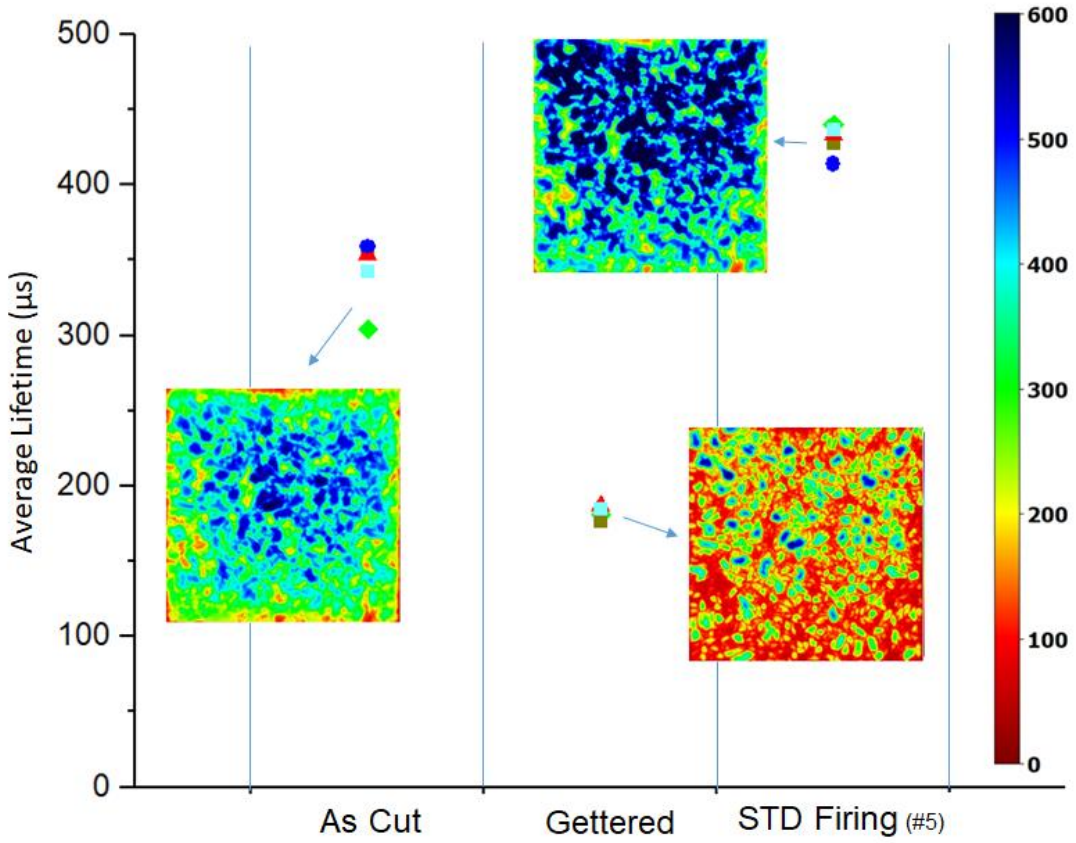
Source: author

The described decrease of the lifetime seen in gettered samples is fortunately overcame by the firing process. The process of rapid heating of the wafer to about 750°C for about 4 seconds, as discussed by H. Sio et al. [120], generates an in-diffusion of hydrogen from the passivation layer, which passivates the grain boundaries. These regions became no longer high active for recombination, considerably increasing the average lifetime of the wafer. This is observed in the PL image of the gettered + fired wafer, where there are blue regions, showing lifetimes between 500-600µs, in greater quantity and even “attached” to each other. There were still red and yellow regions in the color PL image, showing lifetimes between 100-300µs, which are the same regions seen

in the as-cut wafer, but with a visible slight improvement in the lifetime. The crystallographic dislocations can be better seen in the gettered + fired grayscale PL image. This means that, as also discussed by H. Sio et al. [120], hydrogen does not passivates dislocations as it does with grain boundaries. Therefore, the importance of increasingly precise crystallization techniques to avoid dislocations, thus allowing the production of multicrystalline silicon wafers with increasingly lifetimes, comparable to monocrystalline wafers lifetimes, thus keeping the competitiveness of the multi-Si technology. The grain boundaries recombination activity is extensively investigated by A. Krzysztof et al. [121].

To elucidate the wafer average lifetime decrease and increase after the gettering and the firing processes, Figure 32 shows the result of the lifetime, measured by the PL equipment and calibrated by QssPC, before and after each process. The average lifetimes in as-cut wafers were between 300-370µs. After gettering, the average lifetime drops to less than 200µs. After the standard (STD) firing, there is a lifetime recovery to more than 400µs. It is important to note that the average lifetimes are showed. If the harmonic lifetime of the wafer were calculated, these values would be considerably lower, and would better represent the efficiency result that these wafers would achieve in a photovoltaic cell. However, the aim here is the comparison between processes and neighboring wafers.

Figure 32 – Average measured lifetimes with the PL equipment with calibrated by QssPC in as-cut, gettered and gettered + fired wafers. Colored scale PL images shows a selected wafer.



Source: author

4.2.1 Investigations on LeTID

Resistivity and reflectiveness of the produced wafers by the different routes was measured in wafers from numbers 160 to185, the mass of each wafer was measured and the thickness calculated. PL images was taken and the average lifetime obtained with the PL equipment. Results are shown in Table 8. The measured values are compatible with the expected. The resistivity are between 1.1-1.2Ω.cm, reflectiveness are between 10.5-12.7% and thickness, 166-168µm, with the exception of the SBS3 samples that showed a slightly higher mass and thickness. Average lifetime were between 300-350µs for ASC samples, close to 180µs for gettered samples and 410-440µs for gettered + fired samples of all profiles. The exception again was the SBS3 samples, which resulted in a

very low lifetime of 21-36µs. The PL images gives more indicative about the wafers quality, as show below.

Table 8 – Measured resistivity, reflectiveness, mass and calculated thickness of the produced wafers by the different routes. Average lifetime was obtained with the PL equipment

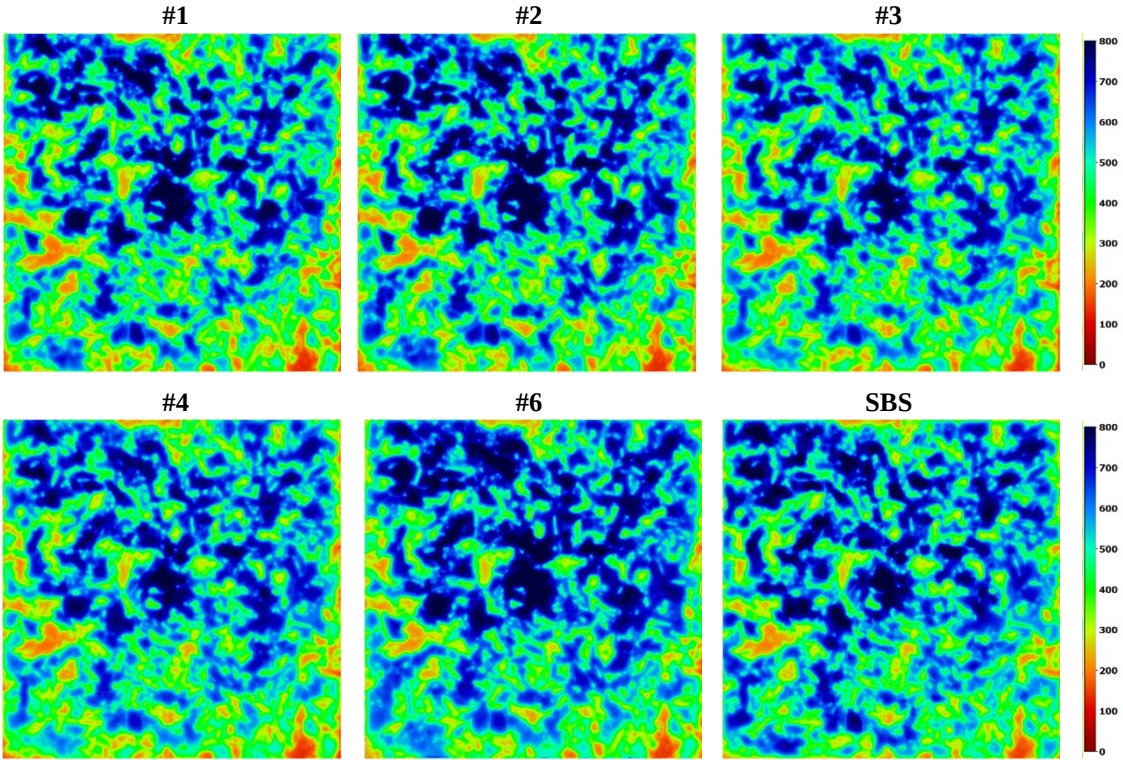
Wafer Number	Process	Mass (mg) after process	Thickness (µm)	Resistivity (Ω.cm)	Reflectiveness (%)	PL average lifetime (µs)
160	As Cut	9491,5	167,5	1,14		304
162	Geterred + Fired (#5)	9463,1	167,0	1,1		427
163	As Cut	9532,4	168,2	1,13	11,8	354
164	Geterred	9530,7	168,2	1,22	11,2 11,1	185
165	Geterred + Fired (#5)			1,14	11,1	434
166	As Cut	9519,5	168,0	1,13	11,1	354
167	Geterred	9546,1	168,4	1,21	11,1	187
168	Geterred + Fired (#5)	9434,00	166,4	1,11	10,8	437
169	As Cut	9521,70	168,0	1,14	11,2	342
170	Geterred	9583,30	169,1		10,8	176
171	Geterred + Fired (#5)	9522,80	168,0			414
172	As Cut	9607,90	169,5	1,14	10,5	359
174	Geterred	9562,90	168,7		10,7	181
175	Geterred + Fired (#5)	9447,40	166,7		10,5	440
178	#1	9525,50	168,1	1,14	10,4	426
179	#3	9531,60	168,2		10,5	430
180	#4	9502,40	167,7		10,2	431
181	SBS3	9859,80	174,0		13,2	21
182	#6	9445,80	166,7		10,2	424
185	SBS3	9770,70	172,4		12,7	36

Source: Author

4.2.1.1 PL images and QssPC measurements for each Firing Profile

To investigate the impact of different firing furnace conditions in the light and elevated temperature-induced degradation (LeTID), samples that went through gettering and firing in different temperature profiles were firstly imaged by PL. Figure 33 shows one selected PL image for each firing profile with the corresponding lifetime colored scale, from 0 to 800µs. Small variations are perceptible between colored PL images, perhaps one larger grain in the center of the wafer from profile #6 is the main observable difference.

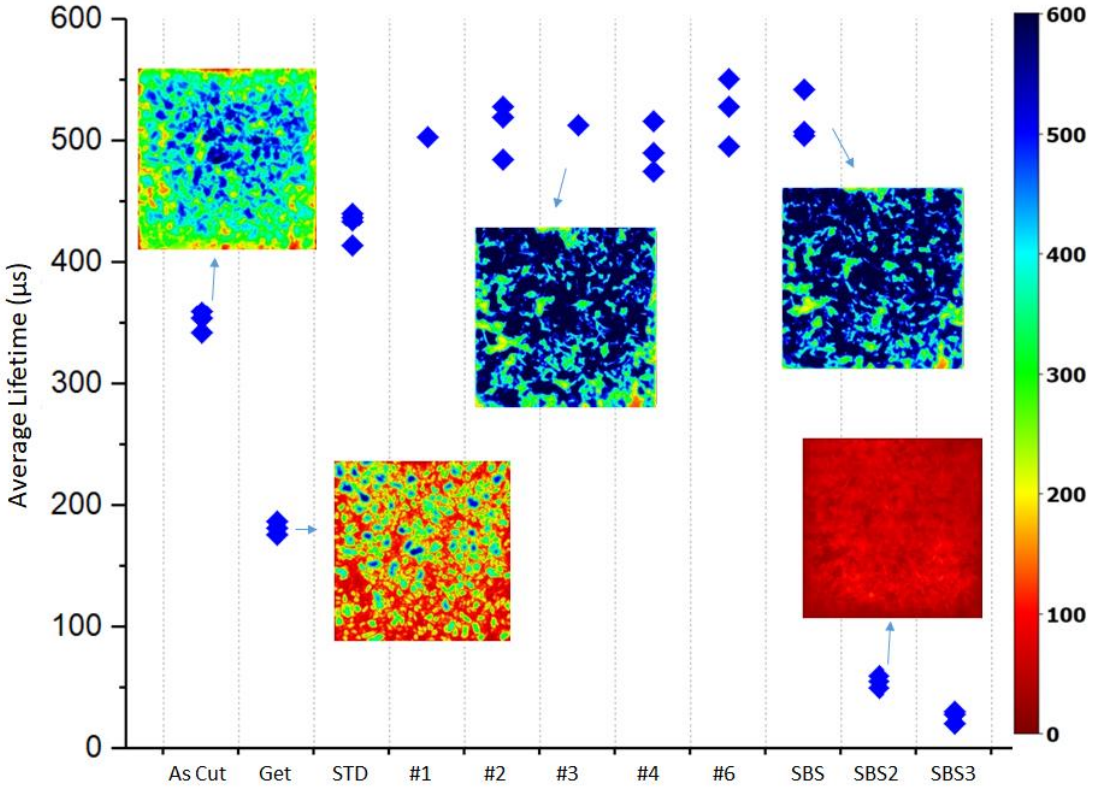
Figure 33 - One selected PL image for each firing profile. The image is color scaled, from 0 to 800ms.



Source: Author

In Figure 34 the average lifetime for each measured wafer and according to the firing profile is given. First as-cut, gettered, gettered + fired wafers, previously showed, were compared with PL images of wafers from the others firing profiles, showing an increase in lifetime between profile #5, considered as standard (STD), and the others. The longer time that profile #5 samples stayed in the desk, in addition to the small increase in grain size between neighboring wafers, the wafers numbers ranging from 165 to 230, are possibly more relevant to the resultant measured average lifetime by PL equipment than the actual differences caused by different firing profiles.

Figure 34 – Average lifetime measured with the PL equipment with calibrated by QssPC for each wafer and according to the firing profile. Colored scale PL images shows a selected wafer.



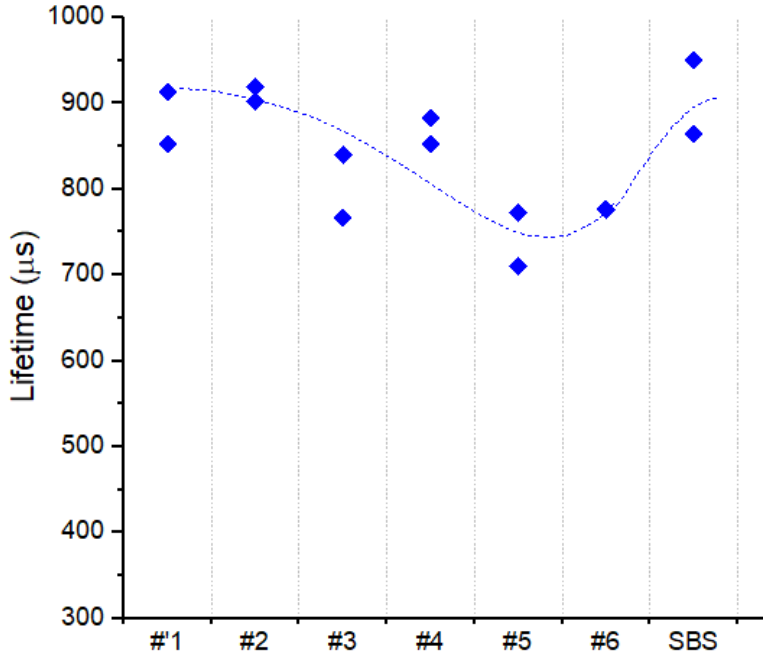
Source: Author

To further analyses the resulted wafer lifetime for different firing profiles, new measurements were carried out with QssPC after a 20 minutes dark annealing, before the evaluation of the lifetime degradation and recovery under illuminated annealing conditions. Figure 35(a) shows the measured lifetimes for the firing profiles from #1 to #6 and SBS. A blue dash line, serving as a guide for the eye, indicates a decrease in lifetime between profiles #1 and #6, from 850-920µs to approximately 780µs. After the lifetime decrease, between profile #6 and SBS, there is an increase in lifetime, from 780µs to 860-950µs.

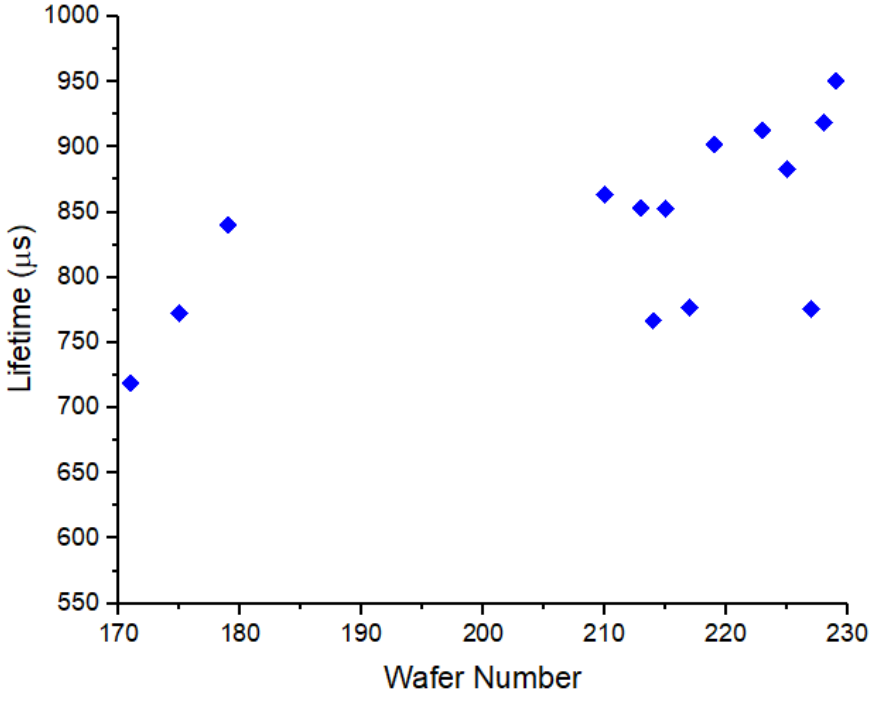
To exclude the hypothesis of a higher influence on the wafer lifetime from the ingot height, even for these neighboring wafers, i.e. a possible slight improvement in lifetime due to the small increase in grain size, Figure 35(b) shows QssPC lifetime measurements after 20 minutes dark annealing related with the wafer number. Although there is a lifetime increasing trend with larger wafer numbers, some wafers showed considerably lower lifetimes between wafers number 210 and 230. These wafers have gone through firing profiles that resulted in lower lifetimes showed in Figure 35(a), such

as the #5 profile. Thus, we assume that the firing profiles influences the lifetime prompt measurement after the 20 minutes dark annealing.

Figure 35 – (a) Measured lifetimes for the firing profiles from #1 to #6 and SBS. A blue dash line, serving as a guide for the eye; (b) QssPC lifetime measurements after a 20 minutes dark annealing related with increasing wafer number.



(a)



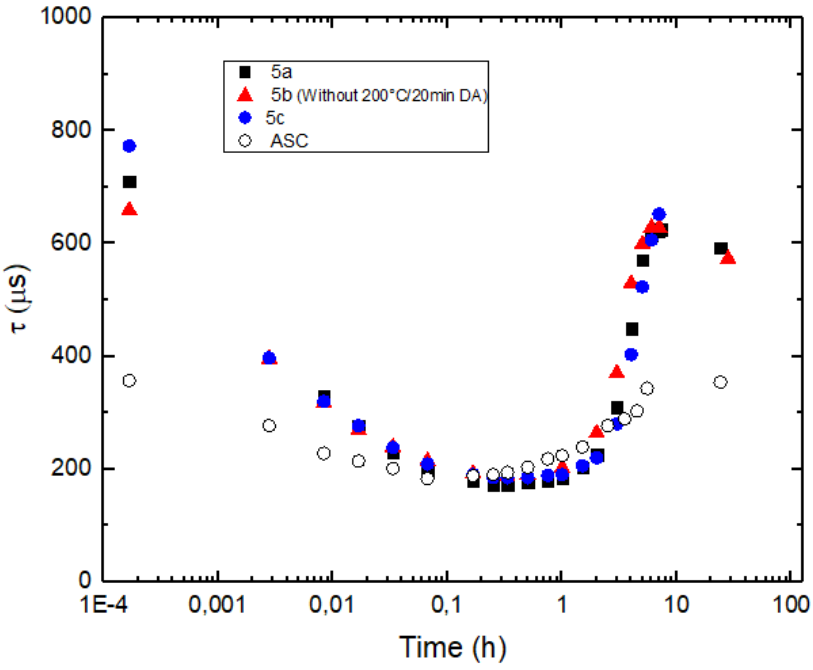
(b)

Source: Author.

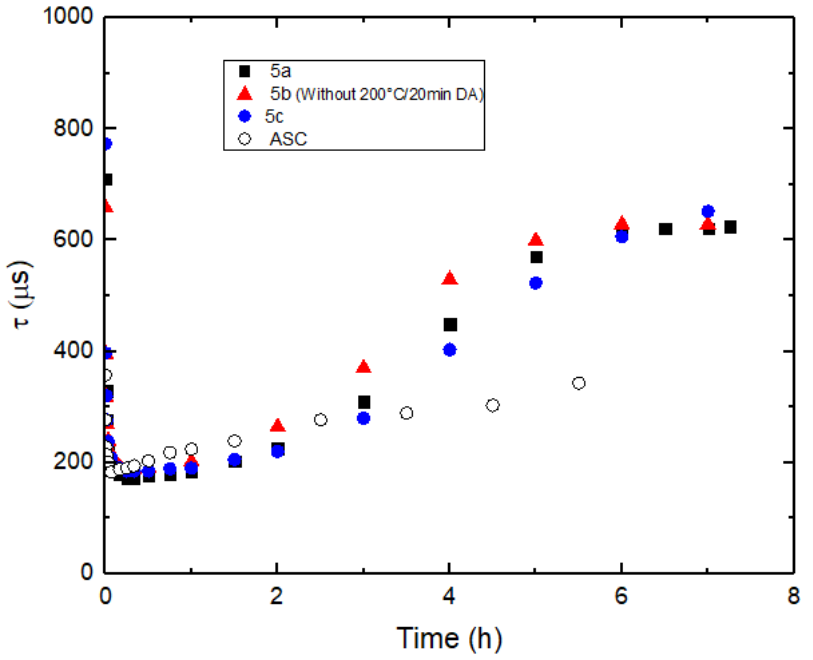
4.2.1.2 Lifetime evaluation under illuminated annealing for different firing profiles

A degradation and recovery curve is presented in Figure 36 for the selected ASC wafer under illuminated annealing at 80 mW/cm² and 150°C. The ASC initial lifetime was 360µs, while a minimum lifetime of 185µs occurred after about 2 minutes. This corresponds to 51% of the initial lifetime. Recovery of the lifetime in the sample started immediately after this 2-minute mark, reaching a lifetime of 345µs after about 5 hours and 355µs after 24 hours, i.e. almost a full recovery of its initial lifetime. According to reference [151], LeTID is only activated when subjected to firing temperatures above 650°C. ASC samples, despite having a double-sided surface passivation layer consisting of hydrogenated amorphous silicon, went through temperatures not higher than 230°C in the PECVD process. Thus, we assume that LeTID has not been activated and that boron-oxygen related light induced degradation (BO-LID), therefore, is the main lifetime limiting defect in the ASC samples.

Figure 36 – a) ASC and firing process #5 illuminated annealing curves at 150°C, 80mW/cm², logarithmic timescale; b) same as (a) but linear timescale.



(a)



(b)

Source: Author

The repeatability of the measurements and the effects of the initial dark annealing process has been evaluated on wafers fired using firing process #5. Degradation and recovery curves under illuminated annealing at 80 mW/cm² and 150°C are obtained for one sample without the DA and two samples with the DA, shown in Figure 36. A small variation in the initial lifetime (τ_0) for the different wafers can be seen. The values

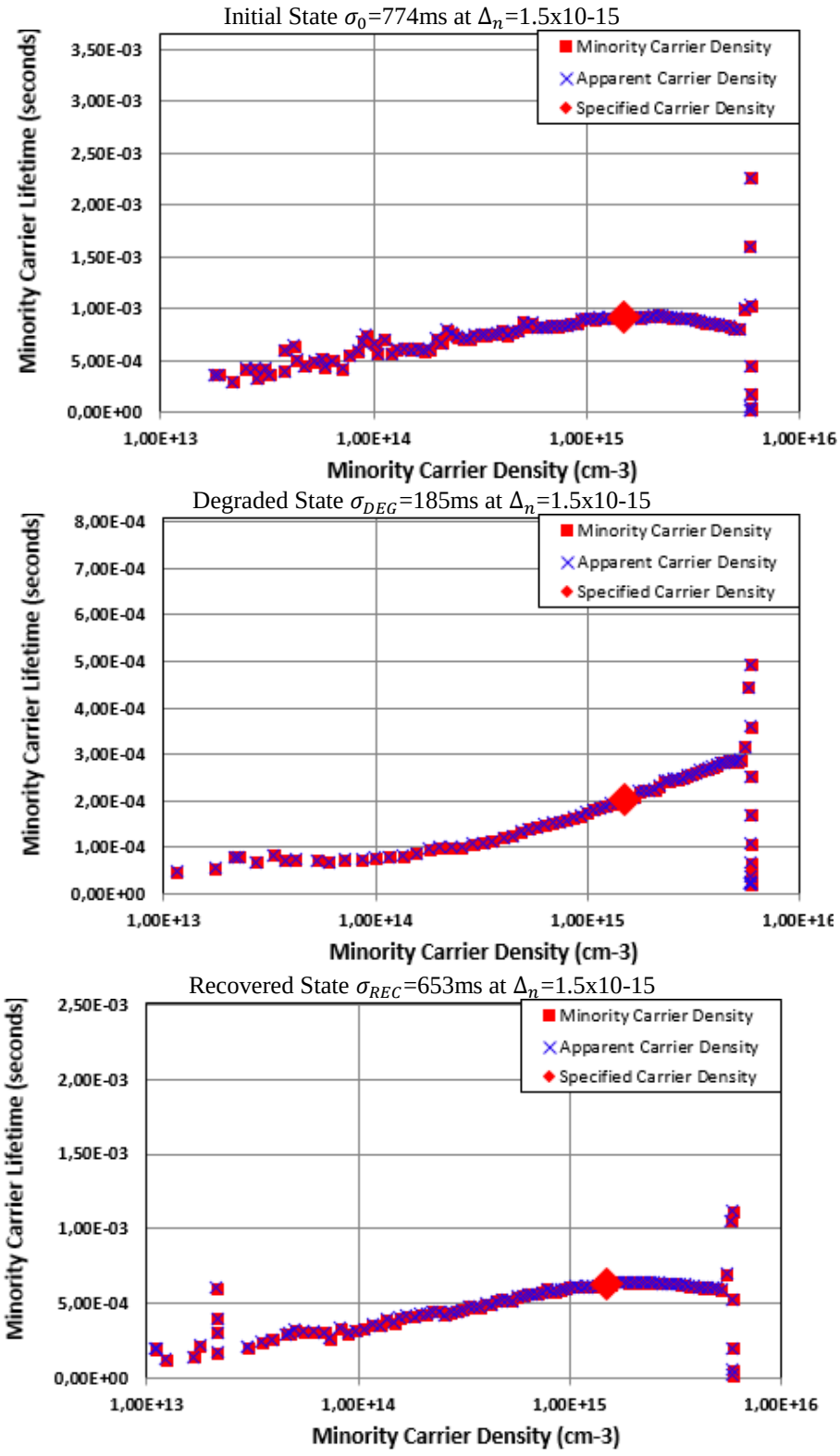
vary from 650 to 780µs, where the lowest value correspond to the sample not subjected to a dark anneal prior to measurements. Quite repeatable curves were obtained for the two dark annealed wafers. All three wafers show practically identical behavior after only 10 seconds of degradation. For these wafers, the pre-dark annealing seems to mainly influence the initial lifetimes. The minimum lifetime values for all wafers fired with process #5 occurred after about 15 minutes, with values close to 185µs, i.e. about 25% of the initial lifetime. The lifetime remained flat at 185µs between 15 and 30 minutes of Illuminated annealing. After about half an hour, regeneration started and last until approximately 7 hours. Regenerated lifetimes were close to 650µs for all samples. Between 7 to 24 hours, there were a secondary reduction in the lifetime, reaching 590µs. This secondary reduction has been attributed to a degradation of the hydrogen rich passivation layer by Sperber et al [148], [164].

While we attributed the degradation down to 51% of the initial lifetime value in the ASC wafers to BO-degradation, an additional and stronger degradation is observed in the fired samples. Using firing profiles #5 and #6 the minimum lifetime of the samples reaches as low as 25% of the initial lifetime. There are overall similarities in behavior between the BO-related degradation in unfired wafers and the total degradation in fired wafers, i.e. an initial decay followed by a recovery of the lifetime. However, the different magnitude of degradation as well as the different timescales to reach the maximum degradation and different recovery start times, as shown in Figure 36(b), lead us to conclude that two different degradation mechanisms are responsible for the different degradation and recovery curves in fired and unfired wafers. This stronger degradation is therefore attributed the LeTID defect, often observed in multicrystalline silicon wafers and solar cells thereof.

The curve that relates the lifetime of the minority charge carriers and the injection level, i.e., illumination intensity, is widely used to search for certain types of defects. In Figure 37, we show the injection dependent lifetime curves, from a wafer from the firing profile #5. The injection level (Δ_n) of 1.5×10^{-15} is the specific carrier density that is choose because it is close to the solar cell operation conditions. The initial lifetime curve and the recovered curve show similar behavior, of a maximum lifetime close to the selected injection level. The lifetime curve at degraded state shows a different behavior, with a continued increased lifetime in injections levels above the selected one. We replicate, with this, the curves from R. Søndenå et al. [134], where the LeTID injection

dependent lifetime curve (degraded state) is compared with the initial and recovered states.

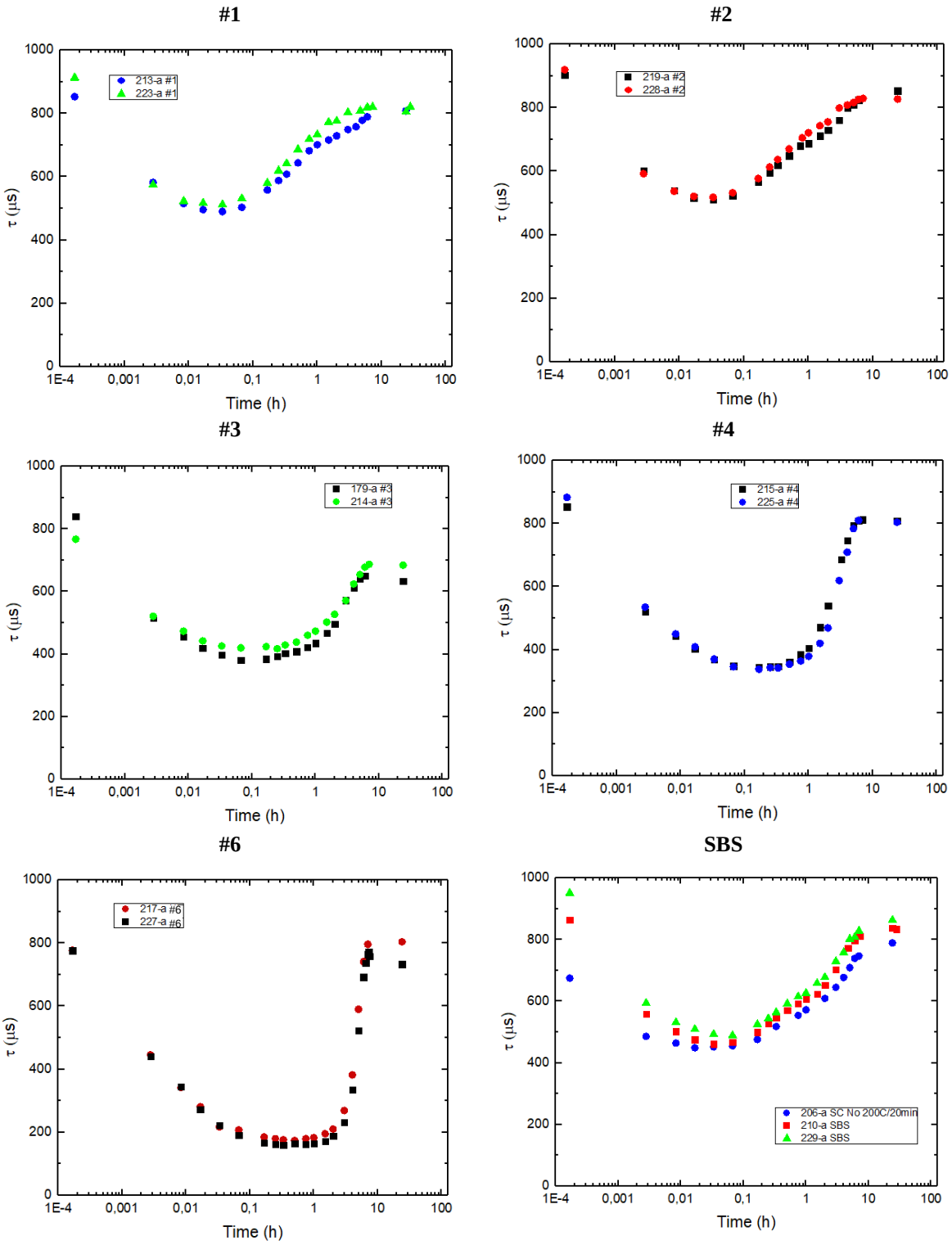
Figure 37 - Injection dependent lifetime curves, from a wafer from the firing profile #5 at different states using Sinton lifetime tester WCT-120TS.



Source: Author

The repeatability of the measurements has been evaluated on wafers fired with profiles #1, #2. #3. #4, #6 and SBS. Degradation and recovery curves under illuminated annealing at 80 mW/cm² and 150°C are obtained for one sample of each group, shown in Figure 38. Quite repeatable curves were obtained for the wafers from same firing profile. The main behavior of a degradation followed by a recovery of the lifetime, found for profile #5 and ASC, is also seen in the other groups of samples. The differences are in the minimum lifetime values, in the time to reach this minimum value, and to starting the recovery. The comparison between the degradation and recovery curves for the different firing profiles is observable through the plotting of these curves in the same graph, which is shown below.

Figure 38 - Degradation and recovery curves under illuminated annealing at 80 mW/cm² and 150°C on wafers fired with profiles #1, #2. #3. #4, #6 and SBS. Repeatability of the measurements is evaluated and wafer number is shown – "a" is the selected area of the wafer

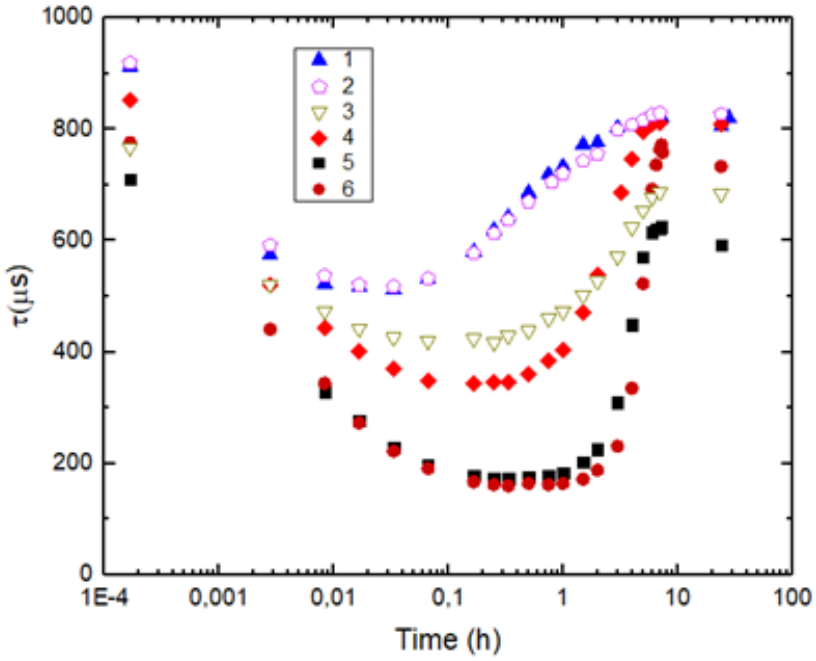


Source: Author

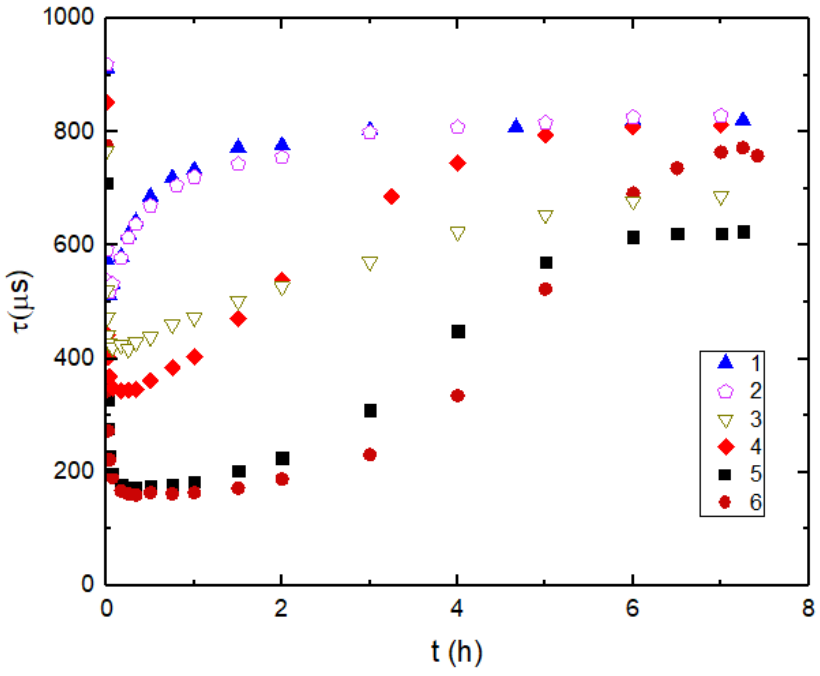
Figure 39(a) shows the degradation and subsequent recovery of the lifetimes under illuminated annealing at 80mW/cm² and 150°C in all the samples fired at the standard belt speed. Samples fired at the highest peak temperatures, i.e. from firing

process #5 and #6, show the strongest degradation, reaching minimum lifetimes of 185 and 170 µs, respectively. A gradual reduction in the degradation is observed for decreasing peak temperatures of the firing process, with quite similar lifetime evolution in samples from process #1 and #2. The minimal lifetime in samples from processes, #1 and #2 corresponds to about 50-60% of its initial lifetimes. In samples from process #5 and #6, recovery of the lifetime started after 30 minutes while for #1 and #2, recovery started right after 2 minutes. The start of the lifetime recovery after only 2 minutes is also seen in the ASC sample. For samples from firing process #3 and #4, fired at the intermediate temperatures, the magnitude of the degradation increases with increasing peak temperatures. Recovery of the lifetimes started at 15 and 20 minutes in samples from process #3 and #4, respectively. For all samples, maximum recovery was complete after 7 hours. The lifetime evolution in samples from process #1 and #2 seems more stable between 7 to 24 hours of illuminated annealing, while samples fired at higher temperatures presents a small degradation in this period. The time to onset of lifetime recovery is better visualized in linear scale in Figure 39(b). Lifetimes in samples from process #1 and #2 are largely recovered after 2 hours, while it takes more than 5 hours for the other samples.

Figure 39 – (a) Lower temperatures firing processes (#1, #2, #3, #4) and high temperature firing process (#6) illuminated annealing curves at 150°C, 80mW/cm², logarithmic timescale, compared with #5; (b) Lower temperatures firing processes (#1, #2, #3, #4) and high temperature firing process (#6) illuminated annealing curves at 150°C, 80mW/cm², linear timescale, compared with #5.



(a)



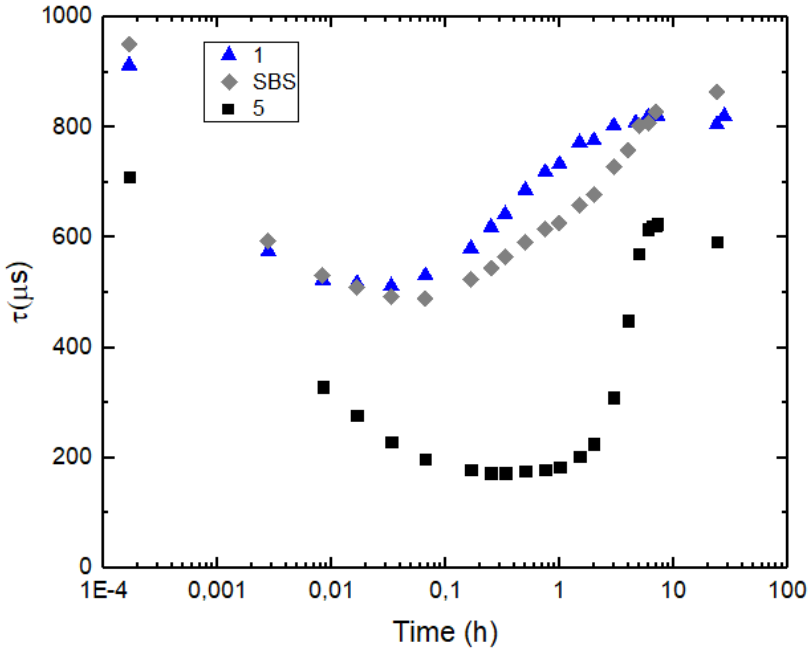
(b)

Source: Author

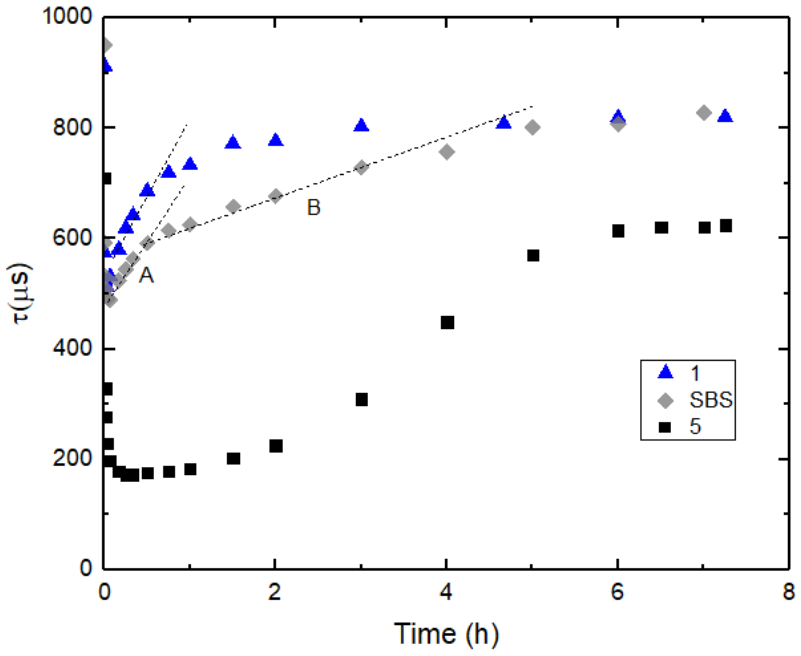
Wafers from the Slow Belt Speed firing process also exhibited reproducible degradation and recovery curves. Figure 40 presents degradation and recovery curves under Illuminated annealing for the SBS sample together with samples from firing process #1 and #5. Samples from process #1 and SBS presented similar initial, minimal

and regenerated lifetimes. The onset of the recovery for both SBS and #1 samples occurred after about 2 minutes. The lifetime evolution, shown with a linear timescale (Figure 40 (b)) shows that the recovery in the SBS sample starts after 2 minutes but has a slightly slower rate than sample from process #1. Lifetime in sample from process #1 regenerates from 490 to 700 μs in one hour, while SBS sample lifetime regenerates from 490 to 700 μs between two and three hours (letters "A" and "B" in Figure 40 (b)). However, both samples recover much faster than the sample from process #5. Like in samples from process #1 and #2, BO-related degradation is assumed the main lifetime limiting defect in the SBS samples. Although, some LeTID defect contribution is suspected due to the apparent slightly slower recovery ("B"). SBS samples had the lowest degradations and the highest initial and recovered lifetime values found despite visible belt marks from the firing furnace. We have shown that the high peak temperature in combination with a slow belt speed considerably reduces the magnitude of the degradation in silicon wafers. Thus, the thermal budget or the heating/cooling rate might be relevant parameters to predict and reduce the detrimental effects of LeTID.

Figure 40 - (a) Slow Belt Speed illuminated annealing curve at 150°C, 80mW/cm², logarithmic timescale, compared with #1 and #5; (b) Same as (a), but linear timescale; letters “A” and “B” indicates two different recovery rates in the SBS curve.



(a)



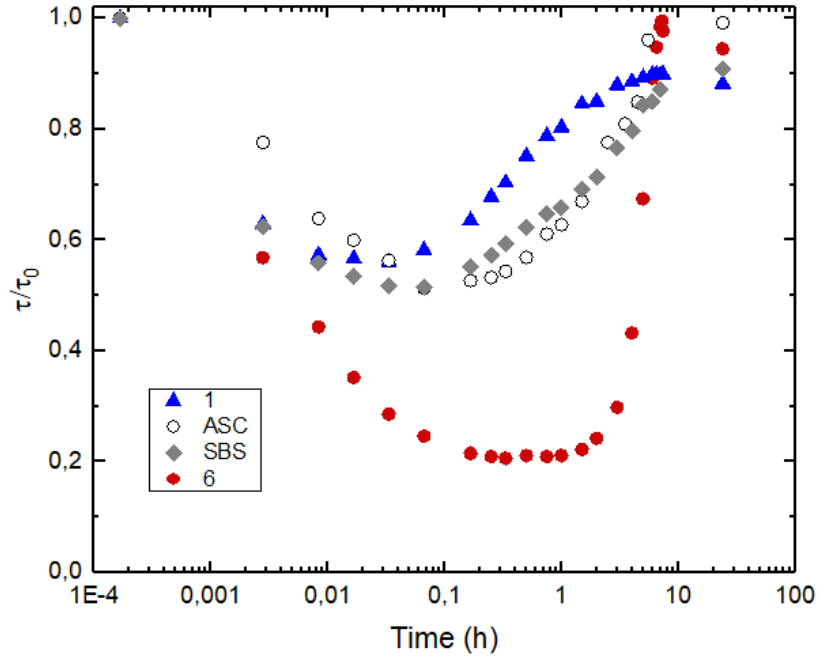
(b)

Source: Author

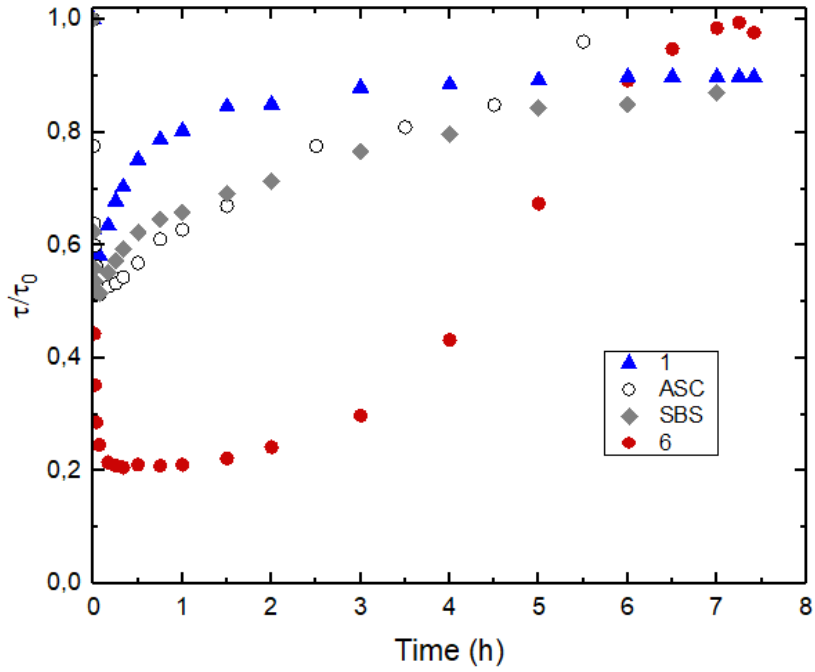
Normalized τ/τ_0 degradation/recovery curves for the SBS, ASC, processes #1 and #6 samples are presented in Figure 41. Similarities between samples from process #1, SBS and ASC are more evident, where normalized lifetime values can be compared. Normalized minimal lifetimes in sample from process #1, SBS and ASC are all between 0,5 and 0,6. Normalized minimal lifetime in sample from process #6 is considerably lower

with a value of 0.2. As mentioned before, regeneration started after around 2 minutes for samples from processes #1 and #2, ASC, and SBS. The normalized lifetime curves show many/great similarities between the ASC, #1 (& #2) as well as the SBS samples despite different processing. The magnitude of the normalized total degradation in samples from processes #1 and #2 is comparable to the degradation seen in the unfired ASC sample. We have attributed the degradation in the unfired ASC sample entirely to BO-LID, since it is not subjected to high temperature processing steps. These similarities indicate that the degradation seen in samples from firing process #1 and #2 is mainly caused by the boron-oxygen related degradation mechanism. This corresponds well with previous studies reporting an activation peak temperature higher than 650°C [151]. The firing peak temperatures of processes #1 and #2 are lower than the activation temperatures for LeTID, hence showing curves comparable to ASC. We therefore propose that the degradation curves in these three samples is mainly attributed to BO-related LID, which is not directly affected by the firing furnace conditions.

Figure 41 - (a) Normalized τ/τ0 SBS, #1, ASC and #6 illuminated annealing curves at 150°C, 80mw/m²; SBS; (b) same as (a) but linear timescale.



(a)



(b)

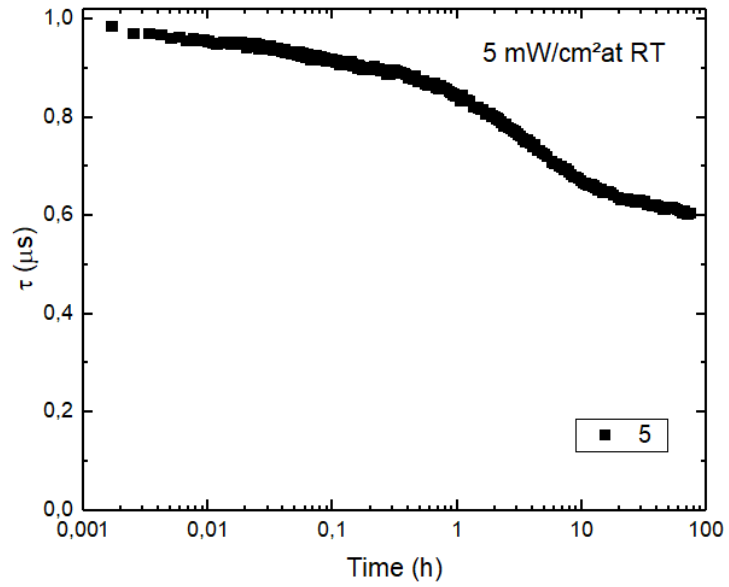
Source: Author

Lifetime measurements under illumination at room temperature on #5 and SBS samples returns a degradation curve for the first 72 hours as shown in Figure 42. Degradation caused by LeTID at RT is expected to be excruciatingly slow (or non-existent), so the main contribution is expected to be the BO-LID [37]. Under these conditions, is visible a drop to 62% and 51%, of the initial lifetime of the samples, #5 and

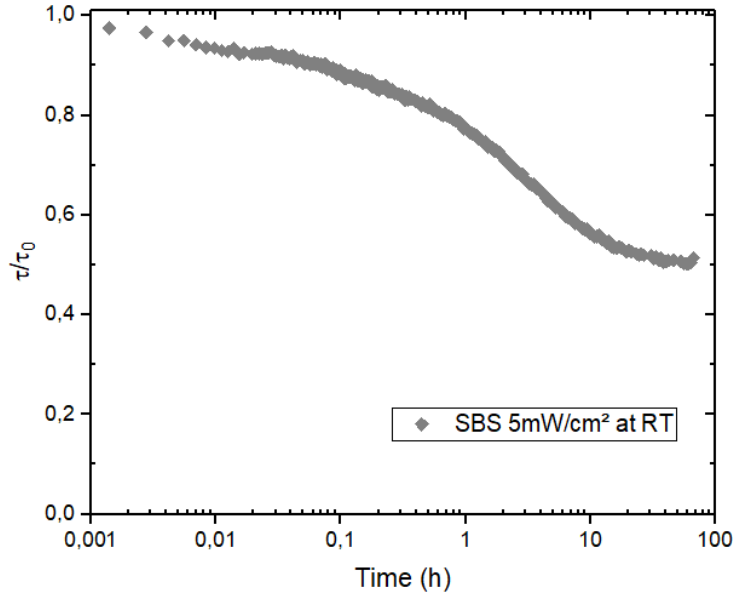
SBS, respectively. This corresponds well to the maximum degradation seen in samples after 2 minutes under illuminated annealing at 150°C, 80mW/cm². Thus, indicates that #5 and SBS firing furnace conditions did not directly affected the BO-related LID on samples, but in the case of SBS, had an impact on largely suppressing the LeTID defect.

In conclusion, wafers from process #6 and #5 degrade to a much lower lifetime upon illuminated annealing. We therefore assume that the samples from processes #6 and #5 suffer from degradation and subsequent recovery of the lifetime caused by two different mechanisms, namely the BO-LID and the LeTID, of which the latter is the most detrimental effect. The different onset times of the recovery mechanisms could explain the flat region of the lifetime curves mentioned above. Wafers from processes #3 and #4 demonstrate the possibility of partly activating the LeTID defects, while from SBS, the possibility of suppressing LeTID defects with a considerably higher thermal budget.

Figure 42 - Low light intensity (5 mW/cm²) illuminated annealing curve at room temperature for 72 hours for BO-LID performed on a #5 sample (a) and on a SBS sample (b); the lifetime was approximately 60% and 51% of initial lifetime after 72 hours, respectively.



(a)



(b)

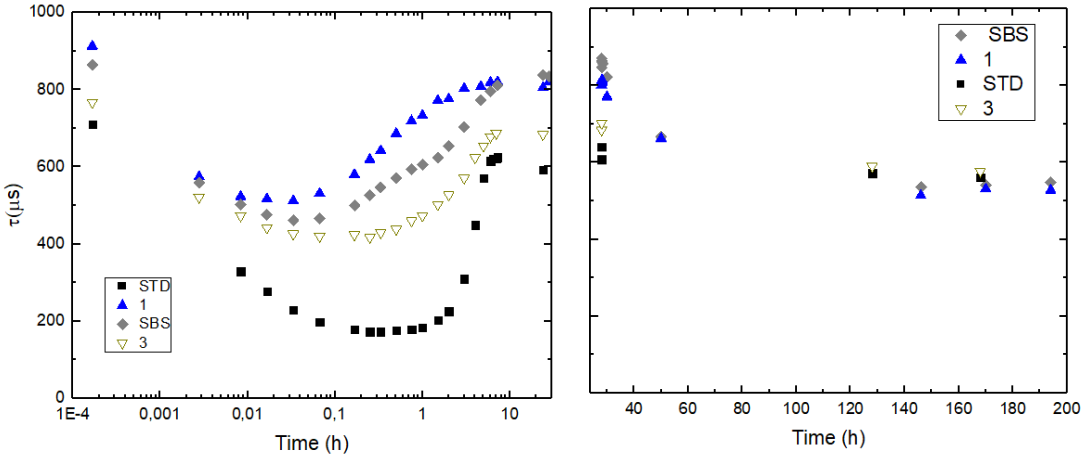
Source: Author

4.2.1.2.1 Lifetime stability after 24 hours

The stability in longer time measurements of 200 hours were tested in samples from SBS, #1, #5 and #3. The results are shown in Figure 43. After 24 hours, the samples were subjected to the same illumination of 80mW.cm^{-2}, but at room temperature. In the first measurements at room temperature, a slightly increase in the lifetime was noted for all the samples, with a higher increase for the SBS sample. However, with the passing hours, the lifetime decreased reaching an almost flat region after 150 hours, to

approximately 500µs. The reason for the almost instant increase in the sample lifetime when subjected to room temperature is unknown.

Figure 43 – Lifetime stability in 200 hours measurements in samples from SBS, #1, #5 and #3. In the first 24 hours, samples are under illuminated annealing at 150°C, 80mw/m². After 24 hours, the samples were subjected to the same illumination of 80mW.cm-², but at room temperature

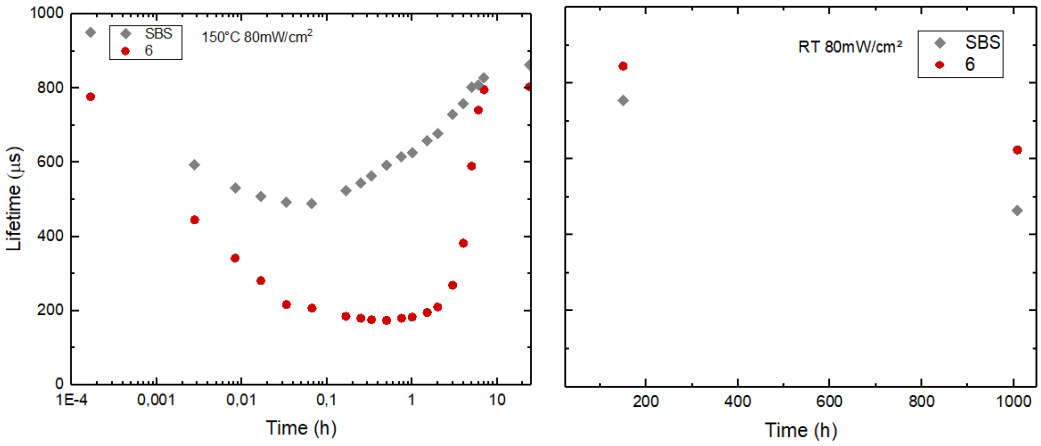


Source: Author

4.2.1.2.2 Lifetime stability up to 1000 hours

The stability in even longer time measurements of 1000 hours were tested in samples from SBS and #6. The results are shown in Figure 44. Again, after 24 hours, the samples were subjected to the same illumination of 80mW.cm^{-2} at room temperature. The first measurements at room temperature was taken in 150-hour mark. Unexpectedly, the #6 lifetime increased to a higher lifetime then the initial. This can be related to the fact that samples from profile #6 (and #5) showed lower initial lifetimes in comparison to other profiles. One of the possible causes is the excess of hydrogen in the bulk material [126], so, after 150 hours, in those conditions, a effusion of hydrogen from the bulk possibly resulted in this lifetime increase at this moment, but this is difficult to assert. After 1000 hours, the lifetime decreased for both samples, but SBS showed a considerably higher degradation to approximately 50% of initial lifetime, while #6 degraded to 80% of its initial lifetime. The reported visible belt marks seen in SBS samples already indicated that its surface could be weakened. These degradation over time, which according to Sperber et al [148], [164], is related to the degradation of the hydrogen rich passivation layer of the wafer surface, suggest that the SBS firing profile caused a significant degradation in the surface layer of the wafer.

Figure 44 – Lifetime stability in 1000 hours measurements in samples from SBS and #6. In the first 24 hours, samples are under illuminated annealing at 150°C, 80mw/m². After 24 hours, the samples were subjected to the same illumination of 80mW.cm-², but at room temperature



Source: Author

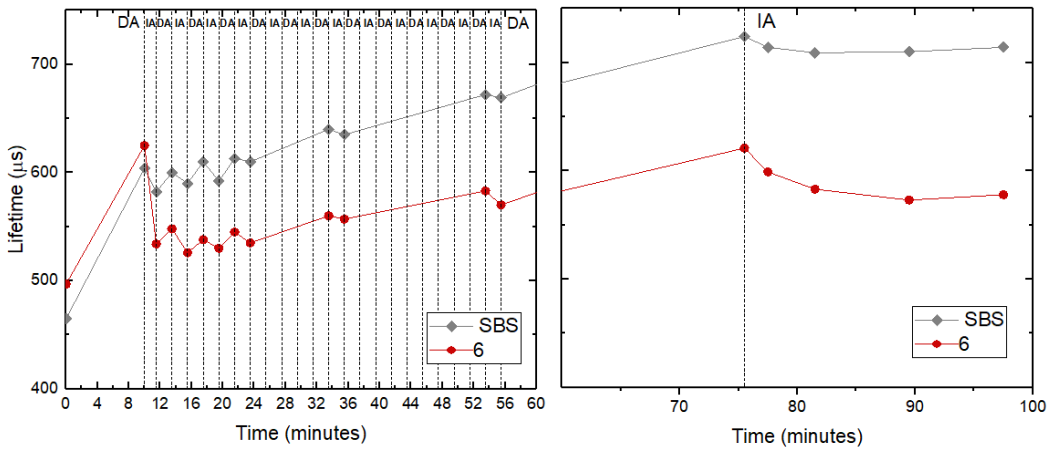
4.2.1.2.2 Dark annealing-Illuminated annealing cycles tests for LeTID detection and suppression

For a last test, these samples that went through 24 hours at illuminated annealing and 1000 hours at RT and illumination, where subjected to dark annealing (DA) illuminated annealing (IA) cycles. The test was performed for two main purposes: to see the possibility of recover the lifetime of these samples; and the possibility of differentiate the samples in relation to the LeTID defects that each one has shown. Figure 45 shows the evolution of the measured lifetimes after dark annealing or illuminated annealing, which are signed with the vertical dash lines. At first, a 10 minutes 150°C DA raise the lifetimes of samples from both SBS and #6, to approximately 600µs and 620µs, respectively. After a one and a half minute IA at 150°C and 3.5 suns, SBS sample lifetime showed a little decrease, while #6 sample showed a considerably higher decrease down to approximately 530µs. Thereafter, 2-minute sequential DA-IA cycles are performed, resulting in small increases in lifetime after DA and decreases after IA, but with a tendency of increasing the lifetime after each cycle. After the 1-hour mark, a 20 minutes DA was performed, and a degradation and recovery curve of lifetime, at IA, was then plotted, exhibiting a small degradation for the two samples and a rapid start in the recovery.

A considerably higher decrease in lifetime in sample from #5, in the first IA condition, from 620µs down to approximately 530µs, compared with SBS, and the

sequential higher decrease in lifetime after IA than an increase after DA, in the following two cycles is visible. This suggest that the LeTID defect is in a much higher quantity in sample from #5 than in sample from SBS. This is because the higher degradation is due to the longer time that the LeTID recovery takes to start, as discussed before. The following DA-IA cycles did not much to the #5 sample unless a step-by-step increase in the lifetime. Possibly, at that point, the quantity of LeTID defect were not enough to cause greater degradation at IA than the recovery seen in DA. Thus, suggesting that these DA-IA cycles possibly reduce the amount of LeTID defects in the material. The lifetime degradation and recovery curve in IA after the 76-minute mark shows that under this condition there is a small maximum degradation and a recovery in the lifetime starting after about 5 to 10 minutes. Thus, we propose for future investigations with these DA-IA cycles aiming the possible findings: rapid detection of the LeTID defect in the material, comparing it with a material without LeTID; feasible treatment for rapid suppression of LeTID defects to acceptable levels. In this test from Figure 45, we used samples that was degraded, recovered and degraded again in a 1000-hour stability test, showing that it is possible to recover wafer lifetime under these conditions at levels up to about 80% of its initial.

Figure 45 – Lifetime evolution after dark annealing (DA - 150°C) and illuminated annealing (IA – 150°C, 3.5 suns). SBS and #5 samples previously went through 24 hours at illuminated annealing and 1000 hours at RT and illumination.



Source: Author

4.2.1.3 A method proposed for LeTID and BO-LID separation

In view of the results, we consider that degradation curve from firing process #1 to be representative for BO-LID. Assuming that is possible to find the contribution of

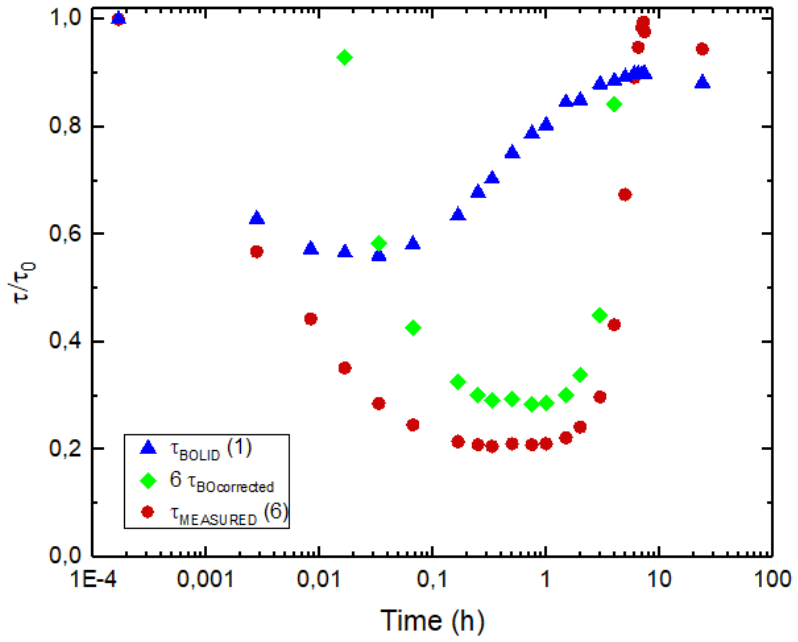
the other degradations, including LeTID defects, for other firing profiles. An equation to correct the total degradation for the BO contribution is proposed as in equation (21),

$$\frac{1}{\tau_{BO-corrected}(t)} = \frac{1}{\tau_{measured}(t)} - \frac{1}{\tau_{BO-LID(t)}} \quad (21)$$

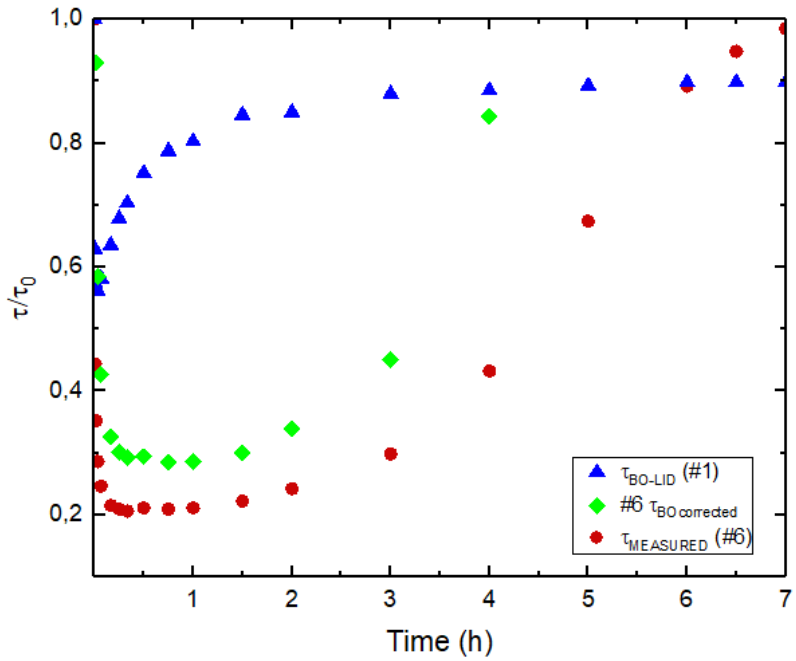
where τ_{BO-LID} is the lifetime value in time for the BO-LID degradation, which is considered the values from degradation curve of the firing process #1 in this case; $\tau_{measured}$ is the measured lifetime values in time under same illuminated annealing condition; and $\tau_{BO-corrected}$ is the calculated remaining degradation. Since the same surface degradation is expected in ASC and fired samples, we argue that the $\tau_{BO-corrected}$ would represent a good approximation for the effect of LeTID.

When the lifetime evolution in sample from process #1 were considered representative for the BO-LID (τ_{BO-LID}), the total degradation in sample from #6 is separated into the BO-contribution and the BO-corrected contribution according to Eq. (21) in Figure 46.

Figure 46 – (a) Normalized curves for τ_{BOLID} considered as normalized #1 curve values (BOLID representative); $\tau_{measured}$ as #6 normalized curve values; and corresponding calculated #6 $\tau_{BOcorrected}$ (considered LeTID representative) at 150°C, 80mw/m² illuminated annealing; (b) same as (a) but linear timescale.



(a)

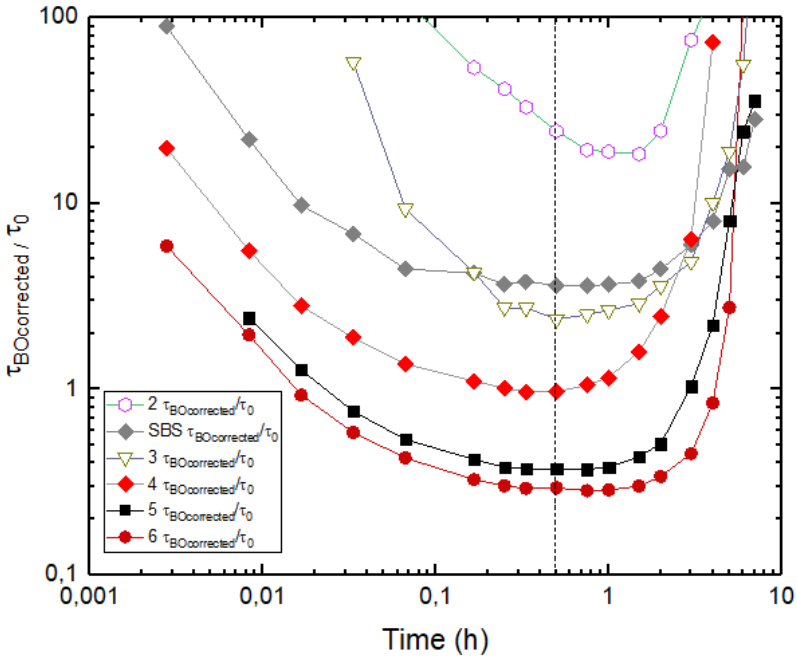


(b)

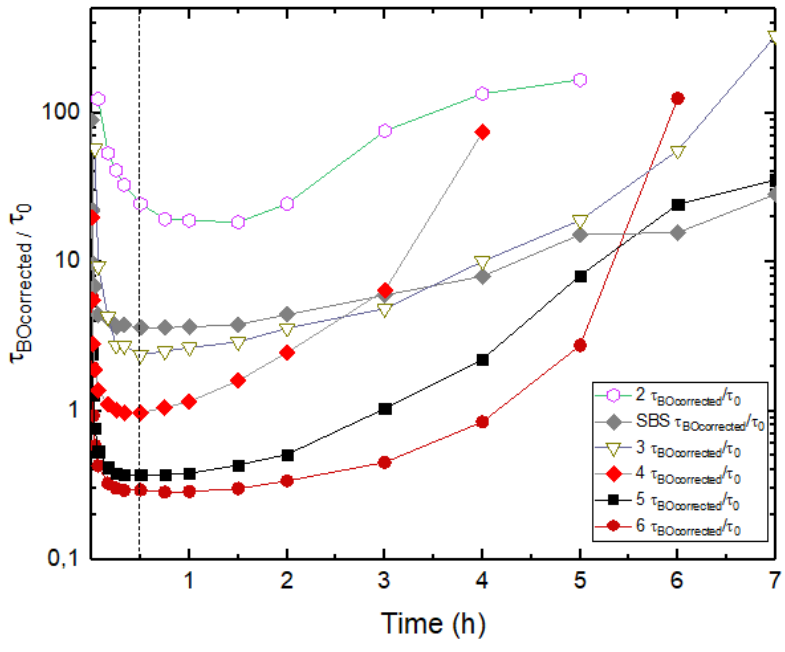
Source: Author

Figure 47 shows the BO-corrected lifetime contribution for all the samples. The BO-corrected lifetime term used as a measure of the LeTID degradation shows the approximate magnitude of the lifetime limiting LeTID defect. Figure 47(b) shows that for sample from process #2 the BO-corrected lifetime contribution is always higher that 20, meaning that the LeTID recombination path is responsible for less than 5% of the total degradation. Similarly, the LeTID becomes the most recombination active defect when the normalized $\tau_{BO-corrected}$ is below 2. For samples from process #5 and #6 the $\tau_{BO-corrected}$ lifetime is as low as 0.3 indicating that the LeTID defect is the most recombination active defect by far. The contributions from BO-LID is, however, not negligible, as minimal $\tau_{measured}$ is down to approximately 0.2. A maximum $\tau_{BO-corrected}$ degradation is visible at 30-60 minutes for all groups. Thus, the onset times of the recovery mechanisms are between 30-60 minutes for LeTID, while it is 2 minutes for BO-related LID in same illuminated annealing conditions. The partial activation of LeTID defects with lowering the firing peak temperature is elegantly demonstrated, and fits with previous studies [151]. The presence of some LeTID recombination also in SBS, as expected from the recovery profile in Figure 47b is confirmed. This enhance the previous study result [152], showing that slower heating or cooling ramp or the longer time above a critical temperature may not completely suppress LeTID.

Figure 47 – (a) Normalized curves for calculated $\tau_{BOcorrected}$ for the groups #2, #3, #4, #5, #6 and SBS at 150°C, 80mw/m² illuminated annealing; maximum $\tau_{BOcorrected}$ degradation occurred at around 30 minutes for all presented groups; #5 and #6 minimum $\tau_{BOcorrected}$ were 0,4 and 0,3; #4 minimum $\tau_{BOcorrected}$ were 1; #2 and SBS minimum $\tau_{BOcorrected}$ were 2 and 4; (b) same as (a) but linear timescale.



(a)



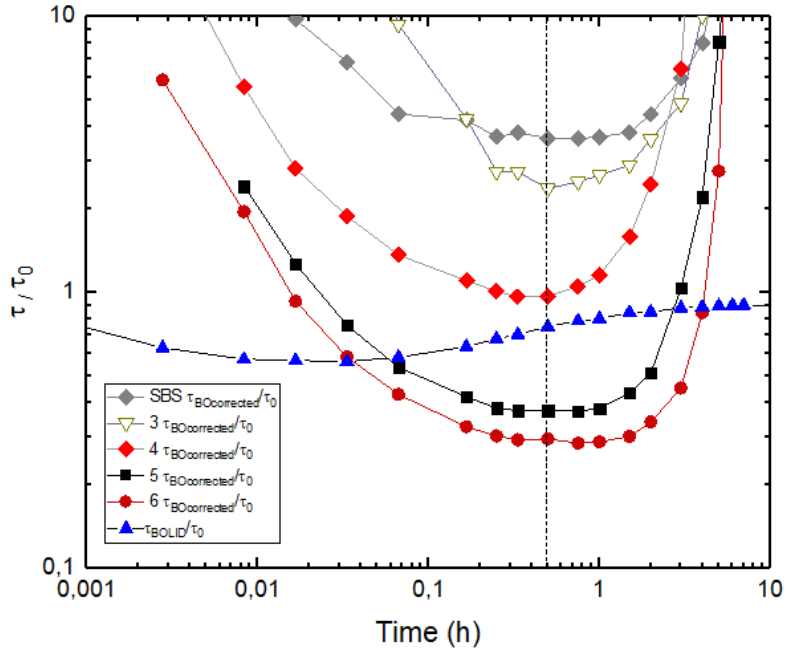
(b)

Source: Author

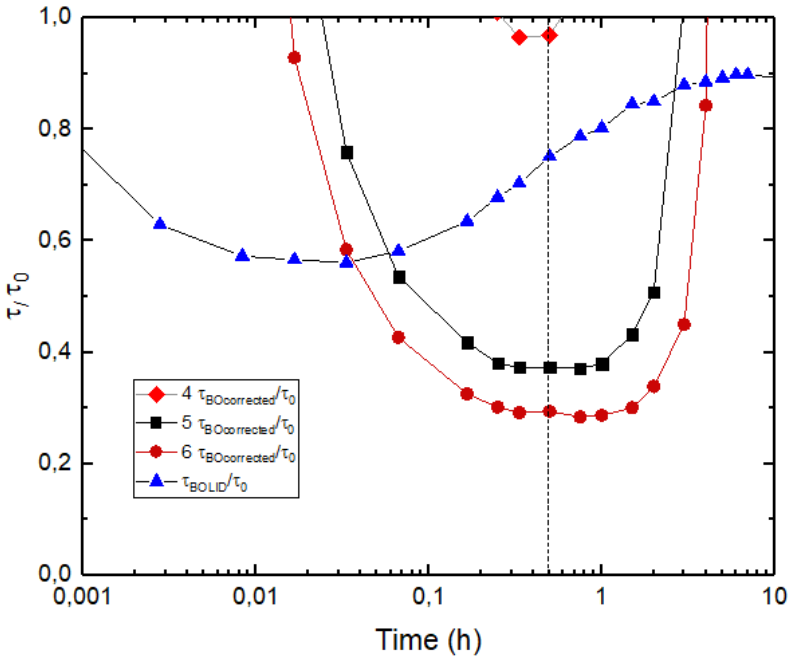
In Figure 48, the normalized BO-related degradation is plotted with previous data from Figure 47. With is, is possible to compare the detrimental effect that the BO-related LID and the LeTID (represented by the BOcorrected). In Figure 48(b), the vertical

axis ranges from 0 to 1, which shows three of the profiles with higher detrimental effects on samples, #4, #5 and #6.

Figure 48 – (a) Normalized curves for calculated $\tau_{BOcorrected}$ for the groups #2, #3, #4, #5, #6 and SBS at 150°C, 80mw/m² illuminated annealing compared with normalized τ_{BOLID}; (b) same as (a) but with a normalized scale from 0 to 1.



(a)



(b)

Source: Author

4.2.1.4 The Firing Profile curves investigation on LeTID formation/suppression mechanisms

The impacts of the different firing profile curves from the different firing furnace conditions on the illuminated annealing were demonstrated in previous items in this chapter. The LeTID formation/suppression mechanism is, although, more complex to detect and understand. Because the real nature of the LeTID defect itself is not settled, its formation and suppression mechanisms are open to discussion.

We propose different possible mechanisms to LeTID formation/suppression, which are different from the hydrogen infusion/effusion form the bulk proposed by A. Cielsa, S. Wellam et al. [126]. We consider that LeTID defects precursors are formed inside the firing furnace, and can be suppressed by emptying a so-called defect reservoir.

In Table 9, data from firing profiles and calculated maximum BO-corrected degradation (LeTID representative) is given. The different peak temperature from different firing profiles was considered in literature [149], [152] and in previous discussion as the main parameter for LeTID defect partial or full formation. The SBS firing peak of 818°C, however, contradicts this trend associated with this parameter alone. Further increase on firing peak temperature, up to 815°C, with the same fast heating and cooling ramps, resulted in a observed higher LeTID on reference [149]. Therefore, different heating and cooling ramps need to be taken into account. On R. Eberle et al. [152] analyses, heating/cooling rates higher than 80°C.s^{-1} (referred to as FFO profile) resulted in a high LeTID, while in the firing process with limited heating/cooling rates minor than 50°/c.s^{-1} (referred to as RTP profiles) the LeTID was not observed, even in high peak temperatures, up to 850°C.

The heating ramp from firing profile #5 is 61°C.s^{-1} and the cooling ramp is 49°C.s^{-1}. Both ramps are comparable with Eberle´s RTP profiles [152], however, slightly fasters. In profile #6, the heating ramp is considerably higher, 86°C.s^{-1}, and the cooling ramp is 65°C.s^{-1}, which is comparable with Eberle´s FFO profile. However, in our results, a high LeTID is observed in profiles #5 and #6, where $\boldsymbol{\sigma_{\mathbf{DEG\ (BO-corrected)}}/\sigma_0}$ is 0.371 for #5 and 0.284 for #6. Is possible that only profiles with higher peak temperatures (> 700°C) with considerably slower heating/cooling ramps than profile #5 ramps could result in less LeTID. This is observable in the resulting LeTID from the SBS sample, where $\boldsymbol{\sigma_{\mathbf{DEG\ (BO-corrected)}}}$ is 3.61, which is a minor contribution to the sample overall lifetime degradation. The SBS cooling rate of 51°C.s^{-1}, from 818°C peak temperature

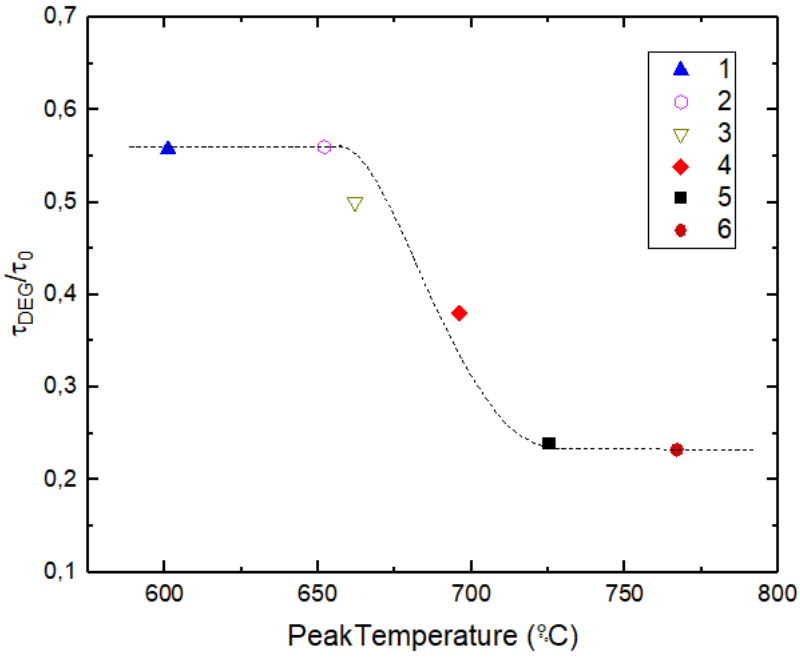
down to 400°C, which is comparable to the other profiles. However, the SBS heating ramp is considerably slower, of 36 °C.s^{-1}. Thus, the heating ramp combined with thermal budget are the characteristics of the firing profile that most likely impact on the resulting observed LeTID.

Table 9 – Data from each firing profile and calculated maximum normalized BO-corrected degradation (LeTID representative)

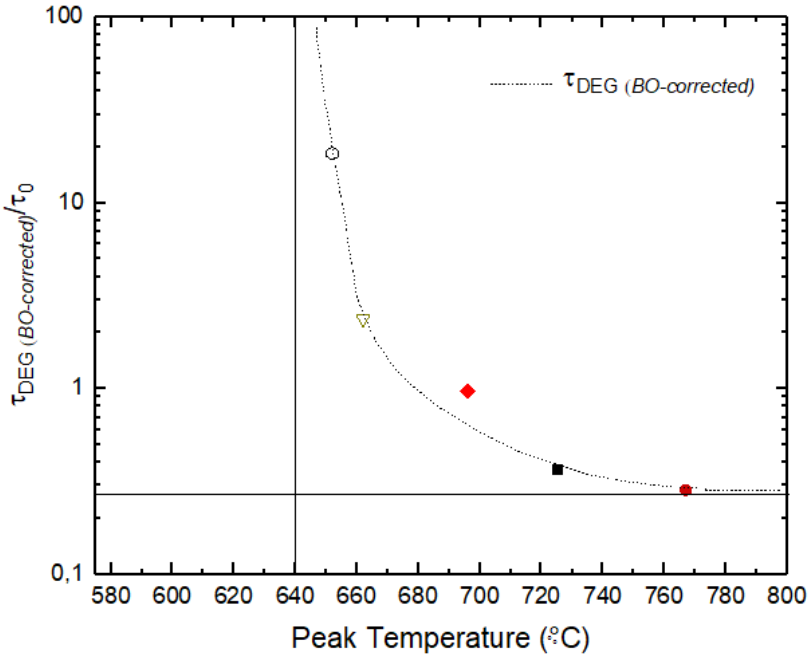
Firing Profiles	**#1**	**#2**	**#3**	**#4**	**#5**	**#6**	**SBS**
Peak Temperature (°C)	600,8	652,4	662,6	696,1	725,1	766,9	818,6
time >600°C	0,37	2,96	2,99	3,32	4,41	4,06	12,18
time >700°C					1,37	2,18	8,02
time >800°C							2,2
Heating ramp (°C/s) *400°C-Tmax*	65	56	60	65	61	86	36
Cooling ramp (°C/s) *Tmax-400°C*	48	60	62	64	49	65	51
Cooling ramp (°C/s) *Tmax-200°C*	36	44	43	45	43	35	29
Thermal Budget >600°C (°C.s)	0,31	98,1	118,6	189,1	309,8	796,3	1557
Thermal Budget >500°C (°C.s)	279	453	544	645	930	918	2930
Normalized maximum BOcorrected lifetime degradation $\boldsymbol{\sigma_{DEG\ (BO-corrected)}/\sigma_0}$ (µs)		18,4	2,37	0,965	0,371	0,284	3,61

The observed degradation and recovery at illuminated annealing in samples from #1 to #6 firing profiles can be related to the peak firing temperature. Figure 49(a) compares normalized maximum degradation found for each group of samples related with peak firing temperatures. An increase is observed in the concentration or recombination activity until a temperature of 725°C is reached. Figure 49(b) relates the peak temperature of the firing profiles and each corresponding normalized maximum $\tau_{BO-corrected}$ degradation. One vertical and one horizontal line illustrates the temperature and the $\tau_{BO-corrected}$ limits, respectively. The exposure of the sample to a higher peak temperature, of 766°C, further form the LeTID defect. The tendency, however, indicates a saturation of the degradation. We considered then, for the samples in this study, that formation of LeTID defects initiates after 640°C and that maximum normalized $\tau_{BO-corrected}$ degradation decreases with further higher peak firing temperatures, with similar heating/cooling ramps, down to approximately 0,26.

Figure 49 – (a) Normalized maximum degradation $\tau_{DEG(measured)}$ under illuminated annealing for each group of samples related with peak temperature in firing process b) Normalized maximum degradation $\tau_{DEG\ (BO-CORRECTED)}$ for each group of samples under illuminated annealing related with peak temperature in firing process.



(a)



(b)

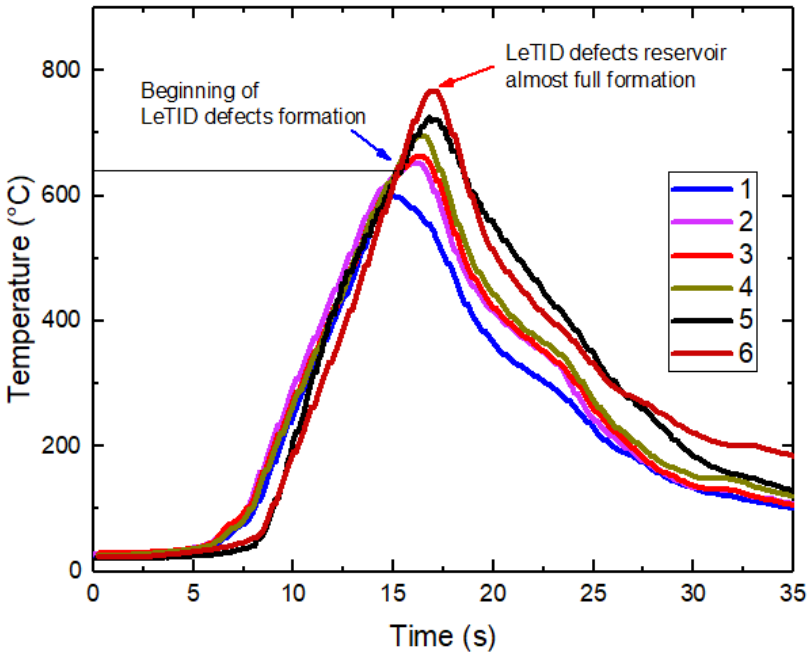
Source: Author

The normalized maximum BOcorrected lifetime degradation calculated in samples from firing profiles #2 and #3 are equals to 18.4 and 2.37, respectively (Table 9). The differences seen between the maximum BOcorrected degradations indicates that LeTID formation starts to be observed after passing through a 640°C “barrier”, illustrated

in Figure 49(b). C. Chan et al. [144] states that the LeTID is triggered if peak temperatures exceed approximately 700°C. This is because they found a considerably higher degradation in the sample fired at 700°C then in the sample fired at 675°C. Our results were very similar with respect to the peak temperatures and the observed degradation, and are in accordance with C. Chan et al. While agreeing, we further consider that the LeTID defect is actually triggered at 640°C. Then, a defect reservoir is increasingly formed, being slightly relevant in a peak temperature of 660°C; almost totally formed at 725°C; and fully formed soon after 765°C. This "step function" triggering mechanism can be visualized in Figure 49(a). However, Figure 49(b) shows the actual presence and relevance of the LeTID with increased peak temperature.

In the view of the discussion, in Figure 50 that shows the firing profiles from #1 to #6, the beginning of LeTID defects formation is signed with the blue arrow. The triggering temperature of 640°C is considered. The temperature firing profile curves can be compared in relation with partial formation of LeTID. Higher peak temperatures increases the formation of LeTID defects reservoir, which is full (or almost full) in firing profile #6 and is indicated by the red arrow.

Figure 50 – Firing profiles from #1 to #6. Beginning of LeTID defects formation is signed with the blue arrow. The triggering temperature of 640°C is considered.



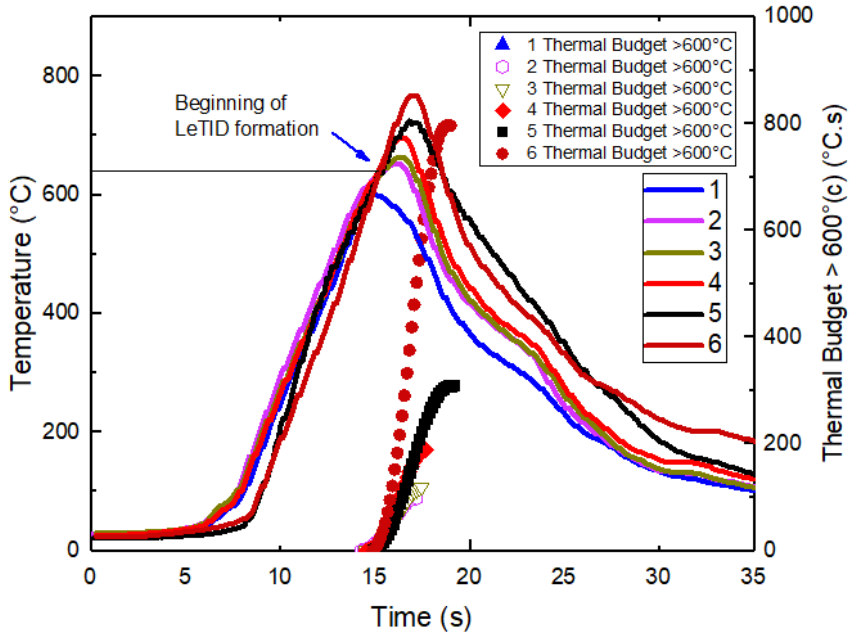
Source: Author

The above-mentioned LeTID formation mechanism is considered for the firing profiles from #1 to #6, which has comparable heating and cooling rates, with a

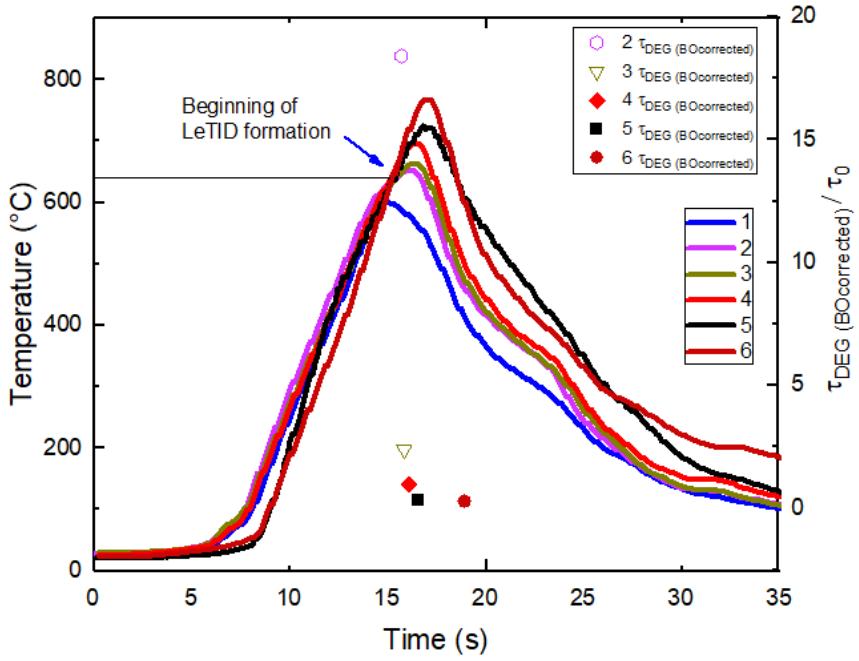
slightly faster heating and cooling ramps for the profile #6. Another possibility for LeTID formation mechanism is the dependence on the increase of the thermal budget above a specific temperature, which promotes an increasingly formation of the LeTID defects reservoir. If this is the case, there could be a variation at the LeTID defect trigger temperature depending on the time of exposure of the sample above the specific temperature and the magnitude of the temperature.

Figure 51 correlates the firing profiles with accumulated thermal budgets above 600°C (a) and with the respective observed Normalized maximum BOcorrected lifetime degradation (b). For this, for each profile, the cumulative thermal budget was calculated point by point, for temperatures above 600°C and plotted on the graph. Thus, a model of how degradation increases inside the firing furnace is illustrated, and then we can propose this LeTID formation mechanism for such profiles with fast heating and cooling ramps.

Figure 51 – (a) Firing profiles from #1 to #6**.** Beginning of LeTID defects formation is signed with the blue arrow. The triggering temperature of 640°C is considered.



(a)

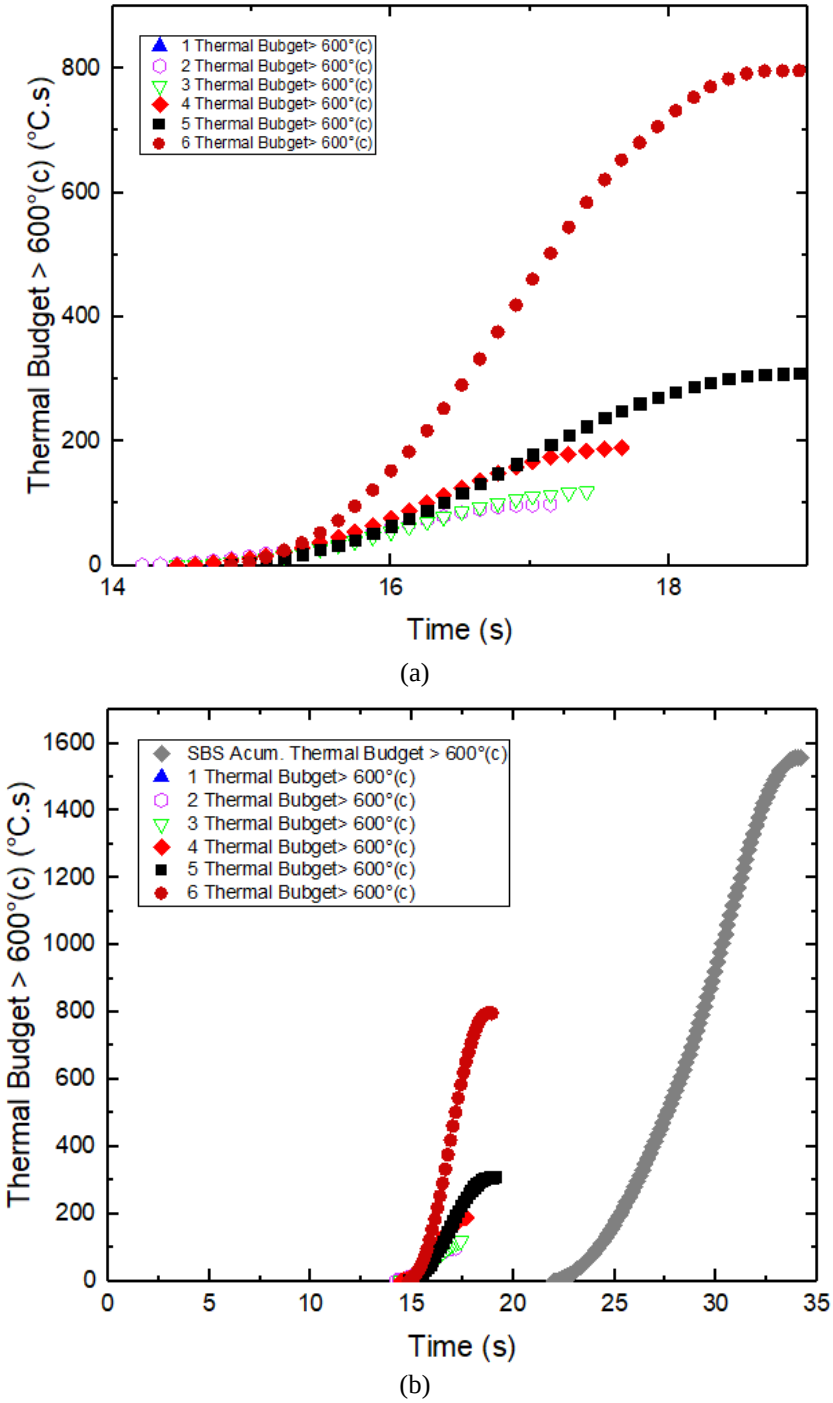


(b)

Source: Author

The thermal budget for temperatures above 600°C for firing profiles from 1# to #6 are better visualized in Figure 52(a). The thermal budget from profile #6 is much higher. The firing profile #5 has the same duration above 600°C as the profile #6, approximately 4s, but a considerably lower thermal budget, close to 300°C.s. The thermal budget curve from profile #3 is slightly minor than from profile #2, showing that, in this range of values, the formation of LeTID is highly sensitive to temperature conditions, since samples from profile #3 showed a considerably higher LeTID (as seen in Figure 47). In Figure 52(b), the SBS firing profile thermal budget for temperatures above 600°C is compared with the previous ones. Because the belt speed is slower for SBS, the thermal budget above 600°C starts to count well after, last for approximately 12s, and is twice as higher as the profile #6 thermal budget.

Figure 52 – (a) Thermal budget for temperatures above 600°C for firing profiles from 1# to #6, the time scale is the time when temperature is higher than 600°C; (b) same as (a), including SBS profile.

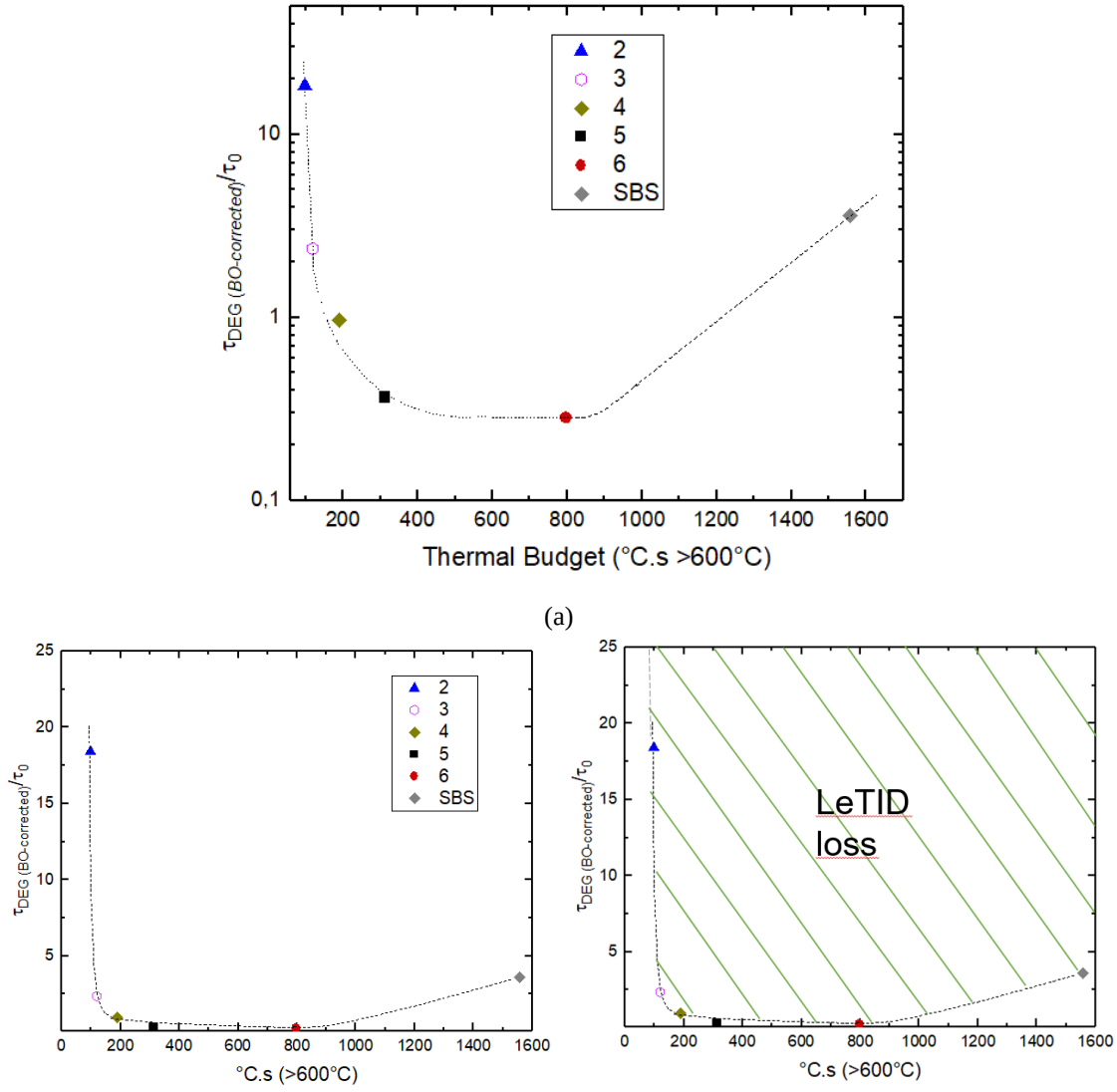


Source: Author

Considering the influence that the thermal budget can have in the formation of the LeTID defects, the maximum normalized BO-corrected lifetime degradation is related with the thermal budget above 600°C for each firing profile, illustrated in Figure 53(a) at logarithmic scale and (b) at linear scale. The dash line suggests a path of formation and suppression of LeTID defects with increasing thermal budget. First, the

increase on the thermal budget resulted in a severe degradation, from 18 to 0.28. Between 800°C.s^{-1} and 1550°C.s^{-1} there is recovery of the degradation, up to 3.6.

Figure 53 – (a) Normalized maximum degradation $\tau_{DEG\ (BO-CORRECTED)}$ for each group of samples under illuminated annealing related with the calculated thermal budget in firing processes above 500°C; (b) Same as (a) but for thermal budget above 600°C; (c) same as (b) but linear scales; (d) same as (c) with a hatched area indicating the loss that the LeTID defect introduces in the material in a firing process with increased thermal budget



Source: Author

As discussed before, the maximum normalized BO-corrected lifetime degradation is considered detrimental on the effective lifetime when values are less than 10 and detrimental in a much higher proportion when values are less than 1. In SBS, the maximum normalized BOcorrected lifetime degradation value found was 3.61. This corresponds to half of the detrimental effect caused by the BO-related degradation in the

same sample. Therefore, we understand that lifetime degradations at these much lower levels of detrimental effect are difficult to detect, especially when measuring V_{oc} degradation in photovoltaic cells.

Perhaps because of this detection difficulty, the LeTID defect was considered by Eberle et al. [152] to be suppressed in cases of high temperature profiles with slower heating and/or cooling ramps. What it is possible to see with the Figure 53, is that the LeTID defect is triggered and starts with very low detrimental effects, with degraded BOcorrected lifetime above 18 when the thermal budget is close to 100°C.s^{-1}. However, it is possible to visualize almost a perpendicular line between the first two degradations from profile #2 and #3. At thermal budget between 100°C.s and 300°C.s, a big drop in the degradation values is seen, down to 0.37, which continue to decrease at a slower rate down to 0.28 at approximately 850°C.s, where there is an apparent saturation. The recovery from the degradation is seen in the thermal budget of 1550°C.s to the value of 3.6. However, this value is not close to the degradation seen at profile #2, which is 18. Thus, the recovery from profile #6 to SBS needs much more thermal budget than the rapid degradation seen from profile #2 to #5. With this, it is possible to expect that it is extremely difficult to completely remove the LeTID defects in samples that did pass, in this case, by a thermal budget above 600°C higher than 100°C.s. Figure 53(c) illustrates the “LeTID” loss caused by the thermal budget. The suppression of the LeTID defects seen in the SBS sample is a partial suppression. However, the remaining LeTID defects showed a very low detrimental effect in effective lifetime (as was shown in Figure 47).

Most part of early discussion in this study is based on the assumption that there is possibly a path of the LeTID defects formation and suppression inside the firing furnace. By assuming that, we are considering a slightly different model for the defect activation from what is usually discussed in some literature [165], [126], [157]. In these recent papers, the LeTID activation and deactivation is considered more related with the hydrogen in-diffusion for the formation of defect reservoirs and hydrogen effusion to drain the reservoir. What we consider in a new proposed model is that at temperatures above 600°C, above a trigger temperature, there is enough energy for the in-diffused hydrogen into the bulk to bond and form the defect (or defects), forming the defect reservoir and later causing LeTID. The suppression is taken by a promptly "disrupted" of the defects in the presence of charge carriers, i.e. temperature and/or light. In other words, we assume that the defects are activated by light and temperature and the charge carriers

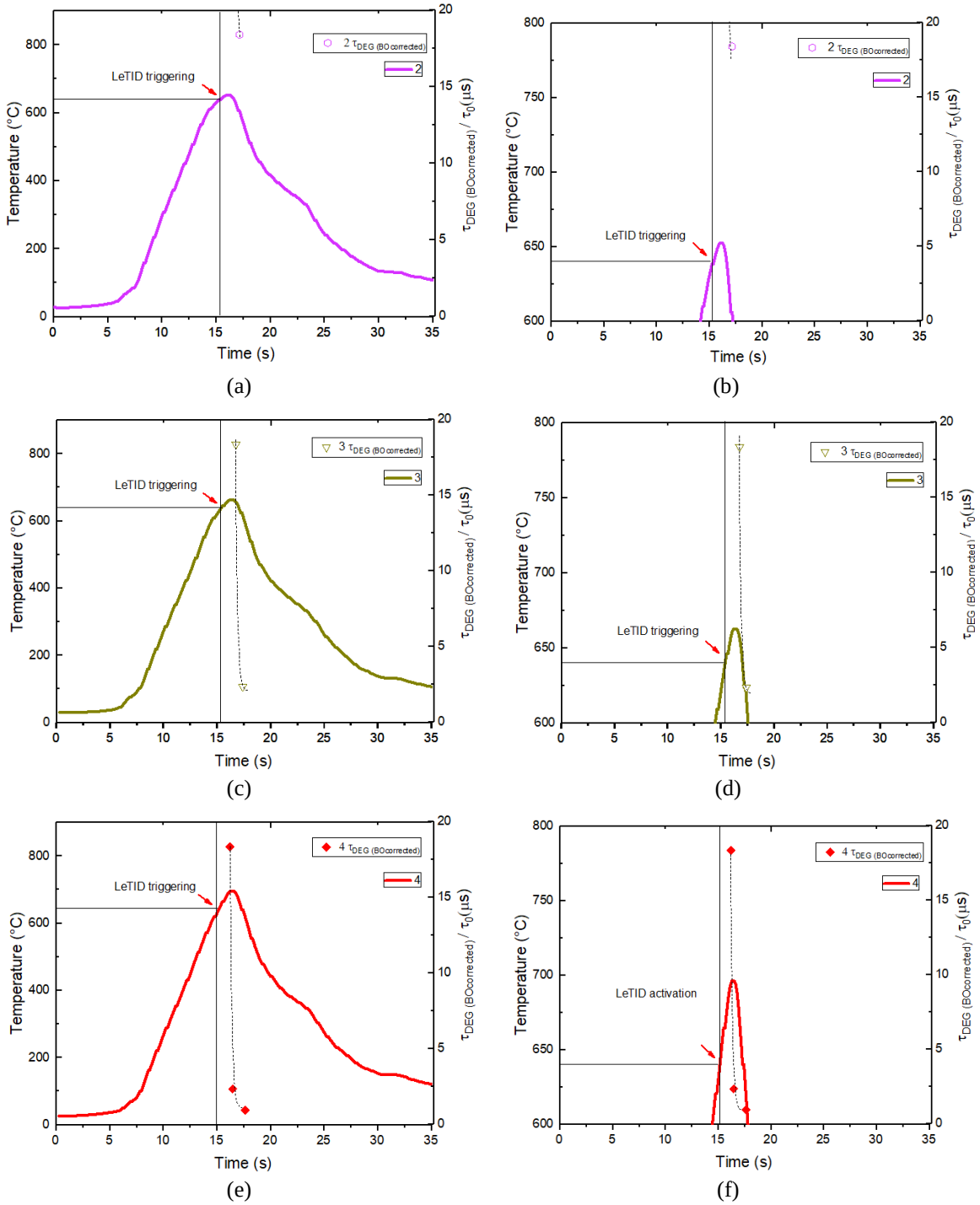
give up their energy to disrupt the defects. That is why LeTID, after each dark-annealing/illuminated annealing cycle, has less and less recombination activity [157].

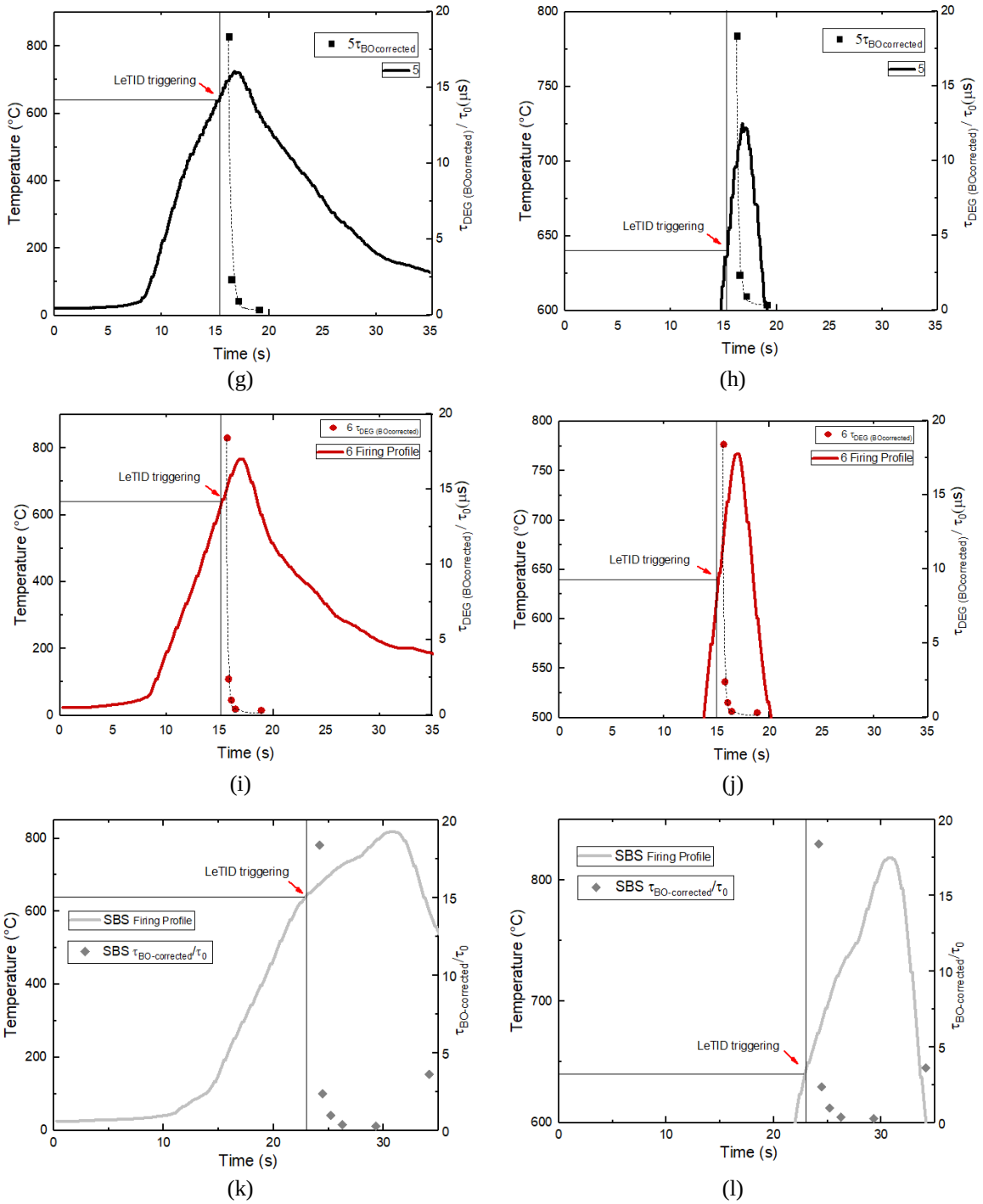
4.2.1.4.1 Models for formation of the LeTID defects

To further investigate the possibility of a path of the LeTID defect inside firing furnace and to analyze its triggering temperature, in Figure 54 the firing profiles from #2 to #6 were related with the maximum normalized BO-corrected lifetime degradation. For this, it was considered that the thermal budget above 600°C is responsible for the increased formation of the defect and that the triggering temperature of the LeTID is fixed at 640°C (from Figure 49 (b)). For each point of the profile curves, the thermal budget was calculated and the maximum normalized BO-corrected lifetime degradation of each firing profile was plotted when thermal budget reached the same value (Table 9). Therefore, it was considered an increasing degradation of the BOcorrected lifetime in a same firing profile, inside the firing furnace and according to the increased thermal budget. A horizontal line and a vertical line indicates the temperature of 640°C and the related time, respectively.

In lower temperatures profiles #2, #3 and #4, as seen in Figure 54 (a, b, c, d, e, and f), the triggering temperature and the maximum normalized BO-corrected lifetime degradation from this proposed model are visualized. It is possible to observe how sensitive is the formation of LeTID, with small increases in temperature from one profile to the other. The vertical line, which marks the time when 640°C is reached, shows that the points of maximum normalized BO-corrected lifetime degradation are seemingly compatible with the triggering temperature. It is possible to observe that, with the increase of temperatures profiles, the maximum normalized BO-corrected lifetime degradation points are closer to the vertical line. This is because the increase of the thermal budget is faster, so the formation of the defects. This resulted model, to which we refer to as model A, is therefore based on two assumptions: the trigger temperature is fixed at 640°C and that; when the thermal budget above 600°C reaches the corresponding Table 9 maximum normalized BO-corrected lifetime degradation values, the plotted values in time can express the formation of LeTID defects within the profile. This model can be reasonable at least in profiles with similar rapid heating and cooling ramps.

Figure 54 - Firing profiles from #2 to #6 related with the maximum normalized BO-corrected lifetime degradation, plotted in time. In this proposed Model A is considered that the thermal budget above 600°C is responsible for the increased formation of the defect and that the triggering temperature of the LeTID is fixed at 640°C.





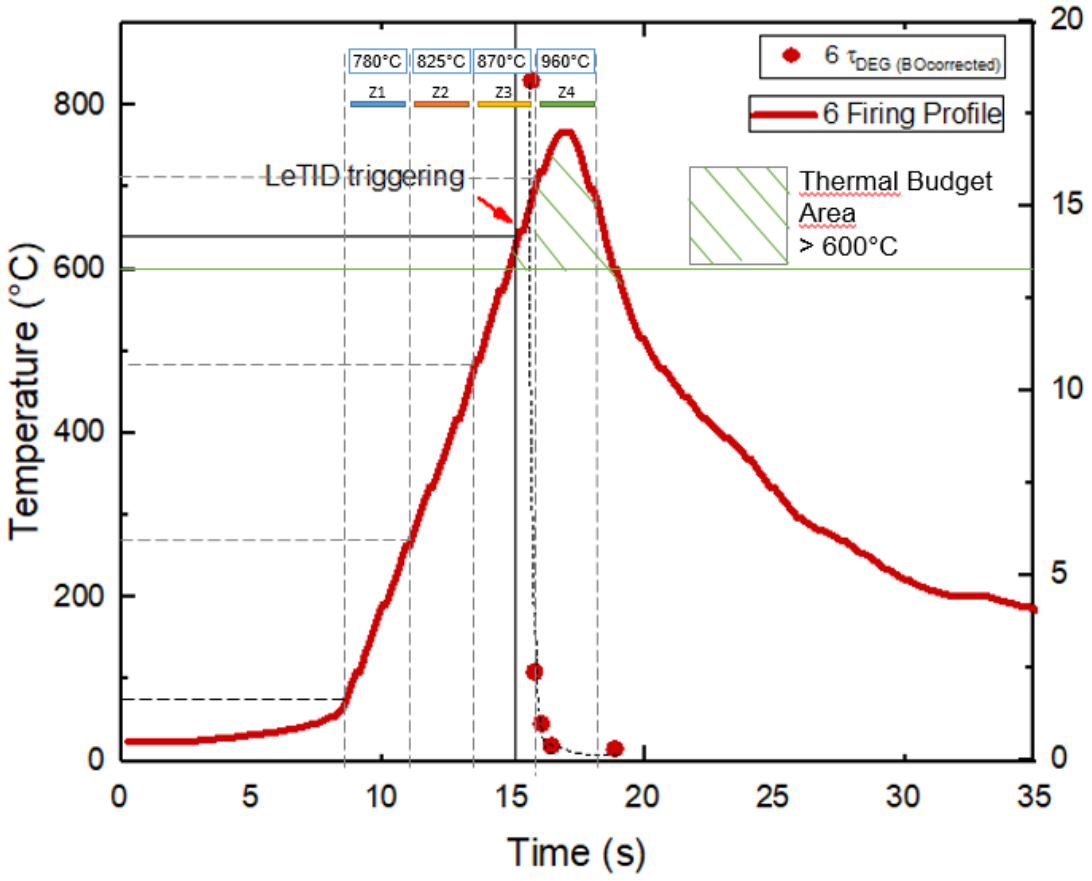
Source: Author

It is important to notice, again, that the maximum normalized BO-corrected lifetime degradation calculated values for each group of samples are from the lifetime data measured at illuminated annealing (Figure 47), subtracting the effect of the degradation related to the BO-LID, considering, therefore, to represent well the LeTID alone. When maximum normalized BO-corrected lifetime degradation is related with the point-to-point thermal budget in the firing profiles, stipulating a degradation of the BO-

corrected lifetime inside the furnace, actually, these degradations represents the detrimental effect that the formation of LeTID defects reservoir would cause. It is therefore considered that there is a full (or almost full) defect reservoir in profiles #5 and #6, a partially full between #2 and #4 and an empty reservoir in # 1. However, there must be a much larger defect reservoir in profiles #5 and #6, or even a big difference between these two, than perhaps this maximum normalized BO-corrected lifetime degradation value may represent. In any case, it represents at that moment inside the furnace, how much that amount of defect in the reservoir would result in terms of lifetime degradation caused by LeTID.

To sum up the proposed model A, which pretends to express the behavior of the LeTID formation path inside the firing furnace, the firing profile #6 related with the maximum normalized BO-corrected lifetime degradation is shown in Figure 55. The LeTID triggering point is at fixed 640°C, the thermal budget above 600°C is signed with the hatched area, and the firing zones as Z1, Z2, Z3 and Z4 are indicated with different colors and different set temperatures. The firing zones were plotted as an indicative of temperatures of these zones, but the position in time is not plenty regarded.

Figure 55 –Model A for the formation of the LeTID inside the firing furnace. Firing profile #6 is related with the maximum normalized BO-corrected lifetime degradation. The LeTID triggering point is at fixed 640°C, the thermal budget above 600°C is signed with the hatched area and the firing zones as Z1, Z2, Z3 and Z4 are indicated with different colors and different set temperatures.



Source: Author

Considering the model A, the cooling ramp does not play a role in the LeTID defect formation within the firing furnace, as discussed before. In model A, the formation of the LeTID defects start at the trigger temperature, from then on, the defects are increasingly formed with the increase of the thermal budget above 600°C. Therefore, the main cooling ramp role would be to "turn off" the thermal budget, which would be responsible for either increasing the defect reservoir formation (profiles #2 to #6) or for avoiding defect reservoir emptying seen in SBS profile. What endorses this assertion is that the SBS cooling ramp, from peak temperature to 400°C, is similar to the other firing profiles (Table 9).

A second possibility to formation of LeTID defects is that a higher or lower thermal budget around the LeTID triggering point influences the actual LeTID triggering temperature (model B).

Although we understand that model A fairly expresses the path of the LeTID defect inside the firing furnace and can be applied to firing profiles with fast

heating/cooling ramps, this model A could not be applicable to the SBS profile in which the belt speed is half the speed of the other profiles. Therefore, a separate investigation, proposing another model, was performed by establishing that a thermal budget of 50°C.s and thus a variable temperature gives the LeTID triggering point. Assuming this, the thermal budgets above 600°C were calculated point-to-point in the firing profiles, and when that value reached 50°C.s, the corresponding temperature was plotted in Table 10.

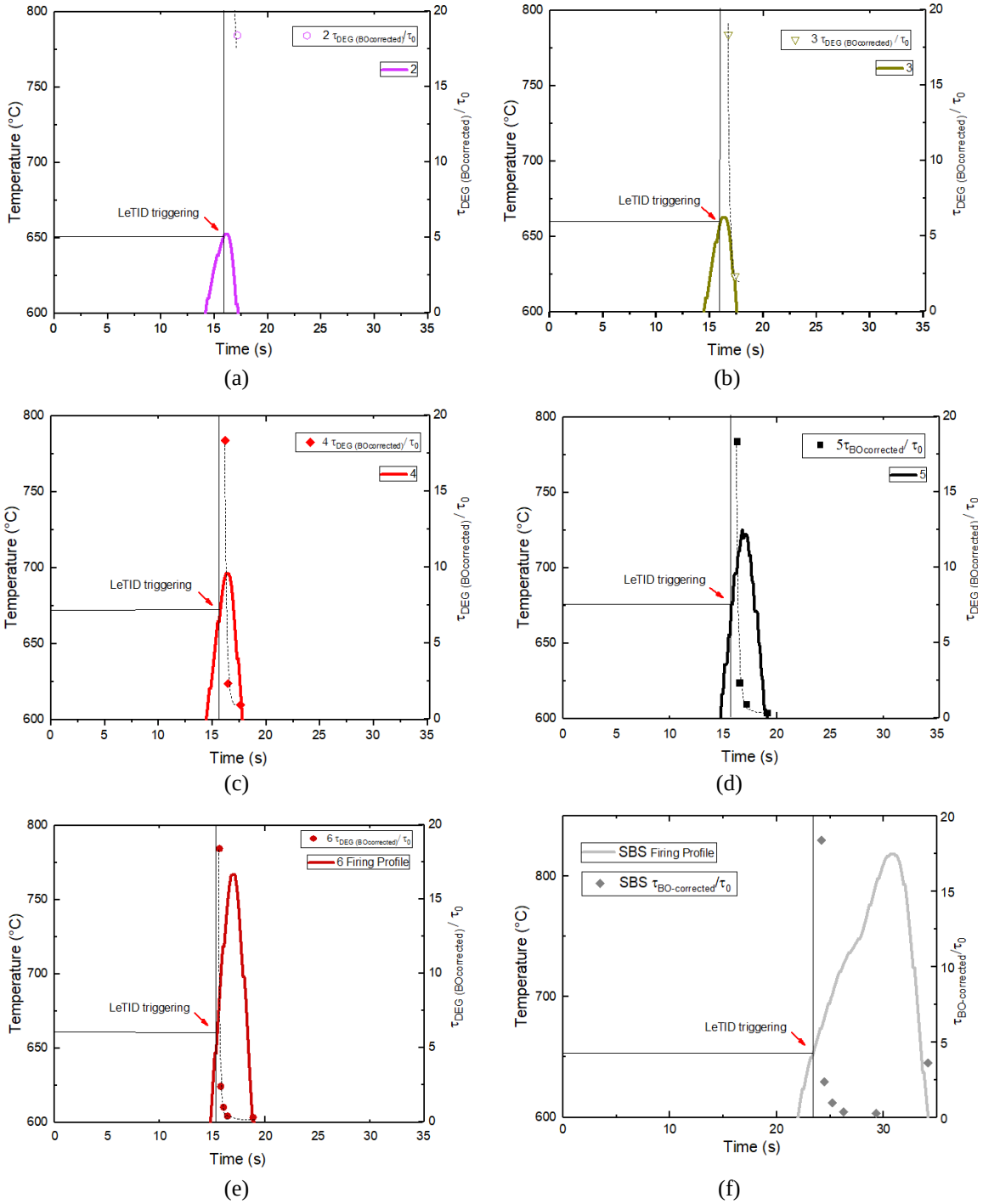
Table 10 – Model B with LeTID triggering temperature for each firing profile, assuming when the thermal budgets above 600°C value reached 50°C.s.

Firing Profiles	**#1**	**#2**	**#3**	**#4**	**#5**	**#6**	**SBS**
Peak Temperature (°C)	600,8	652,4	662,6	696,1	725,1	766,9	818,6
Thermal Budget >600°C (°C.s)	0,31	98,1	118,6	189,1	309,8	796,3	1557
Triggering Temperature (°C) *when Thermal Budget >600°C* = 50°C.s		651	660	672	676	661	653

Source: Author

The triggering temperatures, in Table 10, vary considerably and present higher values if compared with model A fixed triggering temperature of 640°C. In profiles #2 to #4, triggering temperatures were close to each peak temperature. Profile #5 presented the highest triggering temperature of 676°C. In profile #6 and in SBS the triggering temperatures were lower than in #5. Figure 56 from (a) to (f) show the model B for the formation of LeTID defects inside the firing furnace with the triggering temperature related to a thermal budget above 600°C of 50°C.s. Perhaps variable triggering temperature is more appropriate if the triggering is indeed related to the thermal budget. However, the model A of fixed trigger temperature should be more applicable, taking into account that a chemical reaction is necessary to form the defect. Hence, a triggering thermal budget may be even a more appropriate choice then model A.

Figure 56 - Model B for the formation of LeTID defects inside the firing furnace from profiles #2, #3, #4, #5, #6 and SBS. Triggering temperature related to a thermal budget above 600°C of 50°C.s.



Source: Author

The two models, A and B, can be taken into account in future investigations. One possible way to investigate LeTID formation mechanism is testing firing profiles with peak temperatures lowers then 640°C, such as 600°C or even lower, and with higher and much higher thermal budgets. If in those cases, higher thermal budget with temperatures lower than 640°C results in LeTID, presumably, thermal budget above

600°C can be considered the main factor for LeTID formation. If no LeTID is found, then a fixed triggering temperature is more likely to describe the formation mechanism. What is even more important, in our view, is to uncouple the suppression mechanism of the LeTID defects inside firing furnace from the triggering defect formation.

4.2.1.4.2 Models for emptying LeTID defects reservoir

As previously shown, SBS firing process resulted in a partially suppressed LeTID, which were considered even less detrimental to the effective lifetime that the BO-related LID. Two possibilities exist for the firing process to have led to this LeTID suppression. The firing process minimally formed the LeTID defects; or the firing process formed the defects and, soon after, partially suppressed them. Howsoever, all that we have analyzed so far with regard to the formation of the LeTID defects reservoir leads us to take more into account the formation/suppression possibility. Therefore, the mechanism for emptying of LeTID defects from the reservoir is analyzed in terms of four factors: heating and cooling ramp, time above 600°C and thermal budget above 600°C.

SBS profile, in comparison to the others, showed slower heating ramp, considerably higher thermal budget above 600°C and similar cooling ramp (Table 9). In the two previous considered LeTID defect formation models A and B, the triggering temperature would be 640°C and 653°C, respectively, showing a short distance between both. It is thus possible that the slower heating ramp does not anticipates the triggering of the LeTID formation. The thermal budget above 500°C does not seem to be a good parameter, as it resulted in conflicting results that would not explain the difference between profile #5 and #6 lifetime degradations. The temperatures between 500°C and 600°C are, then, considerably less relevant for defect formation than temperatures above 600°C. All these analyses suggests that a slow ramp before 600°C minimally (or does not) affect the formation of the LeTID defect. This topic is not clearly discussed in the literature and can be the subject of future investigations.

From above discussions, all profile cooling ramps had similar values between the peak temperature and 400°C as shown in Table 9. If the proposed models A and B of formation of the LeTID defects reservoir are applicable, the cooling ramp plays a minor role. Also, it suggests that the LeTID defect reservoir may be partially emptied if the cooling ramp is considerably slower, leading to a higher thermal budget above 600°C, or possibly, in this case of reservoir emptying, a thermal budget of above 500°C or 400°C.

Possible different mechanisms of formation of the LeTID regarding cooling ramp will be discussed later.

Another possibility for relating the firing profiles to the formation of the LeTID defects is the time at which the profile is above 600°C, 700° C and 800°C. These values were shown in Table 9. Profile # 5 stays more time above 600°C than profile # 6, but shows less degradation of the BOcorrected lifetime. This suggests that higher thermal budgets at these temperatures have significant effects on the formation of the defects. SBS profile stays more time above 700°C than profile #6, but shows less degradation of the BOcorrected lifetime. It is known from Eberle et al. study [152] that this is only possible because there is a different heating and/or cooling ramp and/or a different thermal budget.

Since the other possibilities have been at first ruled out, the LeTID defect reservoir emptying process in the firing furnace is considered to be influenced by the thermal budget, where, unlike the cooling ramp and the heating ramp, would be the main cause of the reduction of the quantity of LeTID defects. The emptying process of LeTID defects reservoir is seen in cycles of dark/illuminated annealing at temperatures up to 230°C in Ref. [166]. It is therefore considered, also as in our view of the resulting LeTID from SBS profile that the furnace conditions above 600°C generates a high rate of charge carriers, which promotes the emptying of the LeTID defects reservoir.

In order to analyze this proposed model of emptying the LeTID defect reservoir into the firing furnace, we used the data of Figure 53(b) to calculate the rate of defect formation and the rate of emptying of LeTID defects reservoir as $\boldsymbol{\sigma_{\mathbf{DEG\ (BO-corrected)}}} \cdot \boldsymbol{\sigma_0}^{-1}$ / °C.s. Table 11 presents the calculated rates and other parameters. First, the defect emptying rate is calculated as the difference between SBS and #6 $\boldsymbol{\sigma_{\mathbf{DEG\ (BO-corrected)}}} \cdot \boldsymbol{\sigma_0}^{-1}$ divided by the difference between SBS and #6 thermal budget above 600°C and assuming that it is a constant value among thermal budgets above 600°C, and started when defect formation started. Thus, we are assuming that there is the defect emptying process at the same time as the formation. Defect formation rate is calculated as the difference between Bo-corrected degradation divided by the difference between thermal budgets of sequential profiles, the resulted rate is plotted in the former profile with the addition of the defect-emptying rate. The resulted graph is shown in Figure 57.

Table 11 – Calculated rate of defect formation and the rate of emptying of LeTID defects reservoir, considered represented by the difference between maximum normalized BOcorrected lifetime degradations under illuminated annealing for each profile divided by the difference between thermal budgets above 600°C.

Firing Profiles	**#1**	**#2**	**#3**	**#4**	**#5**	**#6**	**SBS**
Peak Temperature (°C)	600,8	652,4	662,6	696,1	725,1	766,9	818,6
$\boldsymbol{\sigma_{\mathbf{DEG\ (BO-corrected)}}/\sigma_0}$		18,4	2,37	0,965	0,371	0,284	3,61
Defect formation rate $\boldsymbol{\sigma_{\mathbf{DEG\ (BO-corrected)}}\cdot\sigma_0^{-1}}$ **/ °C.s^{-1}**	0	0,78758	0,02429	0,00930	0,00455	0,00437	0
Defect emptying rate $\boldsymbol{\sigma_{\mathbf{DEG\ (BO-corrected)}}\cdot\sigma_0^{-1}}$ **/ °C.s^{-1}**	0	0,00437	0,00437	0,00437	0,00437	0,00437	0,00437

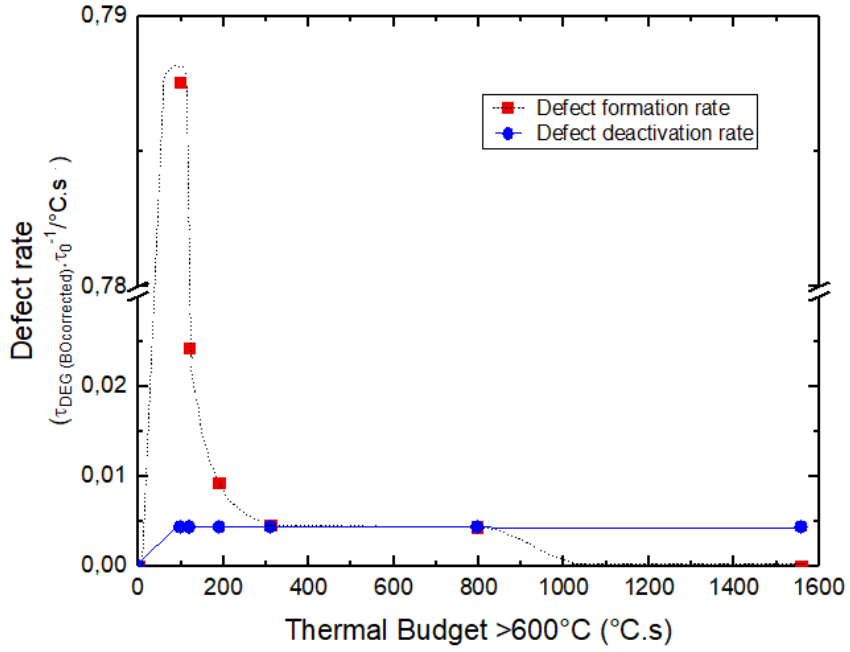
Source: Author

In Figure 57, a break was placed between 0.004 and 0.78 on the axis of the abscissa. This shows how much high is the defect formation rate at the beginning of the formation. The drop of the defect formation rate is also fast, from 0.78 to 0.03 in a difference of just about 20°C.s. The defect formation rate gets close to the defect emptying rate already in profile #5, around 300°C.s. Between profile #5 and #6 defect emptying rate is higher than defect formation rate, thus, the reservoir initiate the emptying process.

The Figure 57 is a fitted derivative of Figure 53(b). However, it is difficult to state if it describes precisely the formation and emptying of the LeTID defect reservoir inside the furnace. Several assumptions were considered to plot both figures. The most decisive was that there is a path of LeTID defect reservoir inside the firing furnace. Regardless of the accuracy of the plotted values, we understand that there are two parallel processes, one of formation and one of emptying of defects in the reservoirs. The formation possibly occurs by the hydrogen binding with the X species forming the defect, and the emptying occurs by the rupture of this bond by the charge carrier created under these high temperature conditions, in other words, by the cumulative elimination of the defects from the reservoir.

According to Figure 57, there is an abrupt formation and a rapid filling of the defect reservoir, while the emptying rate is very slow if compared to the initial formation rate. That is, the formation of defects is a step function related with a specific temperature or a specific thermal budget while the emptying of the defects varies only depending on the thermal budget, but at much lower rates.

Figure 57 – Calculated rate of defect formation, considered represented by the difference between maximum normalized BOcorrected lifetime degradations under illuminated annealing for each profile divided by the difference between thermal budgets above 600°C, using data from Table 9. Rate of emptying of LeTID defects reservoir is considered equal to the rate between #5 and SBS.



Source: Author

Assuming that there is this path of the LeTID defects inside the firing furnace described by Figure 51, and analyzing the resulting LeTID of the SBS profile, we consider that the defect reservoir begins to be emptied between the thermal budgets above 600°C of 900°C.s and 1500°C.s. The fast decrease in defect formation rate is probably due to the fulfilling of the reservoir, which may be explained by the decrease in the available amount of hydrogen or X specie that binds with hydrogen to create the defect.

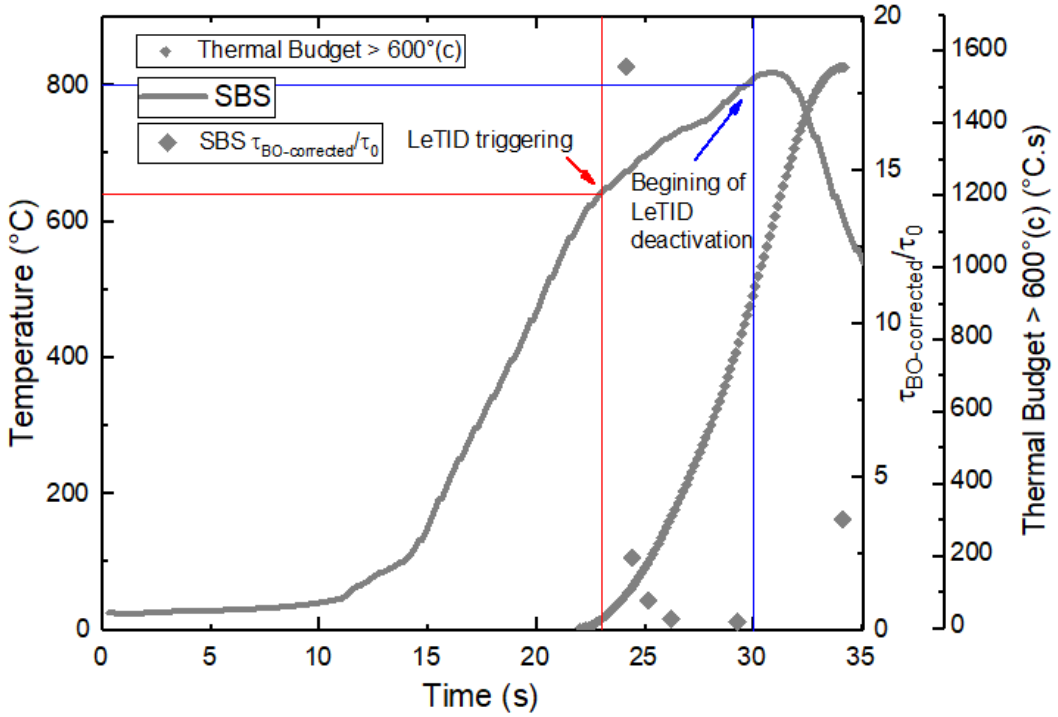
There are three possible explanations for why this reservoir is not continually re-filled to the point it is always full. The first, less plausible, is that the furnace conditions are different at that specific time when reservoir is fulfill and formation of defects does not takes place anymore. The second, is because the increasing number of the new specie formed by the combined charge carrier-LeTID defect serve as barriers to more LeTID defect formation, as would be the case if hydrogen have opposite charge states before and after LeTID defect reservoir formation and emptying, or if, only, hydrogen becomes unavailable as this new specie is formed. The third possibility is that the emptying defect rate is only higher than formation rate at temperatures below the LeTID triggering temperature, and in higher temperatures, the reservoir does tends to be always full.

The defects emptying rate is considered to be related to the thermal budget above 600°C, but may be relevant at temperatures below 600°C. This should not apply to

the defects formation rate. Thus, depending on the influence that lower temperatures than 600°C have on emptying LeTID defects reservoir, cooling ramp can be a more or less important factor.

In a view of the results discussed so far, we propose two possible models for emptying LeTID defects inside the firing furnace. The first model (1) is shown in Figure 58. The emptying of the LeTID defects reservoir in the firing furnace is considered a function of the thermal budget above 600°C. At a thermal budget above 900° C.s, the emptying process begins and when is 1500°C.s, LeTID defects are largely suppressed, showing a maximum normalized BOcorrected lifetime degradation, which is LeTID representative, of approximately 3.6. In Figure 58, the formation of defects is considered starting at the fixed temperature of 640°C, as model A, previous shown in Figure 54(k).

Figure 58 – Model 1 for the emptying of the LeTID defects reservoir inside the firing furnace, considered as a function of the thermal budget above 600°C.



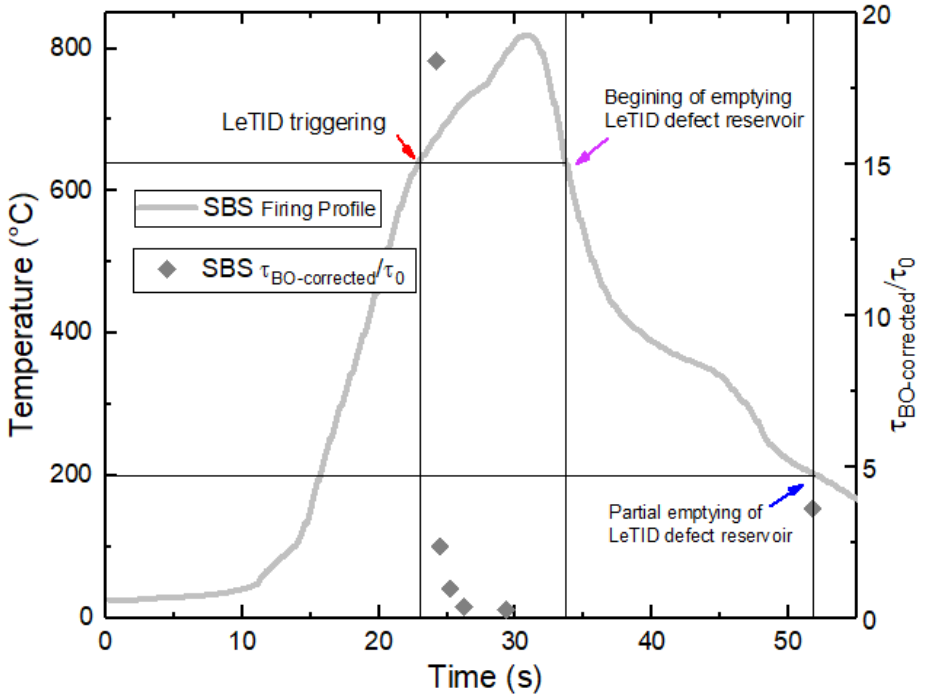
Source: Author

The direct influence of other possible factors in the emptying of the of LeTID defects reservoir in model 1, such as heating and cooling ramps, are ruled out. Therefore, we propose as a final result for this model and if the model is applicable, that a thermal budget above 600°C of at most 1500°C.s will be desirable for the firing profile to guarantee a process with satisfactory suppression of the LeTID defects.

It is likely that the quality of contact formation will be affected under this firing profile thermal budget above 600°C of 1500°C.s. Therefore, a compromise relation between LeTID suppression and wafer quality is required. To do so, the investigation on the feasibility of process with profiles with thermal load above 600°C lower than 1500°C is a suggestion for future work. Studying profiles with very high peak temperature, and consequently high thermal budget, can help to understand the importance and/or the limitation of the influence of the thermal budget or temperature on emptying the reservoir of LeTID defects.

The second proposed model for emptying LeTID defects inside the firing furnace, model 2, is shown in Figure 59. The formation of defects is considered starting at the fixed temperature of 640°C, as model A, previous presented in Figure 54. The reservoir of LeTID defects formation is function of the thermal budget above 600°C. The maximum normalized BOcorrected lifetime degradation values in time represents this reservoir formation. In model 2, the beginning of emptying LeTID defect reservoir is considered only when temperature in profile is down to triggering temperature again. From triggering temperature to 200°C, the LeTID defect reservoir is partially emptied to a normalized BOcorrected lifetime degradation of 3.61. Model 2, therefore, is based on two main considerations. The first is that the LeTID defect reservoir does not start emptying if the temperature is above the trigger temperature, i.e. at higher temperatures, new defects formation refill the reservoir, keeping it always full. The second consideration is that at temperatures below 640°C, and according to the cooling ramp seen in the SBS profile, the emptying rate of the LeTID defects reservoir is enough to suppress the LeTID.

Figure 59 – Model 2 for the emptying of the LeTID defects reservoir inside the firing furnace, considered as begging after the cooling ramp pass through the LeTID triggering temperature.



Source: Author

4.2.1.4.2 Comparing results and proposed models with literature

The objective in this study of the LeTID defects related to firing profiles is not to find an ideal firing profile that would overcome LeTID. What we investigate, are possible models and metrics of formation and emptying of the LeTID defect reservoirs inside the firing furnace. With this, we analyzes relevant information about the dynamics of the defect and seek for answers to what can and what cannot explain the defect mechanisms. To validate the proposed models A and B for LeTID defects reservoir formation and models 1 and 2 for LeTID defects reservoir emptying, the models and results are compared with those found recently in the literature. To do so, Table 12 summarizes this study results and models and relates with some results from literature.

Our results are in accordance whit R. Eberle et.al. [152] and D. Chen et al. [165] in terms of resulting LeTID compared with the firing profiles. In Table 12, we compare peak temperature, thermal budget above 600°C, heating and cooling ramp between peak temperature of the profile and 400°C, time above 600°C and if the resulting LeTID is a full degradation curve, a partial degradation curve (minor then the full), or none degradation curve (also almost none degradation).

As discussed before, it was found by R. Eberle that is possible to produce a virtually LeTID free wafer with a high peak temperature firing profile. We confirm this result with the SBS firing profile, which resulted in a very low degradation caused by the LeTID defect (Figure 47). Comparing the SBS profile with Eberle´s 800°C and 850°C RTP profiles (Ref 1b and Ref 1c), is possible to see that the thermal budget above 600°C is the variable with a similar value of 1000 and 1500 °C.s. SBS heating ramp was also similar of 36°C.s for SBS and 40°C.s for Ref 1b and Ref 1c, while SBS cooling ramp was slightly faster than Refs 1b and 1c, of 51°C.s and 40°C.s, respectively. Eberle´s FFO firing profile (Ref 1a) is comparable with profile #6. Ref 1a shows faster heating and cooling ramps and less thermal budget above 600°C but seemly same observed full LeTID. Eberle cut the ramp speeds by a bit more than half and get a free LeTID result. In our case, we can say that we only cut the heating ramp speed by half. Consequently, in both cases, the time above 600°C doubled or little more than that.

D. Chen´s showed an 815°C peak temperature firing profile and resulting in a strong LeTID (Ref 2a), which is comparable with firing profile #6. Both showed full LeTID and comparable firing profile parameters. D. Chen´s profiles with lower peak temperatures (Ref 2b and Ref 2c) are comparable with previously showed profile #5 (Figure 47). Both Ref 2b and 2c partial LeTID are due to the lower peak temperature, thus the partial fulfillment of the LeTID defects reservoir as discussed before and showed in Figure 54(g).

Table 12 – Results for profiles #5 and SBS compared with results from literature

Results	**#6**	**SBS**	**Ref 1a**	**Ref 1b**	**Ref 1c**	**Ref 2a**	**Ref 2b**	**Ref 2c**
Peak Temperature (°C)	767	820	800	800	850	815	744	715
Thermal Budget >600°C (°C.s)	800	1560	500	1000	1500	645	360	287
Heating ramp (400°C - T peak)	86	36	100	40	40	70	57	47
Cooling ramp (T peak - 400°C)	65	51	100	40	40	70	57	47
Time above 600°C	4	12	5	10	12	6	5	5
Resulting LeTID? (full, partial or none)	full	none	full	none	none	full	partial	partial

Source: Author, R. Eberle et.al. [152] and D. Chen et al. [165]

In Table 13, we proceeded a little more difficult comparison, that is of the profiles # 6 and SBS with results from C. E. Chan et al. [156] that performed firing profiles with the same sample, twice. Thus, in addition to the initial firing profile, with

peak temperature parameters, thermal budget above 600°C, heating and cooling ramps between the peak temperature and 400°C and the time above 600°C, we added the parameters of the second firing, specifically, the accumulated thermal budget after the two firing processes and the resulting LeTID.

C. E. Chan et al. [156] performed a standard firing profile with a peak temperature of 760°C, comparable with profile #6, resulting in a full LeTID. A second fast ramp firing profile was performed using different peak temperatures. The 750°C peak temperature (Ref 3d) in the second firing resulted in a full LeTID, while 700°C (Ref 3c) resulted in partial LeTID, 660°C (Ref 3b), none, and 565°C (Ref3a), a partial LeTID. All Chen´s firing profiles resulted in a low thermal budget above 600°C that is why, the accumulated thermal budget after the two firing were only 720°C.s or less. This corresponds to half of the SBS thermal budget above 600°C.

R. Sharma et al. [167] results shows that the sequence of the different firing profiles do influences the resulted LeTID. With a first profile with a peak temperature of 800°C, comparable with profile #6, resulted in a full LeTID, and a second with a peak of 550°C (Ref 4a), resulted in a partial LeTID, which is in accordance with Ref 3a. If doing the opposite (Ref 4b), a full LeTID is observed.

Table 13 – Results for profiles #5 and SBS compared with results from literature that performed two sequential firing process with the same sample

Results	**#6**	**SBS**	**Ref 3a**	**Ref 3b**	**Ref 3c**	**Ref 3d**	**Ref 4a**	**Ref**
Peak Temperature (°C)	767	820	760	760	760	760	800	55(
Thermal Budget >600°C (°C.s)	800	1560	less then 360	less then 360	less then 360	360	500	0
Time above 600°C	4	12	5	5	5	5	5	0
Resulting LeTID? (full, partial or none)	full	none	full	full	full	full	full	non
Peak Temperature 2nd Annealing	-	-	565	660	700	750	550	80(
Accumulated Thermal Budget >600°C (°C/s)	800	1560	less then 720	less then 720	less then 720	720	500	50(
Resulting LeTID? (full, partial or none)	-	-	partial	none	partial	full	partial	ful

Source: Author, C. E. Chan et al. [156] and R. Sharma et al. [167]

C. E. Chan et al. [156] re-firing studies in comparison with our results indicates the possibility of suppress LeTID with lower thermal budgets above 600°C, which we consider desirable to guarantee a feasible contact quality. Chan discuss this contact quality problems in a re-firing process, thus assumes that is better to suppress

LeTID in a one firing step. Therefore the importance to understand e validate the mechanisms of LeTID defect reservoir formation and emptying.

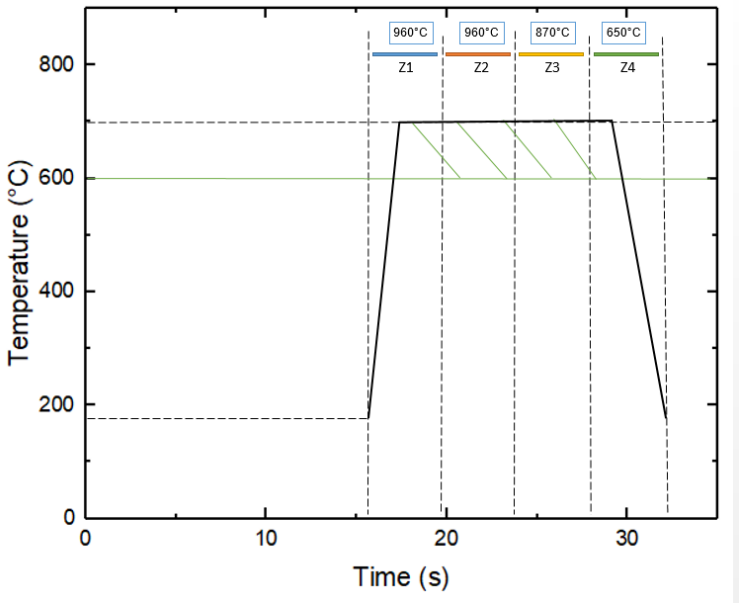
Assuming C. E. Chan et al. [156] results and comparing with proposed models 1 and 2 for emptying LeTID defect reservoir, it is possible to note that even at a peak temperature of 565°C (Ref 3a), the re-firing did not promote the total emptying of LeTID defects. This was only achieved in the profile with a peak temperature of 660°C (Ref 3b). The 700°C and 750°C peak temperatures profiles (Ref 3c and 3d), showed that the LeTID reservoir can be refilled in these same conditions that filled reservoir at the first firing. Therefore, temperatures around 600 to 660°C (and possibly little more) may be crucial for the rapid emptying of the defect reservoir without refilling. Moreover, at temperatures below 600°C, the rate of emptying has already dropped considerably. This can be seen in the results from Yli-Koshi et al. [168], where a annealing at 350°C to suppress the LeTID defects took 30 minutes. Thus, the 400-200°C SBS slower cooling ramp (Figure 59) influence on LeTID defects suppression is ruled out.

In addition, the possibility that the reservoir emptying actually occurs only below the LeTID trigger temperature, stipulated by model 2, is restricted in this case. There is only one second available for the defect reservoir emptying at a cooling ramp of 50°C.s for profile SBS, between 650°C and 600°C. Therefore, it seems plausible, that a midterm between the two models 1 and 2 is closer to the real dynamic. Therefore, the dynamics of reservoir emptying and reservoir refilling at temperatures above 650°C must be further investigated. The possible different dynamics have already been listed and discussed previously. Finding the actual formation-emptying dynamic will result in a far better understanding of the LeTID defect.

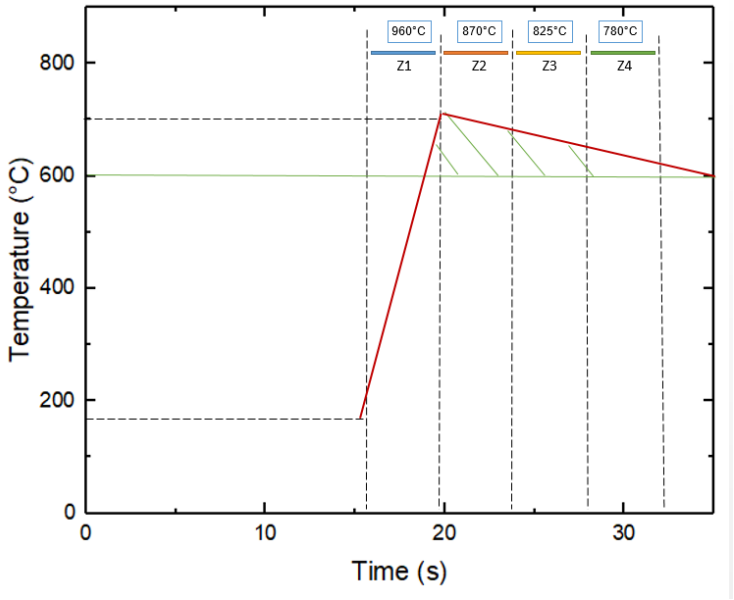
If any of the proposed models in this study is applicable, still taking into account the results of the literature, and the quality of the contact formation, some characteristics of the firing profile are desirable anyway. Among them: reaching triggering condition for the formation of the LeTID defects reservoir as soon as possible, inside the firing furnace, which means a fast heating ramp; rapid reaching of peak temperature for contact formation around 700°C; a post-period of 4 to 6 seconds at temperatures close to 650°C to satisfactorily emptying LeTID defects reservoir. Depending on which emptying model is most applicable, 1 or 2, the profile curve may be more or less square or triangular. In Figure 60, two profiles are simulated, presented according to the applicability of model 1 (a) or model 2 (b). As the zones of the firing furnace are fixed, to reach the proposed parameters for the firing profile, the speed of the

belt must be close to that of the SBS profile, of 260 cm.min^{-1}. For the firing profile simulated in (a), the temperature close to 700°C enables contact formation, and at some point, the reservoir of LeTID defects starts emptying. For the simulated profile in (b), the temperature of 700°C is also fast-reached for contact formation, and is slowly decreased so that there is enough time, and at a lower temperature range, between 650°C and 600°C for satisfactory emptying of LeTID defects. Therefore, if the refilling of the reservoir of the LeTID defects is always high intense at temperatures above 700°C, (b) is more applicable for the suppression of LeTID. If the emptying of the LeTID defect reservoir is higher than formation at some point at temperatures above 700°C, it is possible that (a) is even more effective than (b) even for faster belt speeds that could be desirable.

Figure 60 – Simulated firing profiles according to the applicability of model 1 (a) or model 2 (b). As the zones of the firing furnace are fixed, to reach the proposed parameters for the firing profile, the speed of the belt is close to that of the SBS profile, of 260 cm.min^{-1}. Set temperatures for each zone of furnace are proposed values. The real repercussion of these temperatures in the profile are not regarded.



(a)



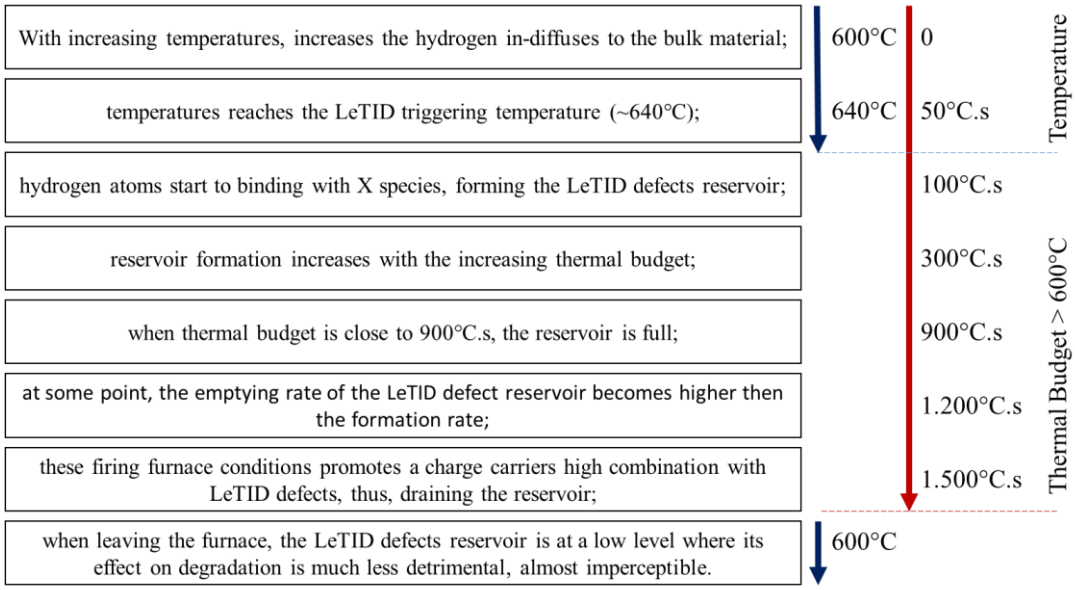
(b)

Source: Author

Lastly, based on all discussions, we propose that future investigations with respect to the impact of firing profiles on the observed LeTID, to test these different profiles from Figure 60, in addition to some others that potentially help to explain the dynamics of the defects. For the LeTID defect reservoir formation: profiles with a high thermal budget above 600°C but with a peak temperature not exceeding the triggering temperature of 640°C. For the LeTID defects reservoir-emptying model: profiles with even higher peak temperature, with rapid ramps and thermal budgets above 600°C higher than 1500°C.s.

We have shown key findings that supports investigations on feasible firing profiles capable of overcoming LeTID or, in the latter case, producing a wafer that needs a much faster and less expensive post treatment for LeTID suppression. The overall proposed LeTID defect mechanism for formation and emptying reservoir is summarized in Figure 61.

Figure 61 – Summary for the overall proposed LeTID defect mechanism for formation and emptying reservoir for the studied SBS sample.



Source: Author

5 CONCLUSION

To measure the Brazilian quartz acquired by IPEN and to investigate the acid leaching purification route, the impurities content in the materials resulted from processes are measured with ICP-OES and compared with the literature. For the reduction of Quartz into metallic silicon, magnesiothermic reduction were conducted in IPEN laboratory. The result material is Si with MgO, which was then HCl leached. Another route is taken into account, the carbothermic reduction. Commercial carbothermic silicon was acquired and micronized. Both magnesiothermic and carbothermic silicon was subjected to a leaching in HCl + HF solution. The final percentage of silicon purity was calculated for the purified magnesiothermic silicon as 99,12% and as 99,15% for purified carbothermic silicon. The high Boron content in the resulting silicon is responsible for the insufficient purity for the material to be considered UMG-Si. If reaching a Boron content of 50ppm, for example, both materials would achieve a purity of 0.9987% and 0.9999%, respectively. Therefore, a process for Boron removal, such as slagging, is necessary to produce an ultra-metallurgical grade purity silicon. After a successful slagging, the ultra-metallurgical grade silicon can already be used in the manufacture of solar cells. For this, the silicon can be processed in the directional solidification furnace with a good expected process yield.

The degradation and recovery of the bulk minority carrier lifetime in commercial high performance multicrystalline p-type wafers subjected to different contact firing profiles has been measured under simultaneous heating and illumination. In addition, the lifetime behavior of an unfired and undiffused wafer has been measured under identical conditions. This unfired wafer demonstrated a decay to about 50% of its initial lifetime after two minutes of illumination at 150°C, followed by a recovery in the next hours of illuminated annealing. This behavior is attributed to BO-related degradation, as the LeTID defect was never activated. Samples fired at processes with peak temperatures of 601°C and 652°C both showed lifetime degradation curves comparable to the unfired sample. The degradation in these wafers is therefore assumed to be mainly caused by BO-defects. A strong degradation upon illuminated annealing, resulting in lifetimes as low as 20% of the initial lifetime, can be seen in wafers subjected to a simulated contact firing process with higher peak temperatures. This additional decay and recovery is usually referred to as LeTID. A contribution from BO-defects to the total

degradation in the fired samples is confirmed by subjecting a fired wafer to a low intensity illumination at room temperature for 72 hours. A degradation down to 50-60% of the initial lifetime is seen, which is comparable to the decay in unfired wafers.

A method for subtracting the contribution of BO-defects from the measured lifetime is proposed to isolate and evaluate the effect of the LeTID defects on the lifetime evolution. By assuming that the lifetime in the wafer fired at the lowest temperature is mainly limited by the BO-defect, this contribution can be subtracted by measured lifetimes to get a BO-corrected lifetime. We then assume that this BO-corrected lifetime mainly represents the LeTID recombination. The BO-corrected lifetime reaches a minimum between 30 and 90 minutes of illuminated annealing, indicating a maximum concentration of recombination active LeTID defects. A high peak firing temperature result in a more severe LeTID degradation, while the magnitude of the LeTID is reduced gradually for decreasing peak temperatures. Despite a high peak temperature, the wafer subjected to a firing process with slow belt speed show a largely suppressed LeTID. The higher thermal budget combined with the slow heating ramp is possibly enabling an annealing that induces carriers to suppress LeTID defects. The nature of this LeTID suppression is investigated and LeTID defect mechanisms for formation and emptying reservoir are proposed. A path of formation and emptying of LeTID defects inside firing furnace is taken into consideration. We propose that the formation and the emptying of the reservoir are given by different mechanisms, the first related to hydrogen binding with a X specie, fast forming the defect after a triggering temperature, the second with the constant and relatively slower combination between charge carriers and LeTID defects, promoted by the furnace high temperatures conditions. A series of suggestions for future investigations are related with testing more different firing furnace profiles that can indicate the formation and suppression of LeTID defects reservoir inside the firing furnace.

Both silicon purification and light induced degradation (LID) characterization in multicrystalline silicon give a wide range for investigation on processes and new production routes. Combined, silicon from new purification and production routes can pass through adapted crystallization and solar cells processes, such as gettering and firing aiming potential and competitive routes for silicon solar cell production.

REFERENCES

[1] Intersolar Europe, “Global Market Outlook for Solar Power / 2018 -2022,” 2018.

[2] P. R. S. V. Masson-Delmotte, P. Zhai, H. O. Pörtner, D. Roberts, J. Skea, M. I. G. A. Pirani, W. Moufouma-Okia, C. Péan, R. Pidcock, S. Connors, J. B. R. Matthews, Y. Chen, X. Zhou, and T. W. E. Lonnoy, T. Maycock, M. Tignor, “Global warming of 1.5°C. An IPCC Special Report on the impacts of global warming of 1.5°C above pre-industrial levels and related global greenhouse gas emission pathways, in the context of strengthening the global response to the threat of climate change ,” 2018.

[3] UNFCCC. Conference of the Parties (COP), “ADOPTION OF THE PARIS AGREEMENT - Conference of the Parties COP 21,” *Adopt. Paris Agreement. Propos. by Pres.*, vol. 21932, no. December, p. 32, 2015.

[4] C. Breyer *et al.*, “Solar photovoltaics demand for the global energy transition in the power sector,” *Prog. Photovoltaics Res. Appl.*, vol. 26, no. 8, pp. 505–523, 2018.

[5] C. Le Quéré *et al.*, “Global Carbon Budget 2018,” *Earth Syst. Sci. Data*, vol. 10, no. 4, pp. 2141–2194, Dec. 2018.

[6] D. Knob, “Geração de hidrogênio por eletrólise da água utilizando energia solar fotovoltaica,” Universidade de São Paulo, São Paulo, 2014.

[7] S. T. Thompson *et al.*, “Direct hydrogen fuel cell electric vehicle cost analysis: System and high-volume manufacturing description, validation, and outlook,” *J. Power Sources*, vol. 399, no. March, pp. 304–313, 2018.

[8] Y. Ligen, H. Vrubel, and H. H. Girault, “Mobility from renewable electricity: Infrastructure comparison for battery and hydrogen fuel cell vehicles,” *World Electr. Veh. J.*, vol. 9, no. 1, 2018.

[9] California Air Resources Board, “2018 Annual Evaluation of Fuel Cell Electric Vehicle Deployment & Hydrogen Fuel Station Network Development,” no. July, 2018.

[10] OPEC, “World Oil Outlook 2040,” Nov. 2017.

[11] J. Jean, P. R. Brown, R. L. Jaffe, T. Buonassisi, and V. Bulović, “Pathways for solar photovoltaics,” *Energy Environ. Sci.*, vol. 8, no. 4, pp. 1200–1219, 2015.

[12] D. Sarti and R. Einhaus, “Silicon feedstock for the multi-crystalline photovoltaic industry,” *Sol. Energy Mater. Sol. Cells*, vol. 72, no. 1–4, pp. 27–40, 2002.

[13] E. Lobato, “A Mineraçao Brasileira. Relatório Técnico 37. Perfil do Quartzo,” p. 32, 2009.

[14] M. A. R. R. Pedro Sérgio Landim de Carvalho, Pedro Paulo Dias Mesquita, “A rota metalúrgica de produção de silício grau solar: uma oportunidade para a indústria brasileira?,” *BNDES Setoria*, vol. 40, pp. 205–234, 2012.

[15] P. J. Knob, H. G. Riella, and D. Knob, “Energia Solar Fotovoltaica Auxiliando Na Redução Dos Picos Anuais De Demanda,” in *10º Congresso sobre Geração Distribuída e Energia no Meio Rural*, 2014.

[16] E. B. Pereira, F. R. Martins, S. L. de Abreu, and R. Ruther, “Brazilian atlas of solar energy - SWERA,” São José dos Campos, 2006.

[17] D. Romeiro, E. De Almeida, and L. Losekann, “A Escolha de Tecnologias de Geração Elétrica Despacháveis versus Intermitentes e o Caso Brasileiro - The choice of dispatchable versus intermittent electricity generating technologies and the Brazilian case,” pp. 1–14, 2014.

[18] D. Knob, P. J. Knob, and H. G. Riella, “Photovoltaic solar energy as a solution for the supply of annual demand peaks in Brazil,” *to be Publ.*, 2019.

[19] EPE, “Plano decenal de expansão de energia 2027,” 2017.

[20] N. Edition, “International Technology Roadmap for Photovoltaic— Results 2017 including maturity report 2018,” *Ninth Ed.*, no. September, 2018.

[21] P. Frankl and S. Nowak, “Technology roadmap: solar photovoltaic energy,” OECD Publishing, May 2010.

[22] V. V. Tyagi, N. a. a. Rahim, N. a. Rahim, and J. a. /L. Selvaraj, “Progress in solar PV technology: Research and achievement,” *Renew. Sustain. Energy Rev.*, vol. 20, pp. 443–461, Apr. 2013.

[23] L. Zhang and A. Ciftja, “Recycling of solar cell silicon scraps through filtration, Part I: Experimental investigation,” *Sol. Energy Mater. Sol. Cells*, vol. 92, no. 11, pp. 1450–1461, 2008.

[24] B. Mitchell, “Photoluminescence characterisation of silicon bricks,” THE UNIVERSITY OF NEW SOUTH WALES, 2013.

[25] M. Di Sabatino, S. Binetti, J. Libal, M. Acciarri, H. Nordmark, and E. J. Øvrelid, “Oxygen distribution on a multicrystalline silicon ingot grown from upgraded metallurgical silicon,” *Sol. Energy Mater. Sol. Cells*, vol. 95, no. 2, pp. 529–533, 2011.

[26] T. Niewelt, F. Schindler, W. Kwapil, R. Eberle, J. Schön, and M. C. Schubert, “Understanding the light-induced degradation at elevated temperatures: Similarities between multicrystalline and floatzone p-type silicon,” *Prog. Photovoltaics Res. Appl.*, no. October, pp. 1–10, 2017.

[27] K. O. Davis *et al.*, “Manufacturing metrology for c-Si photovoltaic module reliability and durability, Part I: Feedstock, crystallization and wafering,” *Renew. Sustain. Energy Rev.*, vol. 59, pp. 84–106, 2016.
[28] S. Pizzini, “Towards solar grade silicon: Challenges and benefits for low cost photovoltaics,” *Sol. Energy Mater. Sol. Cells*, vol. 94, no. 9, pp. 1528–1533, 2010.
[29] I. Buchovska, O. Liaskovskiy, T. Vlasenko, S. Beringov, and F. M. Kiessling, “Different nucleation approaches for production of high-performance multi-crystalline silicon ingots and solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 159, pp. 128–135, Jan. 2017.
[30] T. Trupke, B. Mitchell, J. W. Weber, W. McMillan, R. a. Bardos, and R. Kroeze, “Photoluminescence Imaging for Photovoltaic Applications,” *Energy Procedia*, vol. 15, no. 2011, pp. 135–146, Jan. 2012.
[31] F. Kersten *et al.*, “Degradation of multicrystalline silicon solar cells and modules after illumination at elevated temperature,” *Sol. Energy Mater. Sol. Cells*, vol. 142, pp. 83–86, 2015.
[32] R. R. Silva, “PURIFICAÇÃO HIDROMETALÚRGICA DO SILÍCIO OBTIDO POR MAGNESIOTERMIA,” Universidade Federal de Santa Catarina, 2016.
[33] F. Ebrahimfar and M. Ahmadian, “Purification of Metallurgical-Grade Silicon by Acid Leaching,” 2018.
[34] T. U. Nærland, *Characterization of light induced degradation in crystalline silicon*, no. November. 2013.
[35] T. U. Naerland, H. Haug, H. Angelskar, R. Sondena, E. S. Marstein, and L. Arnberg, “Studying Light-Induced Degradation by Lifetime Decay Analysis: Excellent Fit to Solution of Simple Second-Order Rate Equation,” *IEEE J. Photovoltaics*, vol. 3, no. 4, pp. 1265–1270, Oct. 2013.
[36] T. U. Nærland *et al.*, “The role of excess minority carriers in light induced degradation examined by photoluminescence imaging,” *J. Appl. Phys.*, vol. 112, no. 2012, 2017.
[37] Rune Søndenå1a & Marie Syre Wiig, “Evidence of three different light induced degradation mechanisms in high performance multicrystalline silicon wafers.”
[38] R. Søndenå and M. S. Wiig, “Evolution of the light sensitive defects in high performance multicrystalline silicon wafers,” *J. Appl. Phys.*, vol. 125, no. 8, p. 085701, Feb. 2019.
[39] R. Haus, S. Prinz, and C. Priess, “Assessment of High Purity Quartz Resources,” in *Quartz: Deposits, Mineralogy and Analytics*, 2012, pp. 29–52.
[40] J. L. Abel, “OBTENÇÃO DO CARBONETO DE SILÍCIO PELA REDUÇÃO,” IPEN, 2009.
[41] A. SCHEI, J. TUSET, and H. TVEIT, *Production of High Silicon Alloys*. Norway: Tapir forlag, 1998.
[42] K. I. Vatalis, G. Charalambides, and N. P. Benetis, “Market of High Purity Quartz Innovative Applications,” *Procedia Econ. Financ.*, vol. 24, no. January, pp. 734–742, 2019.
[43] E. H. Myrhaug, J. K. Tuset, and and H. Tveit, “REACTION MECHANISMS OF CHARCOAL AND COKE IN THE SILICON PROCESS,” in *Tenth International Ferroalloys Congress*, 2004, no. February, pp. 108–121.
[44] A. Luque and S. Hegedus, *Handbook of Photovoltaic Science and Engineering*, vol. 36. John Wiley & Sons, Ltd, 2003.
[45] S. Ranjan, S. Balaji, R. A. Panella, and B. E. Ydstie, “Silicon solar cell production,” *Comput. Chem. Eng.*, vol. 35, no. 8, pp. 1439–1453, 2011.
[46] S. Seetharaman, S., McLean, A., Guthrie, R., & Sridhar, *Treatise on Process Metallurgy. Treatise on Process Metallurgy*. 2013.
[47] S. E. Sadique, “Production and Purification of Silicon by Magnesiothermic Reduction of Silica Fume,” University of Toronto, 2010.
[48] P. Raschman and A. Fedoročková, “Study of inhibiting effect of acid concentration on the dissolution rate of magnesium oxide during the leaching of dead-burned magnesite,” *Hydrometallurgy*, vol. 71, no. 3–4, pp. 403–412, 2004.
[49] F. Chigondo, “From Metallurgical-Grade to Solar-Grade Silicon: An Overview,” *Silicon*, vol. 10, no. 3, pp. 789–798, 2018.
[50] F. Xi *et al.*, “Simple and High-Effective Purification of Metallurgical-Grade Silicon Through Cu-Catalyzed Chemical Leaching,” *Jom*, 2018.
[51] H. Lai, L. Huang, C. Gan, P. Xing, J. Li, and X. Luo, “Enhanced acid leaching of metallurgical grade silicon in hydrofluoric acid containing hydrogen peroxide as oxidizing agent,” *Hydrometallurgy*, vol. 164, pp. 103–110, 2016.
[52] T. Wang, K. Q. Xie, W. H. Ma, Q. Liu, H. Zhang, and Y. Mai, “Comparative Study on Removal of Fe, Al and Ca From MG-Si by Acid Leaching,” *Adv. Mater. Res.*, vol. 581–582, pp. 831–835, 2012.
[53] S. K. Sahu and E. Asselin, “Effect of oxidizing agents on the hydrometallurgical purification of

metallurgical grade silicon," *Hydrometallurgy*, vol. 121–124, pp. 120–125, 2012.
[54] J. Kraiem *et al.*, "Status of the Photosil Project for the Production of Solar Grade Silicon," *Sol. Energy*, no. September, pp. 1506–1509, 2010.
[55] A. ELKEM, E. ENEBANK, K. FRIESTAD, R. TRONSTAD, C. ZAHEDI, and D. DETHLOFF, "Silicon feedstock for solar cells," 20070128099A1, 2007.
[56] M. J. de Wild-Scholten, R. Gløkner, J.-O. Odden, G. Halvorsen, and R. Tronstad, "LCA Comparison of the ELKEM Solar Metallurgical Route and Conventional Gas Routes to Solar Silicon," *23rd Eur. Photovolt. Sol. Energy Conf.*, no. September, pp. 1–5, 2008.
[57] A. F. B. Braga, S. P. Moreira, P. R. Zampieri, J. M. G. Bacchin, and P. R. Mei, "New processes for the production of solar-grade polycrystalline silicon: A review," *Sol. Energy Mater. Sol. Cells*, vol. 92, no. 4, pp. 418–424, 2008.
[58] X. Chen, S. Nakano, and K. Kakimoto, "Three-dimensional global analysis of thermal stress and dislocations in a silicon ingot during a unidirectional solidification process with a square crucible," *J. Cryst. Growth*, vol. 312, no. 22, pp. 3261–3266, 2010.
[59] L. Chen and B. Dai, "Optimization of power consumption on silicon directional solidification system by using numerical simulations," *J. Cryst. Growth*, vol. 354, no. 1, pp. 86–92, 2012.
[60] S. Riepe *et al.*, "Research on efficiency limiting defects and defect engineering in silicon solar cells - results of the German research cluster SolarFocus," *Phys. Status Solidi Curr. Top. Solid State Phys.*, vol. 8, no. 3, pp. 733–738, 2011.
[61] B. Wu, N. Stoddard, R. Ma, and R. Clark, "Bulk multicrystalline silicon growth for photovoltaic (PV) application," vol. 310, pp. 2178–2184, 2008.
[62] Y. M. Yang, A. Yu, B. Hsu, W. C. Hsu, A. Yang, and C. W. Lan, "Development of high-performance multicrystalline silicon for photovoltaic industry," *Prog. Photovoltaics Res. Appl.*, vol. 23, no. 3, pp. 340–351, Mar. 2015.
[63] I. Takahashi, N. Usami, K. Kutsukake, G. Stokkan, K. Morishita, and K. Nakajima, "Generation mechanism of dislocations during directional solidification of multicrystalline silicon using artificially designed seed," *J. Cryst. Growth*, vol. 312, no. 7, pp. 897–901, Mar. 2010.
[64] K. Kutsukake, M. Deura, Y. Ohno, and I. Yonenaga, "Characterization of silicon ingots: Mono-like versus high-performance multicrystalline," *Jpn. J. Appl. Phys.*, vol. 54, no. 8, 2015.
[65] G. Stokkan, Y. Hu, Ø. Mjøs, and M. Juel, "Study of evolution of dislocation clusters in high performance multicrystalline silicon," *Sol. Energy Mater. Sol. Cells*, pp. 1–7, 2014.
[66] T. Hiramatsu, I. Takahashi, S. Matsushima, and N. Usami, "Growth direction control of dendrite crystals in parallel direction to realize high-quality multicrystalline silicon ingot," *Jpn. J. Appl. Phys.*, vol. 55, no. 9, 2016.
[67] T. Markvart, *Solar Electricity*, vol. 21, no. 224. John Wiley & Sons, 2000.
[68] A. RICHTER, M. LANZ, C. MEYER, J. HEIBER, and R. POURTALES, "Wafering process development," *Manuf. Sol. Futur. - 2012 Prod. Annu.*, pp. 74–82, 2012.
[69] S. M. Iftiquar, Y. Lee, and M. Ju, "Fabrication of Crystalline Silicon Solar Cell with Emitter Diffusion , SiNx Surface Passivation and Screen Printing of Electrode," in *Photodiodes - From Fundamentals to Applications*, 2012.
[70] A. Bentzen and A. Holt, "Overview of phosphorus diffusion and gettering in multicrystalline silicon," *Mater. Sci. Eng. B Solid-State Mater. Adv. Technol.*, vol. 160, pp. 228–234, 2009.
[71] H. J. Choi *et al.*, "Dislocation Density Reduction During Impurity Gettering in Multicrystalline Silicon," vol. 3, no. 1, pp. 189–198, 2013.
[72] M. S. Wiig *et al.*, "Modeling of recombination strength at grain boundaries after Modeling of recombination strength at grain boundaries after phosphorus diffusion geterring and the effect of hydrogen diffusion," *Energy Procedia*, vol. 124, pp. 215–224, 2017.
[73] H. Wang, H. Yang, H. Yu, and G. Chen, "Influence of gettering and passivation on uniformity of the electrical parameters in monolithic multicrystalline silicon solar cell," *Solid State Electron*, vol. 47, pp. 1363–1367, 2003.
[74] T. Saga, "Advances in crystalline silicon solar cell technology for industrial mass production," vol. 2, no. July, pp. 96–102, 2010.
[75] A. Peral, A. Dastgheib-Shirazi, V. Fano, J. C. Jimeno, G. Hahn, and C. Del Caï¿½izo, "Impact of Extended Contact Cofiring on Multicrystalline Silicon Solar Cell Parameters," *IEEE J. Photovoltaics*, vol. 7, no. 1, pp. 91–96, 2017.
[76] "SOLAR BUZZ - SILICON," 2011. [Online]. Available: http://www.solarbuzz.com/facts-and-figures/retail-price-environment/module-prices.
[77] J. Lindroos and H. Savin, "Review of light-induced degradation in crystalline silicon solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 147, pp. 115–126, 2016.
[78] J. Nelson, *The Physics of Solar Cells*. PUBLISHED BY IMPERIAL COLLEGE PRESS AND

DISTRIBUTED BY WORLD SCIENTIFIC PUBLISHING CO., 2003.
[79] A. Cuevas and D. Macdonald, “Measuring and interpreting the lifetime of silicon wafers,” *Sol. Energy*, vol. 76, no. 1–3, pp. 255–262, 2004.
[80] O. Schultz, *High-Efficiency Multicrystalline Silicon Solar Cells*. 2005.
[81] G. Coletti, D. Macdonald, and D. Yang, “Role of Impurities in Solar Silicon,” *Adv. Silicon Mater. Photovolt. Appl.*, pp. 79–125, 2012.
[82] M. Sheoran *et al.*, “Investigation of the effect of resistivity and thickness on the performance of cast multicrystalline silicon solar cells,” in *4th World Conference on Photovoltaic Energy Conversion*, 2006, pp. 1–4.
[83] P. Engelhart *et al.*, “Influence of Base Resistivity on Solar Cell Parameters of Double-Side Contacted Rear Junction Solar Cells,” *Energy Procedia*, vol. 27, no. 3494, pp. 53–58, 2012.
[84] T. Mankad, R. a. Sinton, J. Swirhun, and A. Blum, “Inline Bulk-lifetime Prediction on as-cut Multicrystalline Silicon Wafers,” *Energy Procedia*, vol. 38, pp. 137–146, Jan. 2013.
[85] A. Metz *et al.*, “Industrial high performance crystalline silicon solar cells and modules based on rear surface passivation technology,” *Sol. Energy Mater. Sol. Cells*, vol. 120, pp. 417–425, 2013.
[86] H. J. MOLLER, C. FUNKE, A. LAWRENZ, S. RIEDEL, and M. WERNER, “Oxygen and lattice distortions in multicrystalline silicon,” *Sol. energy Mater. Sol. cells*, vol. 72, pp. 403–416, 2002.
[87] M. A. Green, *Solar cells: Operating principles, technology, and system applications*, vol. 1. University of New South Wales, 1982.
[88] R. H. Hopkins, R. G. Seidensticker, J. R. Davis, P. Rai-Choudhury, P. D. Blais, and J. R. McCormick, “Crystal growth considerations in the use of ‘solar grade’ silicon,” *J. Cryst. Growth*, vol. 42, pp. 493–498, Dec. 1977.
[89] R. H. Hopkins and A. Rohatgi, “Impurity effects in silicon for high efficiency solar cells,” *J. Cryst. Growth*, vol. 75, no. 1, pp. 67–79, 1986.
[90] A. Rohatgi, J. R. Davis, R. H. Hopkins, P. Rai-Choudhury, P. G. McMullin, and J. R. McCormick, “Effect of titanium, copper and iron on silicon solar cells,” *Solid State Electron.*, vol. 23, no. 5, pp. 415–422, 1980.
[91] S. Pizzini, “On the Effect of Impurities on the Photovoltaic Behavior of Solar Grade Silicon,” *J. Electrochem. Soc.*, vol. 133, no. 11, p. 2363, 1986.
[92] J. Degoulange, I. Périchaud, C. Trassy, and S. Martinuzzi, “Multicrystalline silicon wafers prepared from upgraded metallurgical feedstock,” *Sol. Energy Mater. Sol. Cells*, vol. 92, no. 10, pp. 1269–1273, Oct. 2008.
[93] a. a. Istratov, T. Buonassisi, and M. D. Pickett, “Control of metal impurities in ‘dirty’ multicrystalline silicon for solar cells,” *Mater. Sci. …*, vol. 134, no. 2–3, pp. 282–286, Oct. 2006.
[94] S. Binetti *et al.*, “Study of defects and impurities in multicrystalline silicon grown from metallurgical silicon feedstock,” *Mater. Sci. Eng. B*, vol. 159–160, pp. 274–277, Mar. 2009.
[95] V. Osinniy *et al.*, “Factors limiting minority carrier lifetime in solar grade silicon produced by the metallurgical route,” *Sol. Energy Mater. Sol. Cells*, vol. 95, no. 2, pp. 564–572, Feb. 2011.
[96] K. P. Jeong and Y. K. Kim, “Electrical properties of the multi-crystalline silicon ingots grown with UMG (upgraded metallurgical grade) silicon materials,” *Sol. Energy Mater. Sol. Cells*, vol. 107, pp. 201–204, Dec. 2012.
[97] P. Wagner *et al.*, “Impact of compensation on the boron and oxygen-related degradation of upgraded metallurgical-grade silicon solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 120, pp. 390–395, 2013.
[98] G. P. W. L. J. Geerligs, P. Manshanden, “Specification of solar grade silicon: how common impurities affect the cell efficiency of mc–Si solar cells,” in *20th European Photovoltaic Solar Energy Conference*, 2005, pp. 619–622.
[99] S. Dubois, O. Palais, M. Pasquinelli, S. Martinuzzi, C. Jaussaud, and N. Rondel, “Influence of iron contamination on the performances of single-crystalline silicon solar cells: Computed and experimental results,” *J. Appl. Phys.*, vol. 100, no. 2, p. 024510, 2006.
[100] S. Dubois, O. Palais, P. J. Ribeyron, N. Enjalbert, M. Pasquinelli, and S. Martinuzzi, “Effect of intentional bulk contamination with iron on multicrystalline silicon solar cell properties,” *J. Appl. Phys.*, vol. 102, no. 8, p. 083525, 2007.
[101] J. Hofstetter, J. F. Lelièvre, C. del Cañizo, and a. Luque, “Acceptable contamination levels in solar grade silicon: From feedstock to solar cell,” *Mater. Sci. Eng. B*, vol. 159–160, pp. 299–304, Mar. 2009.
[102] CRYSTAL_CLEAR, “Workshop on Arriving at Well Founded SOG Silicon Feedstock Specifications,” Amsterdam, 2008.
[103] S. Pizzini, “Towards solar grade silicon: Challenges and benefits for low cost photovoltaics,” *Sol. Energy Mater. Sol. Cells*, vol. 94, no. 9, pp. 1528–1533, Sep. 2010.

[104] G. Mount, L. Wang, K. Putyera, M. Lepage, and E. A. Group, “Characterization of Solar Grade Silicon Contaminants,” vol. 3, pp. 395–398, 2012.
[105] S. J. Hill, *Inductively Coupled Plasma Spectrometry and its Applications*. Oxford, UK: Blackwell Publishing Ltd, 2006.
[106] Y. Delannoy, “Purification of silicon for photovoltaic applications,” *J. Cryst. Growth*, vol. 360, pp. 61–67, Dec. 2012.
[107] F. Gibaja, T. Bartel, M. Heuer, O. Graf, M. Kaes, and F. Kirscht, “Silicon Ingot Quality and Resulting Solar Cell Performance,” *Energy Procedia*, vol. 38, pp. 551–560, Jan. 2013.
[108] R. A. Sinton, “Quasi-steady-state photoconductance, a new method for cell material and device characterization,” *25th PVSC*, pp. 457–460, 1996.
[109] A. Cuevas, S. Member, M. Stocks, D. Macdonald, M. Kerr, and C. Samundsett, “Recombination and Trapping in Multicrystalline Silicon,” vol. 46, no. 10, pp. 2026–2034, 1999.
[110] J. a. Giesecke, M. C. Schubert, B. Michl, F. Schindler, and W. Warta, “Minority carrier lifetime imaging of silicon wafers calibrated by quasi-steady-state photoluminescence,” *Sol. Energy Mater. Sol. Cells*, vol. 95, no. 3, pp. 1011–1018, Mar. 2011.
[111] H. Haug, R. Søndenå, M. S. Wiig, E. S. Marstein, and I. Andri, “Temperature dependent photoluminescence imaging calibrated by photoconductance measurements,” *Energy Procedia*, vol. 124, pp. 47–52, 2017.
[112] S. Y. Lim *et al.*, “Applications of photoluminescence imaging to dopant and carrier concentration measurements of silicon wafers,” *IEEE J. Photovoltaics*, vol. 3, no. 2, pp. 649–655, 2013.
[113] M. Tajima *et al.*, “Deep-level photoluminescence due to dislocations and oxygen precipitates in multicrystalline Si,” vol. 113523, 2012.
[114] T. Trupke, J. Nyhus, and J. Haunschild, “Luminescence imaging for inline characterisation in silicon photovoltaics,” *Phys. Status Solidi - Rapid Res. Lett.*, vol. 5, no. 4, pp. 131–137, 2011.
[115] F. Schindler *et al.*, “Potential gain in multicrystalline silicon solar cell efficiency by n-type doping,” *IEEE J. Photovoltaics*, vol. 5, no. 2, pp. 499–506, 2015.
[116] F. Schindler *et al.*, “Optimized multicrystalline silicon for solar cells enabling conversion efficiencies of 22 %,” *Sol. Energy Mater. Sol. Cells*, vol. 171, no. April, pp. 180–186, 2017.
[117] B. Sopori *et al.*, “Performance Limitations of mc-Si Solar Cells Caused by Defect Clusters,” in *ECS Transactions, Semicon, Shanghai, China*, 2009, pp. 1049–1058.
[118] S. Riepe *et al.*, “Correlation of Defect Luminescence and Recombination in Multicrystalline Silicon,” *IEEE J. Photovoltaics*, vol. 9, no. 1, pp. 55–63, 2018.
[119] M. Kasemann *et al.*, “Analysis of performance limiting material properties of multicrystalline silicon,” *Sol. Energy Mater. Sol. Cells*, vol. 94, no. 9, pp. 1451–1456, 2010.
[120] H. C. Sio *et al.*, “Recombination sources in p-type high performance multicrystalline silicon,” *Jpn. J. Appl. Phys.*, vol. 56, no. 8S2, p. 08MB16, 2017.
[121] K. Adamczyk *et al.*, “Recombination activity of grain boundaries in high-performance multicrystalline Si during solar cell processing,” *J. Appl. Phys.*, vol. 123, no. 5, 2018.
[122] B. J. Hallam *et al.*, “Advanced bulk defect passivation for silicon solar cells,” *IEEE J. Photovoltaics*, vol. 4, no. 1, pp. 88–95, 2014.
[123] M. C. Schubert *et al.*, “Analysis of performance limiting material properties of multicrystalline silicon,” *Sol. Energy Mater. Sol. Cells*, vol. 94, no. 9, pp. 1451–1456, Sep. 2010.
[124] S. Riepe *et al.*, “Research on efficiency limiting defects and defect engineering in silicon solar cells - results of the German research cluster SolarFocus,” *Phys. Status Solidi*, vol. 8, no. 3, pp. 733–738, Mar. 2011.
[125] S. Dubois, N. Enjalbert, and J. P. Garandet, “Effects of the compensation level on the carrier lifetime of crystalline silicon,” vol. 032114, no. 2008, pp. 2006–2009, 2008.
[126] A. Ciesla *et al.*, “Hydrogen-Induced Degradation,” in *7th World Conference on Photovoltaic Energy Conversion*, 2018, no. June.
[127] K. Petter *et al.*, “Long Term Stability of Solar Modules Made from Compensated SoG-Si or UMG-Si Solar Cells,” *Energy Procedia*, vol. 8, no. April, pp. 365–370, 2011.
[128] D. Bredemeier, D. Walter, S. Herlufsen, and J. Schmidt, “Understanding the Light-induced Lifetime Degradation and Regeneration in Multicrystalline Silicon,” *Energy Procedia*, vol. 92, no. 0, pp. 773–778, 2016.
[129] F. Kersten, J. Heitmann, and J. W. Müller, “Influence of Al2O3 and SiNx Passivation Layers on LeTID,” *Energy Procedia*, vol. 92, no. 0, pp. 828–832, 2016.
[130] B. Lim, K. Bothe, and J. Schmidt, “Deactivation of the boron – oxygen recombination center in silicon by illumination at elevated temperature pss,” vol. 95, no. 3, pp. 93–95, 2008.
[131] A. Herguth, G. Schubert, M. Kaes, and G. Hahn, “Investigations on the Long Time Behavior of the Metastable Boron – Oxygen Complex in Crystalline Silicon,” no. September 2007, pp. 135–

140, 2008.
[132] S. Wilking, C. Beckh, S. Ebert, A. Herguth, and G. Hahn, “Influence of bound hydrogen states on BO-regeneration kinetics and consequences for high-speed regeneration processes,” *Sol. Energy Mater. Sol. Cells*, vol. 131, pp. 2–8, 2014.
[133] B. Hallam *et al.*, “Modelling Kinetics of the Boron-Oxygen Defect System,” *Energy Procedia*, vol. 92, pp. 42–51, 2016.
[134] R. Søndenå and M. S. Wiig, “Evolution of the light sensitive defects in high performance multicrystalline silicon wafers,” *J. Appl. Phys.*, vol. 125, no. 8, p. 085701, 2019.
[135] K. Ramspeck *et al.*, “Light Induced Degradation of Rear Passivated mc-Si Solar Cells,” *27th Eur. Photovolt. Sol. Energy Conf. Exhib.*, vol. 27, pp. 861–865, 2012.
[136] D. N. R. Payne *et al.*, “Acceleration and mitigation of carrier-induced degradation in p-type multi-crystalline silicon,” *Phys. Status Solidi - Rapid Res. Lett.*, vol. 10, pp. 237–241, 2016.
[137] F. Fertig, K. Krau??, and S. Rein, “Light-induced degradation of PECVD aluminium oxide passivated silicon solar cells,” *Phys. Status Solidi - Rapid Res. Lett.*, vol. 9, no. 1, pp. 41–46, 2015.
[138] K. Krauss, F. Fertig, D. Menzel, and S. Rein, “Light-induced Degradation of Silicon Solar Cells with Aluminiumoxide Passivated Rear Side,” *Energy Procedia*, vol. 77, pp. 599–606, 2015.
[139] A. E. Morishige *et al.*, “Lifetime Spectroscopy Investigation of Light-Induced Degradation in p-type Multicrystalline Silicon PERC,” *IEEE J. Photovoltaics*, vol. 6, no. 6, pp. 1466–1472, 2016.
[140] D. N. R. Payne *et al.*, “Rapid passivation of carrier-induced defects in p-type multi-crystalline silicon,” *Sol. Energy Mater. Sol. Cells*, vol. 158, pp. 102–106, 2016.
[141] and G. H. Zuschlag, Annika, Daniel Skorka, “Degradation and regeneration in mc-Si after different gettering steps.”
[142] M. A. Jensen, A. E. Morishige, J. Hofstetter, D. B. Needleman, and T. Buonassisi, “Evolution of p-type LeTID defects in multicrystalline silicon during degradation and regeneration,” *IEEE J. Photovoltaics*, vol. 7, no. 4, pp. 980–987, 2017.
[143] J. M. Fritz, A. Zuschlag, D. Skorka, A. Schmid, and G. Hahn, “Temperature dependent degradation and regeneration of differently doped mc-Si materials,” *Energy Procedia*, vol. 124, pp. 718–725, Sep. 2017.
[144] H. C. Sio *et al.*, “Light and elevated temperature induced degradation in p-type and n-type cast-grown multicrystalline and mono-like silicon,” *Sol. Energy Mater. Sol. Cells*, vol. 182, no. August 2017, pp. 98–104, 2018.
[145] C. Chan *et al.*, “Modulation of Carrier-Induced Defect Kinetics in Multi-Crystalline Silicon PERC Cells Through Dark Annealing,” *Sol. RRL*, vol. 1, no. 2, p. 1600028, 2017.
[146] K. Nakayashiki *et al.*, “Engineering Solutions and Root-Cause Analysis for Light-Induced Degradation in p-Type Multicrystalline Silicon PERC Modules,” *IEEE J. Photovoltaics*, vol. 6, no. 4, pp. 860–868, 2016.
[147] P. P. Altermatt *et al.*, “High-performance p-type multicrystalline silicon (mc-Si): Its characterization and projected performance in PERC solar cells,” *Sol. Energy*, no. January, pp. 0–1, 2018.
[148] D. Sperber, A. Heilemann, A. Herguth, and G. Hahn, “Temperature and Light-Induced Changes in Bulk and Passivation Quality of Boron-Doped Float-Zone Silicon Coated with SiNx:H,” *IEEE J. Photovoltaics*, vol. 7, no. 2, pp. 463–470, 2017.
[149] D. Chen *et al.*, “Evidence of an identical firing-activated carrier-induced defect in monocrystalline and multicrystalline silicon,” *Sol. Energy Mater. Sol. Cells*, vol. 172, no. August, pp. 293–300, 2017.
[150] M. Kim, S. Wenham, V. Unsur, A. Ebong, and B. Hallam, “Impact of Rapid Firing Thermal Processes on Meta-Stable Defects: Preformation of the LeTID and the Suppression of B-O Defects,” *2018 IEEE 7th World Conf. Photovolt. Energy Conversion, WCPEC 2018 - A Jt. Conf. 45th IEEE PVSC, 28th PVSEC 34th EU PVSEC*, pp. 341–346, 2018.
[151] C. E. Chan *et al.*, “Rapid Stabilization of High-Performance Multicrystalline P-type Silicon PERC Cells,” *IEEE J. Photovoltaics*, vol. 6, no. 6, pp. 1473–1479, 2016.
[152] R. Eberle, W. Kwapil, F. Schindler, M. C. Schubert, and S. W. Glunz, “Impact of the firing temperature profile on light induced degradation of multicrystalline silicon,” *Phys. Status Solidi - Rapid Res. Lett.*, vol. 10, no. 12, pp. 861–865, 2016.
[153] D. Bredemeier, D. C. Walter, and J. Schmidt, “Possible Candidates for Impurities in mc-Si Wafers Responsible for Light-Induced Lifetime Degradation and Regeneration,” *Sol. RRL*, vol. 2, no. 1, p. 1700159, 2018.
[154] T. Luka, S. Großer, C. Hagendorf, K. Ramspeck, and M. Turek, “Intra-grain versus grain boundary degradation due to illumination and annealing behavior of multi-crystalline solar cells,”

Sol. Energy Mater. Sol. Cells, vol. 158, pp. 43–49, 2016.
[155] M. A. Jensen *et al.*, "Evaluating root cause: The distinct roles of hydrogen and firing in activating light- and elevated temperature-induced degradation," *J. Appl. Phys.*, vol. 124, no. 8, p. 085701, Aug. 2018.
[156] B. J. Hallam *et al.*, "Rapid mitigation of carrier-induced degradation in commercial silicon solar cells," *Jpn. J. Appl. Phys.*, vol. 56, p. 08MB13, 2017.
[157] C. E. Chan *et al.*, "A four-state kinetic model for the carrier-induced degradation in multicrystalline silicon: Introducing the reservoir state," *Sol. Energy Mater. Sol. Cells*, vol. 184, no. October 2017, pp. 48–56, 2018.
[158] K. Bothe and J. Schmidt, "Fast-forming boron-oxygen-related recombination center in crystalline silicon," *Appl. Phys. Lett.*, vol. 87, no. 26, p. 262108, Dec. 2005.
[159] A. Herguth and G. Hahn, "Kinetics of the boron-oxygen related defect in theory and experiment," *J. Appl. Phys.*, vol. 108, no. 11, p. 114509, Dec. 2010.
[160] T. Luka, M. Turek, C. Kranert, S. Großer, and C. Hagendorf, "Microstructural investigation of LID sensitive mc-PERC solar cells," *Energy Procedia*, vol. 124, pp. 759–766, 2017.
[161] M. Kim, D. Chen, M. Abbott, S. Wenham, and B. Hallam, "Role of hydrogen: Formation and passivation of meta-stable defects due to hydrogen in silicon," in *AIP Conference Proceedings*, 2018, p. 130010.
[162] S. Wilking, J. Engelhardt, S. Ebert, C. Beckh, A. Herguth, and G. Hahn, "High speed regeneration of bo-defects: improving long-term solar cell performance within seconds," in *29th European PV Solar Energy Conference and Exhibition*, 2014, no. September, pp. 22–26.
[163] B. J. Hallam *et al.*, "Hydrogen passivation of B-O defects in Czochralski silicon," *Energy Procedia*, vol. 38, no. Lid, pp. 561–570, 2013.
[164] D. Sperber, A. Graf, D. Skorka, A. Herguth, and G. Hahn, "Degradation of Surface Passivation on Crystalline Silicon and Its Impact on Light-Induced Degradation Experiments," *IEEE J. Photovoltaics*, vol. 7, no. 6, pp. 1627–1634, Nov. 2017.
[165] D. Chen *et al.*, "Hydrogen induced degradation : A possible mechanism for light- and elevated temperature- induced degradation in n-type silicon," *Sol. Energy Mater. Sol. Cells*, vol. 185, no. March, pp. 174–182, 2018.
[166] T. H. Fung, C. E. Chan, B. J. Hallam, D. N. R. Payne, M. D. Abbott, and S. R. Wenham, "Impact of annealing on the formation and mitigation of carrier-induced defects in multi-crystalline silicon," *Energy Procedia*, vol. 124, pp. 726–733, 2017.
[167] R. Sharma, A. P. Chong, J. B. Li, A. G. Aberle, and Y. Huang, "Role of post-metallization anneal sequence and forming gas anneal to mitigate light and elevated temperature induced degradation of multicrystalline silicon solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 195, no. August 2018, pp. 160–167, 2019.
[168] M. Yli-Koski, M. Serué, C. Modanese, H. Vahlman, and H. Savin, "Low-temperature dark anneal as pre-treatment for LeTID in multicrystalline silicon," *Sol. Energy Mater. Sol. Cells*, vol. 192, no. September 2018, pp. 134–139, 2019.

INSTITUTO DE PESQUISAS ENERGÉTICAS E NUCLEARES
Diretoria de Pesquisa, Desenvolvimento e Ensino
Av. Prof. Lineu Prestes, 2242 – Cidade Universitária CEP: 05508-000
Fone/Fax(0XX11) 3133-8908
SÃO PAULO – São Paulo – Brasil
http://www.ipen.br

O IPEN é uma Autarquia vinculada à Secretaria de Desenvolvimento, associada à Universidade de São Paulo e gerida técnica e administrativamente pela Comissão Nacional de Energia Nuclear, órgão do Ministério da Ciência, Tecnologia, Inovações e Comunicações.