

**ROBERTO RANGEL DA SILVA**

**BLUETOOTH LOW ENERGY RF FRONT-END  
FOR LOW-VOLTAGE APPLICATIONS IN CMOS  
TECHNOLOGY**

São Paulo  
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Concentration Area:

Microelectronics

Supervisor:

Prof. Dr. Wilhelmus Adrianus  
Maria Van Noije

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Orientador:

Prof. Dr. Wilhelmus Adrianus  
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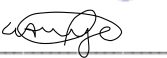
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# RESUMO

Este trabalho apresenta a análise, métodos de projeto e implementação de circuitos eletrônicos em tecnologia Metal Óxido Silício Complementar (CMOS) para operação em rádio frequências na banda industrial, científica e médica, seguindo o protocolo de comunicação Bluetooth Low Energy, para a banda de frequência de 2,4 GHz a 2,4835 GHz.

São apresentadas as motivações atuais para o trabalho com o padrão Bluetooth Low Energy, assim como os parâmetros de performance necessários para o projeto. Este protocolo oferece um conjunto de especificações mais flexíveis, ajudando na redução da tensão de alimentação e do consumo de potência.

Estão incluídas considerações sobre o trabalho com transistores de efeito de campo em Metal Óxido Silício em baixas tensões, incluindo sua operação na região de inversão fraca.

Três implementações são apresentadas, com resultados para blocos de Amplificador de Baixo Ruído e bloco conjunto Amplificador de Baixo Ruído e Misturador de Frequências. O sinal convertido a frequência intermediária é analisado, assim como a operação do Amplificador de Baixo Ruído.

Todos os projetos apresentados mostraram um consumo de potência abaixo de 1 mW, para tensão de alimentação 0,5 V e linearidade compatível com potências de entrada até -20 dBm.

**Palavras-Chave** – Microeletrônica, CMOS, Rádio Frequência, Bluetooth Low Energy.



# ABSTRACT

This work presents the analysis, design methodology and implementation of CMOS electronic circuits for operation in RF frequency, in the Industrial, Scientific and Medical (ISM) band, following the Bluetooth Low Energy communication protocol, for the frequency band of 2.4 GHz to 2.4835 GHz.

The contemporary motivation for working with Bluetooth, as well as the necessary performance parameters to be followed by the design is presented. Bluetooth Low Energy present a more flexible specification set, which helps with the reduction of supply voltage and power consumption.

The considerations on how to work with MOSFETs with low voltage are presented, including the operation with inversion levels next to weak inversion region.

Three implementations are presented, with results for LNA blocks and Front-End, which present a system with LNA and Mixer. The signal converted to an intermediate frequency is analyzed, as well as the LNA operation.

All the presented design showed power consumption below 1 mW, for 0.5 V supply and linearity compatible with input power up to -20 dBm.

**Keywords** – Microelectronics, CMOS, Radio-Frequency, Bluetooth Low Energy.

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# LIST OF ABBREVIATIONS AND ACRONYMS

<b>AC</b>	Alternated Current
<b>ADC</b>	Analog-to-Digital Converter
<b>BiCMOS</b>	Bipolar and Complementary Metal-Oxide-Semiconductor
<b>BLE</b>	Bluetooth Low Energy
<b>BR</b>	Basic Rate
<b>CMOS</b>	Complementary Metal-Oxide-Semiconductor
<b>DC</b>	Direct Current
<b>EDR</b>	Extended Data Rate
<b>FoM</b>	Figure of Merit
<b>GBW</b>	Gain-Bandwidth Product
<b>IF</b>	Intermediate Frequency
<b>IIP<sub>3</sub></b>	Input Third-Order Intermodulation Intercept-Point
<b>IM<sub>3</sub></b>	Third-Order Intermodulation Intercept-Point
<b>IoT</b>	Internet of Things
<b>IRN</b>	Input-Referred Noise
<b>LNA</b>	Low-Noise Amplifier
<b>LO</b>	Local Oscillator
<b>MiM</b>	Metal-insulator-Metal
<b>MOS</b>	Metal-Oxide-Semiconductor
<b>MOSFET</b>	Metal-Oxide-Semiconductor Field-Effect Transistor
<b>NF</b>	Noise Figure

<b>NMOS</b>	N-type Metal-Oxide-Semiconductor
<b>PDK</b>	Process Design Kit
<b>PGA</b>	Programmable Gain Amplifier
<b>PMOS</b>	P-type Metal-Oxide-Semiconductor
<b>RF</b>	Radio Frequency
<b>SNR</b>	Signal-to-Noise Ratio
<b>THD</b>	Total Harmonic Distortion
<b>ULP</b>	Ultra Low Power
<b>ULV</b>	Ultra Low Voltage

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# 1 INTRODUCTION

This chapter presents the motivation and objectives of this work, including discussions on the issues regarding the reduction of power consumption and supply voltage in the design of integrated circuits for radio-frequency (RF) communication systems using CMOS technology, focusing on RF Front-End circuits for wireless receivers using the Bluetooth Low Energy (BLE) standard, and operating at Ultra Low Voltage (ULV) and Ultra Low Power (ULP).

## 1.1 Motivation

The current advancements on the development of ubiquitous systems with network capabilities contribute on the solution for open problems in the society. Such systems, often categorized as Internet of Things (IoT) rely on the network connection among its peers, which enables the information sharing. It can be applied to monitoring and actuating activities [2, 3]. One of the benefiting areas is that involving Wireless Body Area Networks (WBAN), including wearable, implanted and hand-held devices which can be applied to consumer, health care or productivity solutions [2–6].

Since IoT nodes often have restricted access to power supply, usually depending on battery power, they demand advances on system design towards power consumption minimization. In addition to simply reducing static current by changing to less consuming circuit topologies, the battery life can also be extended by operating at low supply voltages.

The two approaches can be combined, leading to a larger minimization of power consumption, and applying Ultra Low Voltage (ULV) and Ultra Low Power (ULP) solutions. Reported works suggest that ULV and ULP currently stand for supply voltages under 1.0 V and RF receiver power consumption under 3.0 mW [7–9].

The reduction of the supply voltage also allows working with energy harvesting

sources, such as solar cells, without the need for additional voltage level shifters [9–11].

Moreover, supply voltage reduction becomes mandatory along with the scaling of CMOS technologies, reaching maximum values near 0.5 V for thin-oxide MOSFETs in nodes below 22nm [12]. Operating at low supply voltages also reduces quadratically the dynamic power consumption of digital circuits [12–14].

The circuit blocks included in the wireless radio-frequency (RF) transceiver are often the most power consuming part of IoT devices [15]. Moreover, among the circuits comprising the wireless receiver, the majority of power consumption lies in the circuits of the RF Front-End, responsible for the interface with the signal source, such as an antenna.

The most prospective network protocols implementing WBAN systems nowadays are ZigBee, Bluetooth and Wi-Fi. They have been applied in many solutions through the last years, proving to be solid solutions [4, 16]. The Bluetooth standard has been broadly available in mobile phones, peripherals and other devices, contributing for its growing popularity. Recently, the Bluetooth Low Energy standard have been adopted due to the low consumption and high availability among the existing devices [17]. Bluetooth Basic Rate (BR) mode designs have been reported and introduced considerable power reduction comparing to other network protocols available at the time of its release [18–21].

Since its version 4.0, Bluetooth protocol includes the Bluetooth Low Energy (BLE), also called Bluetooth Smart, standard. BLE has relaxed specifications constraints on noise requirement and on sensitivity comparing to basic rate Bluetooth operating mode, thus enabling reduced power consumption and area applications, on the expense of range and data rate [1, 22].

At this moment CMOS technology is known to be the most used for the development of large scale electronics solutions, fitting the demands of most IoT systems. CMOS has the advantage of being capable of operating in radio-frequency range, performing the demanded operation in the ISM band, near 2.4 GHz, and being able to integrate communication and signal processing circuits with low area and power consumption.

This work is focused on study of the implementation of the RF Front-End blocks, including the issues and possible solutions that allow ULV and ULP operation following the BLE standard. The implementation involves the theory analysis, topology choice, simulation, layout, fabrication and testing using conventional CMOS process. Moreover, this work allow to extend the research conducted by previous works in the "Divisão de Metodologias de Projetos e Sistemas VLSI" (DMPSV) group at the University of Sao Paulo [21, 23, 24].

## 1.2 Objectives

This work aims at designing the blocks comprising the RF Front-End of a wireless receiver, including a Low-Noise Amplifier (LNA) and a downconversion Mixer circuits for CMOS technology.

The design follows the performance specifications of the Bluetooth Low energy protocol, evaluating the results with schematic and post-layout simulations, as well as experimental results, when available. Moreover, the circuits are required to operate at Ultra Low Voltage and Ultra Low Power, using the power consumption minimization as the main factor for topology choice and design strategies. Based on the presented analysis on the mandatory supply voltage reduction following CMOS technology scaling, and the benefits for power consumption reduction and energy harvesting applications, this work proposes a supply voltage of 0.5 V for the designed circuits.

The design strategies formulation, topology choices, circuit analysis, schematic simulations, physical layout and post-layout simulations are also realized.

Following the circuits' design and adjustments after post-layout simulations, this work comprises the fabrication of the integrated circuits using CMOS technology.

After Fabrication, it is included the design of test boards to interface the fabricated chips with the test equipment.

Finally, experimental and post-layout results are compared to desired performance parameters and suggestions are made for improvements and future works.

## 1.3 Bluetooth Low Energy Standard

Currently in its 5.0 version, Bluetooth core specification includes Bluetooth Low Energy (BLE) operation mode since its version 4.0 [1]. BLE changes the sensitivity, noise tolerance and adjacent channel rejection specifications toward enabling the operation with less power consumption. Table 1 shows a comparison among BLE, Bluetooth v5.0 (BT5), basic rate (BR) and extended data rate (EDR) Bluetooth operation modes, highlighting the more spaced spectrum of BLE, allowing a less restrict design. As presented, BLE, BT5 and BR modes implement Gaussian Frequency Shift Keying (GFSK) modulation, and EDR mode implements Differential Quadrature Phase Shift Keying (DQPSK) or 8-Phase Differential Phase Shift Keying (8DPSK) [1, 22].



Table 1: Bluetooth standard operation modes.

	BLE	BT5	BR	EDR
Modulation	GFSK	GFSK	GFSK	DQPSK / 8DPSK
Data Rate	1 Mbps	2 Mbps	1 Mbps	2 or 3 Mbps
Channels	40	40	79	79
Spacing	2 MHz	2 MHz	1 MHz	1 MHz

BLE devices operate under the unlicensed 2.4 GHz ISM band. BLE uses a binary frequency modulation, with pulse shaping and data transmission rate down to 1 Msymbol/s, using 1 bit/symbol modulation, giving 1 Mbit/s data rate. It works with 2MHz channel band, using 1MHz for payload and 0.5MHz guard band between payload and adjacent channels. From 2402 MHz to 2483.5 MHz, 40 channels are possible. Channel frequencies receive values of  $2400 + 2 \times k$  MHz, being  $k$  an integer number from 1 to 40 [1, 22].

The receiver requires a -70dBm minimum and 0dBm maximum sensitivity. Signal is modulated using gaussian frequency shift keying (GFSK), combining frequency modulation with pulse shaping using gaussian filters. It is very similar to minimum shift keying modulation, but with variations in the modulation index. To avoid signal interference, it performs frequency hopping spread spectrum (FHSS) techniques, which keeps changing the operating channel for periods determined by the link creation.

Table 2 summarizes the performance specifications regarding Bluetooth Low Energy operation mode, as reported by [1], which will serve as design constraints towards this work.

Based on the required adjacent channel interference, at the maximum usable input level of 0 dBm, the compression point  $P_1dB$  is set at -15 dBm, and hence the IIP3 at -5 dBm.

The sensitivity performance is directly related to the maximum noise figure (NF) contribution allowed in the receiver. Following the analysis reported in [25, 26], an expression can be derived to obtain the maximum NF.

$$NF_{dB} = S_{in} + IL - N_s - SNR_{out,min} \quad (1.1)$$

where NF is the maximum noise figure for the receiver,  $S_{in}$  is the sensitivity, or the minimum detectable input signal level;  $IL$  is the input insertion loss;  $N_s = 10\log(kTB)$  is the in-band noise source, including the Boltzmann constant  $k$ , signal bandwidth  $B$  and

the absolute temperature  $T$ , in kelvin;  $SNR_{out,min}$  is the minimum Signal-to-Noise (SNR) for the receiver output required by the demodulator to identify the information with the specified Bit-Error Rate (BER).

For the noise figure calculation, the value for the input sensitivity  $S_{in}$  is considered to be 10 dBm lower than the one in table 2, to add a safety margin. The signal bandwidth  $B$  is 1 MHz, an insertion loss of 2 dB is considered at the LNA input, as often an external band filter is used, having this typical level of insertion loss [25]. The minimum SNR is derived from the demodulator BER, where an optimal value of 12 dB is assumed [25].

Using the chosen values with equation 1.1, a maximum NF value of 20 dB is found. This value will be considered for the further design on this work.

Table 2: Bluetooth Low Energy main performance parameters [1].

Parameter	Value
Frequency Band	2400 - 2483.5 MHz
Channel length	2 MHz
Signal bandwidth	1 MHz
Sensitivity	-70 dBm
Adjacent Channel Interference	-17 dB
BER	0.1%
Data rate	1 Mbps

## 1.4 Wireless Receiver Architecture for BLE

This work focus on the design of blocks in the physical (PHY) layer of bluetooth low energy protocol. Thus, the study of radio physical architectures is necessary. The following study is based on the analyses suggested by [26–30].

The signal at the input of the wireless receiver contains the original information, sent by an external transmitter, modulated around a carrier signal. The original signal have a bandwidth  $f_b$ , where  $f_b \ll f_c$ , being  $f_c$  the frequency of the carrier signal.

The modulation results in a RF signal having a frequency spectrum with bandwidth  $f_b$  centered at  $f_c$ . Hence, the receiver needs to translate the RF signal back to the original frequency characteristics before the information processing.

The frequency translation is performed by the RF Front-End block, which lies in the beginning of the receiver path, and is composed by a Low-Noise Amplifier (LNA) and a

downconversion Mixer [26, 27].

The LNA is responsible for the interface with the signal source, often an antenna, being the first stage of the receiver. Its noise contribution is the most critical for the overall noise figure of the receiver, as it is entirely added to the receiver's noise figure [26, 31]. Its input matching is responsible for achieving maximum power transfer of the input signal. Also, its gain attenuates the noise contribution of the subsequent stages, justifying the low noise and high gain characteristic of its design [26].

The downconversion Mixer is responsible for the translation of the RF signal centered at the carrier frequency to a lower frequency. Depending on the receiver architecture, the lower center frequency may be zero, or rather an intermediate frequency (IF).

A zero center frequency characterizes a direct-conversion, or Zero-IF receiver. Whereas the presence of an IF characterizes an indirect-conversion receiver. The later is distinguished by the IF value, being called Low-IF receiver for an IF near zero, or High-IF for higher values.

Some receivers implement more than one conversion steps, describing a Sliding-IF architecture.

The value of IF is determined by the frequency generated at a Local Oscillator (LO), where  $f_{IF} = f_{RF} - f_{LO}$ , where  $f_{RF}$  is the modulated input signal frequency. For Zero-IF receivers,  $f_{LO} = f_{RF}$ .

This work contemplate the adoption of a Low-IF receiver, taking into account the benefit of avoiding DC offset and flicker noise [7, 10, 32] influence in the DC spectrum [8, 9, 11, 33–36].

Some works employ a Sliding-IF receiver, seeking to have a more relaxed LO design [5, 6, 17, 37, 38]. However, this approach increases the number of stages in the receiver, contributing to power consumption.

Figure 1 shows the architecture of a Low-IF receiver, including the LNA, quadrature downconversion Mixer, polyphase filters, Programmable Gain Amplifiers (PGA) and Analog-to-Digital converters (ADC).

The quadrature downconversion is performed in conjunction with polyphase filtering as a way to realize image rejection on the resulting IF signal [26, 39]. To perform the quadrature downconversion, the LO generates two outputs with  $90^\circ$  phase separation between the In-Phase (I) and In-Quadrature (Q) IF paths.

After the polyphase filter, the signal voltage level is adjusted by the PGA, and finally converted to digital domain by the ADC.

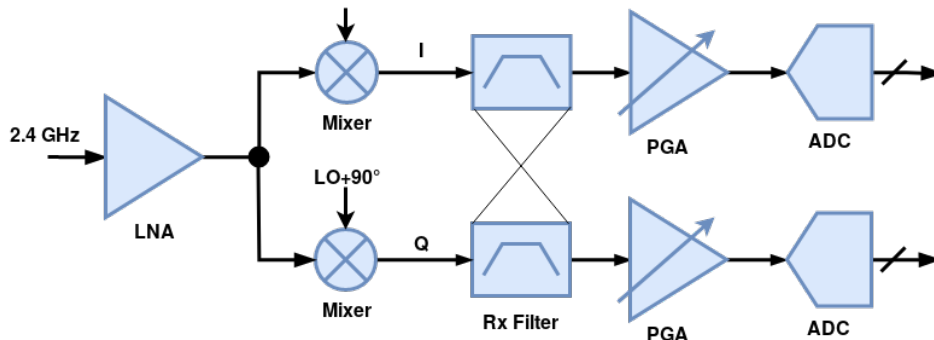


Figure 1: Receiver system considered for this work, with RF Front-End implementing a Low-IF quadrature downconversion.

Source: Author

## 1.5 State of The Art

Table 3 shows a summary of recently published works, which contribute to observe reportedly State-of-The-Art performance results. The work selection criteria seek to match with the objectives of this work, intending to contribute with suitable comparison references. Moreover, they serve to show the tendency for topology choice and design approaches.

The performance parameters reported are the technology node, power consumption, supply voltage, receiver type, sensitivity, noise figure (NF), integrated area, and power consumed by the Front-End (FE) circuit.

It is worthwhile to analyze the type of receiver architecture implemented, the factors that justify the choice of the topologies for the LNA and Mixer circuits, as well as design considerations, and the further effect on the system's performance. It can be observed that all works include either direct-conversion (Zero-IF) or Low-IF receivers, avoiding the implementation of heterodyne architectures. Thus, they avoid the requirement for off-chip image rejection filters, and also reduce the number of stages in the receiver path [26, 33].

Most implementations cited on table 3 were performed using sub-micron technology nodes, except [33]'s, whose design choice was for a 130nm technology, coping with the reduction of fabrication costs. That is a remarkable choice, since consumer Internet of

Things applications also often include requirements for production cost reduction, turning into an interesting choice, provided that the performance requirements are sustained.

The results show that the designs exploit the relaxed noise figure requirements of the BLE standard, showing considerably high NF values, compared to BR/EDR Bluetooth [1] or other more restrained standards, whose NF is often below 3 dB [26, 27]. The relaxed noise response characteristics contribute to lower power consumption.

Table 3: Reported State-of-The-Art BLE receiver implementations

Parameter	EDSSC 19 [11]	ISSCC 18 [7]	ISSCC 18 [8]	TMTT 18 [33]	JSSC 18 [9]
Technology (nm)	55	40	65	130	28
Power (mW)	20.4	2.3	2.3	1.69	0.38
Supply (V)	3	0.8	1	1.2	0.18
Receiver Type	Low-IF	Zero-IF	Low-IF	Low-IF	Low-IF
Sensitivity (dBm)	-95	-95	-94	-92	-
NF (dB)	-	5.9	6	7.2	11.3
Area ( $mm^2$ )	-	0.8	1.64	0.7	1.65
FE Power (mW)	-	0.69	0.7	0.76	0.13

A full System-on-Chip is included in [11]’s implementation with focus on consumer applications, including digital processing, modem and link manager blocks besides the physical layer. It claims a reduction on production costs, as it includes in-chip the necessary memory structures, thus reducing the cost with off-chip materials on a further product application. The sensitivity requirement for the protocol is extended, with a -95 dBm limit, yet having less attractive performance results than the other works regarding power consumption and supply voltage. It implements a low-IF receiver, with RF Front-End including a cascode common-source LNA with inductive source degeneration.

In [7], the receiver works with zero-IF downconversion, and uses a phase-tracking architecture, where an all-digital phase-locked-loop (ADPLL) replace the analog-to-digital converter (ADC) and allows using a single signal path, instead of quadrature downconversion, thus saving power. The RF Front-End is composed by a single-ended, inverter-based LNA, and a single-balanced, current-driven passive mixer. The use of a low supply voltage of 0.8 V also contributes for the power reduction. The choices lead this design to a very reduced power consumption, with low noise figure and chip area.

In [8], a low-IF receiver was chosen for its advantages in low power implementations, reportedly achieving attractive in-band and out-band blocker performance. It uses

an ADPLL centric receiver, as in [7], with RF Front-End composed by a single-ended common-source LNA with inductive source degeneration, integrated balun to modify the signal path to differential, and a double-balanced current-driven passive mixer.

The implementation in [33] exploits the BLE standard frequency requirements to improve power reduction by choosing an IF value of 1 MHz. Since the BLE channels have 1 MHz of signal space and 1 MHz of spacing, using 1 MHz IF avoid the necessity of a band-pass filter, as usual in low-IF receivers, using a low-pass filter instead. The RF Front-End is composed by an inverter-based LNA, whose topology is based on [40]. Modifications are made to reduce power consumption without compromise the noise figure and gain response.

The lowest RF Front-End power consumption is found in [9], where a massive reduction on the supply voltage is performed, reaching 0.18 V. The Front-End includes a two-stage power gating LNA with a common-source inductive degenerated source topology, using a transformer coupling between source and gate in order to implement input matching, and passive gain boosting. It reportedly reduced the DC current on the LNA's first stage after including the transformer.

The observed characteristics on the art presented in this chapter will serve as a strong reference during the design choices of this work, guiding the choice of topologies and design strategies adopted.

## 1.6 Organization of this document

In chapter 1 the motivation and specification of the problem proposed by this work was presented. Moreover, a study on the state-of-the-art reported works including the design of RF Front-End systems for BLE receivers was conducted, contributing with references for the design of Low-Noise Amplifiers, downconversion Mixers and RF Front-Ends including them.

Chapter 2 realizes an theoretical analysis on the Low-Noise Amplifier, Mixer and RF Front-End blocks, allowing the formulation of the mathematical equations that relate circuit parameters and performance specifications. The equations obtained are the foundation for the topology choices and the development of the design strategy.

Chapter 3 describes the design of the Low-Noise Amplifier, Mixer and RF Front-End using conventional CMOS technologies, presenting their circuit sizing, schematic simulation results, physical layout, post-layout simulation results, fabrication results, test

boards design, measurement procedures and experimental results.

Finally, in chapter 4 the experimental results are discussed and compared with post-layout simulations and design performance objectives tables, verifying how close in the final results to the desirable performance. Also, recommendations for future works are stated, based on the flaws and success of this work.

## 2 LNA AND MIXER LOW-VOLTAGE DESIGN METHODOLOGY

This chapter presents the theoretical bases for the RF Front-End, Low-Noise Amplifier (LNA) and Mixer circuits analysis and design. The presented theory will guide the topology choice and formulation of equations describing the relation between the performance specifications and the circuit parameters. In the implementation chapter of this work, the equations gathered will be applied to CMOS technology parameters, to verify the feasibility of the proposed circuit, as well as finding the initial circuit sizing.

The proposed supply voltage of 0.5 V imposes restrictions on the topology choices. The main guideline is the choice of circuits with no more than two stacked transistors, thus allowing sufficient voltage headroom to maintain the devices operating in saturation region [12].

To help in the reduction of power consumption, the topology choices will try to minimize the number of circuit stages consuming static current.

### 2.1 Low-Noise Amplifier

The previous chapter introduced the LNA as an important block for the overall noise figure level on the receiver, and also for performing the proper input matching with the off-chip signal source. Implementations lacking a LNA block, with rather simpler input matching and direct downconversion of the received signal exist [10], yet resulting in a substantial increment in the system's noise figure.

Considering those attributes, the following analysis present the topology choice, and formulation of input and output impedances, noise, gain, linearity and stability relations. Moreover, a design procedure based on the gathered formulations is presented.



### 2.1.1 Topology choice

To minimize noise contribution, LNAs usually employ a minimal number of devices and stages, often been implemented as an one-stage amplifier [27]. The circuits can be implemented as differential or non-differential input. Differential input is required when the common-mode noise reduction is critical, but as it contributes with more power and noise, due to the components being doubled, it is not considered when common-mode noise requirements are moderate. Also, differential amplifiers need a balun to interface with the antenna, adding extra external components.

As suggested by [12, 21, 26], the cascode common-source amplifier with inductive de-generation topology, shown in Figure 2, is preferred for optimal noise reduction and yet a satisfactory gain. Also, several recent reported works for BLE support the choice of this topology for ULP design [5, 11, 35, 37, 38, 41, 42]. In [12], the analysis is extended for the case of ULV design, observing that this type of topology is still feasible towards 0.5 V supply voltage ( $V_{DD}$ ). However, the design procedure has to be adapted, being aware of the low overdrive voltage ( $V_{OV}$ ). As a consequence of the massive  $V_{DD}$  reduction relative to the  $V_{TH}$ ,  $V_{OV}$  may reach values below 100 mV, driving the MOSFET channel inversion level towards weak inversion, hardly maintaining moderate inversion conditions [12]. This condition is distinct to the usual operation of LNAs supplied with nominal  $V_{DD}$ , often operating at moderate to strong inversion [27].

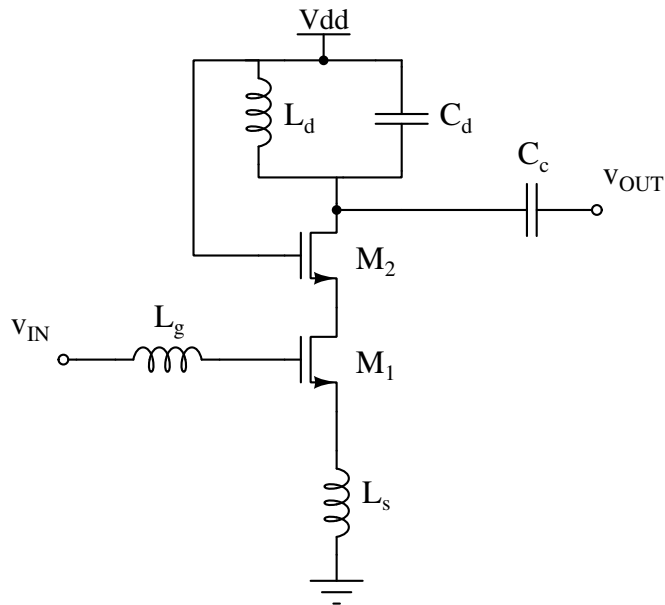


Figure 2: Cascode common-source LNA with inductive source degeneration and LC load.

Source: Author

Despite the advantages of the presented topology, inverter-based topologies are also found among recent ULP implementations, thriving for better operating conditions in ULV conditions [7, 33, 40, 43]. Albeit being a better choice for biasing in ULV condition, the inverter-based topologies show a large bandwidth frequency response compared to the cascode common-source presented. The LC tank, comprising inductor  $L_d$  and capacitor  $C_d$  shown in Figure 2, result in a narrow bandwidth response, contributing to filter out-of-band blockers [26]. The narrow bandwidth LNAs are a better choice, as filtering out-of-band blockers supports the alleviation of band filtering in the subsequent stages, reducing power consumption.

The use of a cascode configuration instead of a simple common-source is due to reverse isolation. In the cascode common-source, the path from the output node,  $v_{OUT}$  to the input node,  $v_{IN}$  is isolated by the impedance composed by the  $M_2$  drain to source capacitance,  $C_{ds,2}$ , drain to source resistance  $R_{ds,2}$ , and the gate to drain capacitance from  $M_1$ ,  $C_{gd,1}$ , hence showing a larger isolation than only  $C_{gd,1}$ , as found in the simple common-source [44]. The capacitance  $C_c$  realizes the coupling with  $v_{OUT}$ , filtering the DC voltage from  $M_2$  drain terminal.

## 2.1.2 Input Matching

The design of the LNA must ensure a proper input matching with the source impedance, assuring the maximum power transfer [26]. Figure 3 shows the small-signal model of the transistor  $M_1$ , from Figure 2. In the model, the drain connections are omitted, highlighting the characteristics of the input interface, at the gate node G. The input signal is represented by the voltage source  $v_s$ , having a impedance  $Z_s$ . For maximum power transfer, and avoiding signal reflection, the input impedance of the LNA,  $Z_{in}$ , must be equal to  $Z_s$  [26].

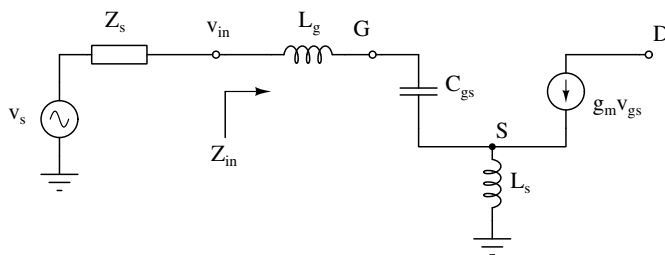


Figure 3: Small-signal model of the transistor  $M_1$ , showing the input interface at gate terminal.

Source: Author

The expression for the input impedance  $Z_{in}$  is shown in Equation 2.1, where the capacitance seen at the gate of  $M_1$  is approximately  $C_{gs}$ , the capacitance from gate to source terminals.

The presence of the inductors  $L_g$  and  $L_s$  result in an impedance with real and imaginary part, giving the necessary means to control the input matching.

$$Z_{in} = j \left[ \omega(L_g + L_s) - \frac{1}{\omega C_{gs}} \right] + \frac{g_{m1}}{C_{gs}} L_s \quad (2.1)$$

where  $\omega$  is the angular frequency at which the impedance is calculated;  $g_{m1}$  and  $C_{gs}$  are the transconductance and gate to source capacitance of the transistor  $M_1$ , respectively.

In wireless systems such as BLE, the input terminal of the LNA is often connected to an antenna having an impedance of  $50 \Omega$  [26]. To design a input matching resulting in  $Z_{in} = 50 \Omega$ , its imaginary part,  $Im \{Z_{in}\}$ , must be zero, and its real part,  $Re \{Z_{in}\}$  must be  $50 \Omega$ .

The real part of  $Z_{in}$  can be calculated to make  $\frac{g_{m1}}{C_{gs}}L_s = 50$ . And the imaginary part reduced to zero, with  $\omega(L_g + L_s) = \frac{1}{\omega C_{gs}}$ .

### 2.1.3 Output Matching

The analysis of the output matching is performed at the load connection, which considering the circuit in Figure 2 is made at the drain of the cascode device,  $M_2$ . Unlike the input impedance, that has to match with the antenna's  $50 \Omega$  impedance, the impedance from the load of the LNA,  $Z_L$ , often has a large real value. Hence, the matching of the output impedance from the LNA,  $Z_{out}$ , and  $Z_L$  is not focused on maximum power transfer. The impedance  $Z_{out}$  is adjusted so that the resulting impedance,  $Z_{out}||Z_L$ , has a resonance frequency,  $\omega_c$ , at the center of the BLE frequency band,  $\omega_c = 2\pi \times 2.44 \times 10^9 \text{ rad/s}$ .

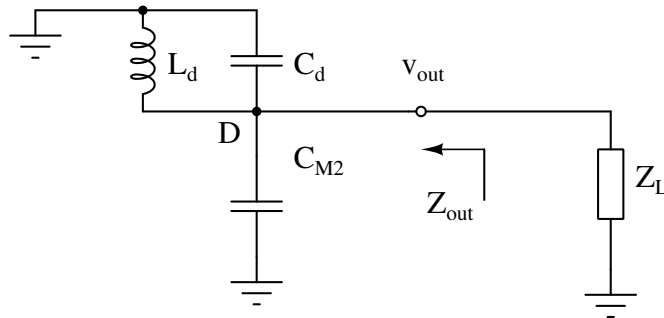


Figure 4: Small-signal model showing the load connection at the drain terminal of the transistor  $M_2$ .

Source: Author

Equations 2.2 and 2.3 show the procedure for calculating a  $C_d$  value resulting in the desired tuning of the LC load at  $\omega_c$ . In the equations,  $C_{eq}$  represents the equivalent capacitance from the parallel connection between the capacitance seen at  $M_2$  drain, represented by  $C_{M2}$ , and the capacitance from  $Z_L$ .

$$\omega_c^2 = \frac{1}{L_d \frac{C_d C_{eq}}{C_d + C_{eq}}} \quad (2.2)$$

$$C_d = \frac{1}{\omega_c^2 L_d - 1/C_{eq}} \quad (2.3)$$

where  $\omega_c$  is the required tuning frequency for the LC load;  $L_d$  and  $C_d$  are the inductor

and capacitor from the LC tank of Figure 2, respectively;  $C_{M_2}$  represent the capacitances seen at the drain terminal of  $M_2$ ; And  $Z_L$  represent the input impedance of the subsequent stage.

### 2.1.4 Noise

The analysis presented in [26, 44] suggest that the noise in the amplifier seen in figure 2 is dominated by the noise source at the channel of  $M_1$ , the input MOSFET. It is proved that the noise at  $M_2$  channel have a high-pass characteristic, being negligible for the frequency range of interest in this work. If the noise from the drain inductor,  $L_d$ , is concerned, the analysis can be approximated to that of an cascode common-source amplifier with resistive load, where the noise is also dominated by the  $M_1$  channel. Therefore the analysis is performed considering the noise sources in  $M_1$ .

Figure 5 shows the small-signal model for the transistor  $M_1$ , including the noise source representing the noise generated by the source impedance,  $\overline{v_{n,s}^2}$ , the noise current at  $M_1$  gate,  $\overline{i_{n,g}^2}$ , and the noise current at  $M_1$  drain,  $\overline{i_{n,d}^2}$ .

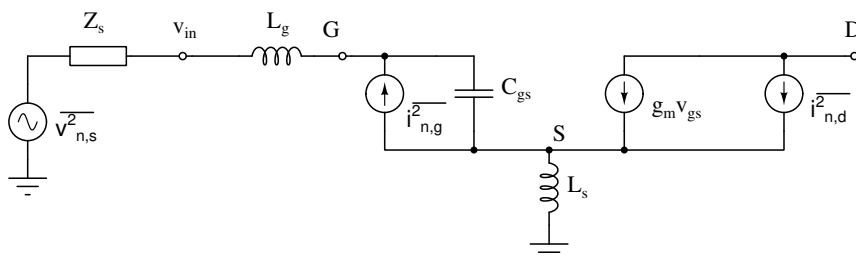


Figure 5: Small-signal model showing the the noise sources at the terminals of  $M_1$ .

Source: Author

The noise performance of the LNA is usually quantified using the Input Referred Noise (IRN) or the Noise Figure (NF). The IRN measures the noise contributed by a circuit referred to its input, as if the circuit was a noiseless block with IRN noise source as input. The NF is the ratio of the input to the output SNR, as shown in Equation 2.4. It indicates the ratio of noise magnitude in the output to the input, and is a more used parameters, as it is measurable [26].

$$NF = \frac{SNR_{in}}{SNR_{out}} = \frac{\overline{V_{n,out}^2}}{\overline{V_{n,in}^2}} \quad (2.4)$$

where NF is the LNA noise figure;  $SNR_{in}$  and  $SNR_{out}$  the signal-to-noise ratio of the input and output signals, respectively;  $\overline{V_{n,in}^2}$  and  $\overline{V_{n,out}^2}$  are the mean square noise voltage at the input and output of the LNA, respectively.

The NF can also be defined as the ratio of the total noise at the output to the noise at the output due to the source impedance [26]. Equation 2.5 shows this relation, where  $\overline{V_{n,R_s}^2}|\alpha|^2 A_v^2$  stands for the output noise due to source impedance. The noise contributed by the noise source at the gate is negligible [26] and will be omitted in this simplified calculation.

$$NF = \frac{\overline{V_{n,R_s}^2}|\alpha|^2 A_v^2 + \overline{V_{n,out}^2}}{\overline{V_{n,R_s}^2}|\alpha|^2 A_v^2} \quad (2.5)$$

where  $\alpha$  is the input attenuation factor,  $\alpha = \frac{Z_{in}}{Z_{in}+Z_s}$ ;  $A_v$  the small-signal gain of the LNA, and  $\overline{V_{n,R_s}^2}$  the mean square noise voltage from the source resistance  $R_s$ .

If an ideal match condition is considered, the factor  $|\alpha|$  equals 0.5, then  $|\alpha|^2 = 1/4$ . Moreover, the noise from source resistance,  $\overline{V_{n,R_s}^2} = 4kTR_s$ . Equation 2.6 shows the equations with these considerations, where  $k$  stands for the Boltzmann constant and  $T$  the temperature.

$$NF_{match} = \frac{\overline{V_{n,R_s}^2} A_v^2 + 4\overline{V_{n,out}^2}}{\overline{V_{n,R_s}^2} A_v^2} = 1 + \frac{\overline{V_{n,out}^2}}{kTR_s A_v^2} \quad (2.6)$$

where  $NF_{match}$  is the noise figure of the LNA for an optimal match between the source resistance and LNA input impedance;  $k$  is the Boltzmann constant; And  $T$  the absolute temperature in Kelvin.

From [26], the noise current at  $M_1$  channel can be described as  $\overline{I_{n,d}^2} = 4kT\gamma g_{m1}$ , where  $\gamma$  is the "noise excess coefficient" [26], and  $g_{m1}$  the transconductance of  $M_1$ . Thus, the noise at the output node can be represented as  $\overline{V_{n,out}^2} = \overline{I_{n,d}^2} \times r_o^2$ , where  $r_o$  is the channel resistance for the MOSFET operating in saturation region. The intrinsic voltage gain can be calculated as  $A_V = g_m r_o$  [44].

Equation 2.7 shows the resulting approximation of the noise figure. It allows to observe the relations between each circuit parameter and the NF, enabling a noise aware design procedure.

$$NF_{match} \approx 1 + \frac{4\gamma}{g_{m1} R_s} \quad (2.7)$$

where  $\gamma$  is the "noise excess coefficient" [26]; And  $g_{m1}$  the input MOSFET  $M_1$  transconductance.

Equation 2.7 reveals a dominance and inverse relation of  $M_1$  transconductance,  $g_{m1}$ , to noise figure. As the transconductance is directly proportional to the bias current, lower noise figure values would require higher power consumption.

### 2.1.5 Gain

The integrated inductors are not ideal, hence showing series resistance associated with the inductance. This resistance can be related to the quality factor (Q) of the inductor, which measures the ratio between the imaginary and real parts of the component impedance, related to inductive reactance and the parasitic resistance, respectively. The quality factor for a series parasitic resistance is described in equation 2.8, from [26].

$$Q_s = \frac{\omega L}{R_s} \quad (2.8)$$

where  $Q_s$  is the quality factor for a series connected parasitic resistance;  $\omega$  the operating angular frequency in rad/s; L the inductance;  $R_s$  the equivalent parasitic series resistance.

Ideally, for signals in frequencies near the resonating frequency,  $\omega_c$ , of LNA's LC tank load, formed by  $L_d$  and  $C_d$ , the tank behaves as an open circuit, and the current from  $M_1$  drain flows directly to  $v_{OUT}$ . However, in a real situation, the parasitic resistance results in a lower load impedance at the resonating frequency. To better analyze this effect, a series to parallel equivalence is performed, to describe the parasitic resistance as a parallel element,  $R_p$  [26]. Figure 6 shows the LNA circuit and the parasitic resistance  $R_p$  parallel to the LC tank at the load.

The quality factor for the parallel resistance is described in Equation 2.9, from [26].

$$Q_p = \frac{R_p}{\omega L} \quad (2.9)$$

where  $Q_p$  is the quality factor for a parallel connected parasitic resistance;  $\omega$  the operating angular frequency in rad/s; L the inductance;  $R_p$  the equivalent parasitic parallel resistance.

If the quality factor  $Q_p$  is known, the parallel resistance value can be estimated and used for further voltage gain calculation. Using the relation in Equation 2.9,  $R_p = \omega L_d Q_p$ .

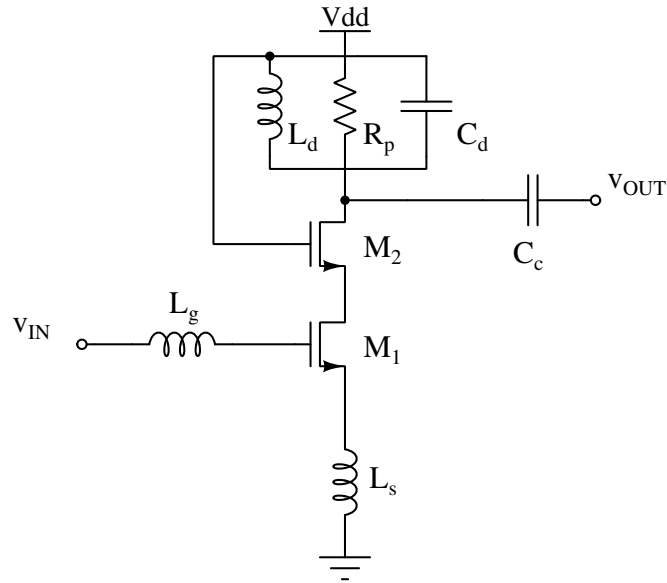


Figure 6: Cascode common-source LNA with inductive source degeneration, including equivalent parallel resistance from load inductor parasitics.

Source: Author

The voltage gain can be obtained using the relation  $A_v = -G_m R_{out}$ , using two-port analysis [44], where  $G_m$  is the total transconductance of the circuit, and  $R_{out}$  its output impedance. If the channel resistance of  $M_1$  is neglected,  $G_m = g_{m1} Q_{in}$ , where  $Q_{in}$  is the input quality factor  $1/(Z_{in} \omega C_{GS})$ . Equation 2.10 shows the resulting expression for the LNA in figure 6.

$$A_v = G_m (R_p || g_{m2} r_{o1} r_{o2}) \approx G_m R_p = g_{m1} Q_{in} \omega L_d Q_p \quad (2.10)$$

where  $A_v$  is the LNA voltage gain;  $G_m$  its total transconductance;  $g_{m1}$  and  $g_{m2}$  the transconductance from  $M_1$  and  $M_2$ , respectively;  $r_{o1}$  and  $r_{o2}$  the channel resistance from  $M_1$  and  $M_2$ , respectively.

The resulting gain expression shows a direct relation with  $g_{m1}$ ,  $L_d$  and  $Q_p$ . Therefore, to obtain high gain with low power consumption, the inductor have to be designed to have a high Q, and high inductance, thus avoiding increments in  $g_{m1}$ .



### 2.1.6 Linearity

The linearity analysis of the LNA is performed by applying a two-tone test, allowing to observe intermodulation and gain compression effects. The test involves applying two tones with equal magnitude at the LNA input, and measuring the resulting intermodulated signal at the output. Varying the input magnitude, it is observed a higher increment in the third-order component of the signal, characterized by the coefficient  $\alpha_3$ , than in the first-order one, characterized by the coefficient  $\alpha_1$ . Thus, the point of convergence between the first and third order responses is calculated as the Third-Order Intermodulation Intercept-Point ( $IM_3$ ). The input magnitude related to the  $IM_3$  is the Input Third-Order Intermodulation Intercept-Point ( $IIP_3$ ), and represent the input magnitude at which the magnitude of the third-order component starts to dominate the signal over the first-order [26].

Also, the first-order magnitude output can be observed to find the point at which the gain falls by 1 dB, representing the 1-dB Compression Point ( $P_{1dB}$ ).

Equations 2.11 and 2.12 show the  $IIP_3$  and  $P_{1dB}$  expressions, respectively, as a function of the first order coefficient,  $\alpha_1$ , and the third order coefficient,  $\alpha_3$ . The expressions for the coefficient values are given in equations 2.15 and 2.17, respectively.

$$IIP_3 = \sqrt{\frac{4}{3} \left| \frac{\alpha_1}{\alpha_3} \right|} \quad (2.11)$$

$$P_{1dB} = \sqrt{0.145 \left| \frac{\alpha_1}{\alpha_3} \right|} \quad (2.12)$$

Equations 2.15, 2.16 and 2.17 show the expressions for the first, second and third order coefficients, respectively, for a cascode common-source amplifier with source degeneration [44], where the degeneration is represented by a resistance,  $R_s$ , comprising the inductor  $L_s$  parasitic series resistance. For the development of the expressions, a large-signal model of the transconductance of the transistor  $M_1$ ,  $g_{m0}$ , is used as presented in equation 2.14. The factor  $K$  in the  $g_{m0}$  expression stands for the CMOS technology parameters at  $M_1$  current expression [44], mobility  $\mu_N$  and gate oxide capacitance,  $C_{ox}$ .

$$K = \frac{1}{2} \mu_N C_{ox} \left( \frac{W}{L} \right)_{M_1} \quad (2.13)$$

$$g_{m0} = 2K(V_{gs} - R_s I_D - V_{TH}) \quad (2.14)$$

$$\alpha_1 = \frac{\partial I_D}{\partial V_{gs}} = \frac{g_{m0}}{1 + g_{m0} R_s} \quad (2.15)$$

$$\alpha_2 = \frac{\partial^2 I_D}{\partial V_{gs}^2} \frac{1}{2} = \frac{K}{(1 + g_{m0} R_s)^3} \quad (2.16)$$

$$\alpha_3 = \frac{\partial^3 I_D}{\partial V_{gs}^3} \frac{1}{6} = -\frac{2K^2 R_s}{(1 + g_{m0} R_s)^5} \quad (2.17)$$

where  $\mu_N$  is the carrier mobility for  $M_1$  substrate;  $C_{ox}$  is the gate-oxide capacitance of  $M_1$ ;  $W$  and  $L$  are the width and length of  $M_1$ 's gate;  $g_{m0}$  is a large-signal model of the transconductance of the transistor  $M_1$ ;  $V_{gs}$  the gate to source voltage in  $M_1$ ;  $R_s$  is the equivalent parasitic series resistance of inductor  $L_s$  from figure 2;  $I_D$  is the large-signal current in  $M_1$ ;  $V_{TH}$  is the threshold voltage of transistor  $M_1$ ;  $\alpha_1$ ,  $\alpha_2$  and  $\alpha_3$  are the first, second and third order coefficients for the current in  $M_1$ .

The expressions given in the Equations 2.15, 2.16 and 2.17 can be applied in Equation 2.11 to analyze the  $IIP_3$  behavior as a function of the circuit parameters. The resulting expression is shown in Equation 2.18.

$$IIP_3 = \sqrt{\frac{2 g_{m0}}{3 R_s} \frac{(1 + g_{m0})^2}{K}} \quad (2.18)$$

Equation 2.18 shows that the linearity of the circuit benefits from the increment of  $g_{m0}$  and the improvement of the quality factor of the inductor  $L_s$ , resulting in  $R_s$  reduction.

The same substitution is made in the 1-dB compression point expression given by 2.12, resulting in the expression of the Equation 2.19. The expression shows that the increment on  $P_{1dB}$  benefits from the increment of  $g_{m0}$  and the improvement of the quality factor of the inductor  $L_s$ , resulting in  $R_s$  reduction, as with  $IIP_3$ .

$$P_{1dB} = \sqrt{0.145 \left| \frac{\alpha_1}{\alpha_3} \right|} \approx 0.1 IIP_3 = \sqrt{\frac{2 g_{m0}}{3 R_s} \frac{(1 + g_{m0})^2}{10K}} \quad (2.19)$$

### 2.1.7 Stability

The K stability factor,  $K > 1$ , must be satisfied to guarantee stability with any load and source impedance [26]. Equation 2.20 shows its expression, where it is possible to observe a relation with the scattering parameter (S-Parameters) from the two-port derived S-Parameter analysis of the LNA circuit [26].

$$K = \frac{1 + (S_{11}S_{22} - S_{12}S_{21})^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|} \quad (2.20)$$

where K is the stability factor [26];  $S_{11}$ ,  $S_{12}$ ,  $S_{21}$  and  $S_{22}$  are the scattering parameters of the LNA.

Assuming a high reverse isolation and relatively high output impedance, a usual scenario in integrated LNAs [26], the expression can be reduced to the one shown by Equation 2.21.

$$K = \frac{1 - |S_{22}|^2}{2|S_{21}||S_{12}|} \quad (2.21)$$

Hence, LNA can be stabilized by maximizing its reverse isolation. The chosen topology contributes for that, as the addition of the cascode transistor increases the reverse isolation compared to the common-source amplifier.

### 2.1.8 Design Procedure

The design procedure of the LNA involves the use of the knowledge acquired with the expressions for matching, noise, gain and linearity applied for sizing of the circuit, fulfilling the specification requirements.

Figure 7 shows the full circuit for the LNA including bias network and parasitic devices. Transistor  $M_3$ , and resistors  $R_{b1}$  and  $R_{b2}$  comprise the biasing circuit, responsible for generating the DC common-mode voltage at the gate of  $M_1$ , biasing it to the required overdrive voltage.

The resistor  $R_{bw}$  and inductor  $L_{bw}$  relate to the resistance and inductance from the bonding wire connecting the die pad to the chip external pin, respectively. The capacitances  $C_{pin}$  and  $C_{pad}$  are the external pin and internal die pad capacitances, respectively.

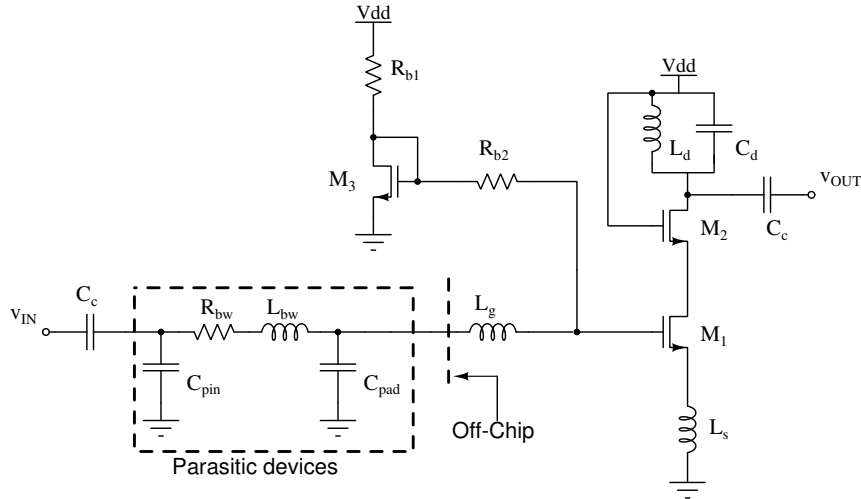


Figure 7: LNA circuit showing the biasing circuit, and off-chip parasitic passive elements.

Source: Author

As a suggestion for the circuit sizing, the following steps may be applied.

For an ULV design, it is important to assure that the transistors are capable of operating at the required frequency range. Equation 2.22 shows the expression for the transistor  $M_1$  transfer frequency, a measure of the maximum frequency in which the transistor allows amplification [44]. Therefore, it is required that  $f_T \gg f_b$ , where  $f_b$  represents the maximum frequency in the required operating frequency band.

$$f_T = \frac{g_{m1}}{2\pi C_{gs}} \quad (2.22)$$

where  $f_T$  is the transfer frequency for MOSFET  $M_1$ ;  $g_{m1}$  is the transconductance of  $M_1$ ; And  $C_{gs}$  is the gate to source capacitance of  $M_1$ .

Therefore, due to the low overdrive voltage imposed by the ULV supply,  $g_{m1}$  requires a carefully inspection as to assure the required  $f_T$ . For the operation in saturation region, the capacitance  $C_{gs}$  may be approximated to  $C_{gs} \approx (2/3)WLC_{ox}$ , where  $W$  and  $L$  are the MOSFET width and length, respectively, and  $C_{ox}$  its gate-oxide capacitance. The transconductance,  $g_{m1}$  can be defined as  $g_{m1} = \mu_N C_{ox} (V_{OV})$ , where  $V_{OV}$  is the overdrive voltage,  $V_{OV} = V_{GS} - V_{TH}$ , and  $\mu_N$  is the carrier mobility at  $M_1$  channel.

Equation 2.23 shows the resulting expression after replacing the referred quantities. It implies that, at minimum channel length, a minimum  $V_{OV}$  must be satisfied to allow the operation in the required frequency range. The minimum  $V_{OV}$  must be determined at

the design beginning, thus setting a limit for the input common-mode voltage. Moreover, the MOSFET  $V_{TH}$  have its value related to the transistor length, thus an analysis may be applied on finding the optimal length for maximum  $f_T$  response.

$$f_T \approx \frac{3}{2} \mu_N \frac{V_{OV}}{L^2} \quad (2.23)$$

where  $L$  is the channel length of  $M_1$ .

Then, for the input matching realization, the expression of  $Z_{in}$  is observed. Its real part,  $\frac{g_{m1}}{C_{gs}} L_s$  can be changed into the relation in Equation 2.24, where  $\omega_T$  is the angular transfer frequency,  $g_{m1}/C_{gs}$  and  $L_s$  the source inductance.

$$Re \{Z_{in}\} = \omega_T L_s \quad (2.24)$$

where  $Re \{Z_{in}\}$  is the real part of the input impedance  $Z_{in}$ ; And  $\omega_T$  is the angular transfer frequency for MOSFET  $M_1$ .

Since  $\omega_T = 2\pi f_T$ , the value of  $Re \{Z_{in}\}$  can be adjusted by changing the value of the inductor  $L_s$ , or changing  $V_{OV}$ , if possible.

The value of the gate inductor,  $L_g$ , is chosen to set the imaginary part of  $Z_{in}$ ,  $Im \{Z_{in}\}$ , to zero.

The frequency of the minimum noise figure is related to  $M_1$  channel width [27], which can be adjusted to set the minimum noise figure at the center of the frequency range of interest.

The size for  $M_2$  can be the same obtained for  $M_1$ , helping to achieve a better layout matching.

The load inductor  $L_d$  is chosen to adjust the gain, where a quality factor maximization is favorable for a large gain. Moreover, the capacitor  $C_d$  is sized to set the load resonating frequency at the center of the frequency range of interest.

## 2.2 Mixer

The Mixer block is responsible for frequency translation in the receiver. In the case of the RF Front-End at the receiver, it is referred as downconversion mixer, due to its characteristic of converting a high frequency input signal in a low frequency output.

As shown in Equations 2.25 and 2.26, the mixer function applies a multiplication

between the sinusoidal signals coming from the LNA and from the LO. The multiplication results in a frequency translated output, with a low frequency component at  $\omega_{RF} - \omega_{LO}$  and other high frequency component at  $\omega_{RF} + \omega_{LO}$ . In the case of a downconversion Mixer, the low frequency component is the signal of interest, and the high frequency component will be filtered out by the next stages of the receiver.

$$y_{mixer} = A_1 \cos(\omega_{RF} t) \times A_2 \cos(\omega_{LO} t) \quad (2.25)$$

$$y_{mixer} = \frac{1}{2} [A_1 A_2 \cos(\omega_{RF} - \omega_{LO}) + A_1 A_2 \cos(\omega_{RF} + \omega_{LO})] \quad (2.26)$$

where  $y_{mixer}$  represents the signal at the output of the mixer block;  $A_1$  and  $A_2$  are the peak amplitude of the RF signal coming from the LNA and the signal from LO, respectively;  $\omega_{RF}$  and  $\omega_{LO}$  are the angular frequency of the sinusoidal signal representing the output of the LNA and LO, respectively.

The following analysis present the topology choice, and development of expressions that describe the Mixer noise, gain, linearity and input impedance behavior. Moreover, a design procedure based on the gathered expressions is presented.

### 2.2.1 Topology Choice

Recent works show a strong tendency in using a passive topology to implement the downconversion Mixer [7, 11, 33, 43], reinforcing the benefits of applying it to ULP designs. Also, its passive structure does not demand great voltage headroom.

As shown in figure 8, the simple structure of a single-balanced passive mixer is composed by two MOS switches, that modulate the input single-ended signal into a differential signal containing the high and low signals resulting from the frequency translation [26].

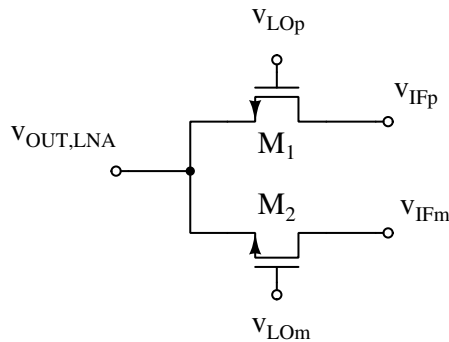


Figure 8: Single balanced passive mixer circuit based on MOS switches.

Source: Author

As suggested by [26], the use of a sampling mixer, or "non return to zero" (NRZ) mixer, using capacitors as load, as in sample-and-hold circuit, results in a gain slightly above 0 dB.

### 2.2.2 Noise

For the mixer, Single Side-Band (SSB) noise is considered. It gets contribution from image band, having 3dB noise contribution despite of mixer circuit contribution [26].

For Zero-IF receivers, the major concern is in reducing the noise around DC, employing techniques to reduce the flicker noise from the MOSFETs [45, 46]. However, in a Low-IF implementation, as the signal of interest will be centered at an IF frequency, the flicker noise is not a major concern, allowing the implementation of a DC biased passive mixer [26, 47]. The DC biased mixer brings the advantage of having a larger input impedance, avoiding the need for a buffer stage in the LNA, as in the case of a current-driven mixer. Also, it allows the interfacing with a high impedance load at the IF stage, apart from the current-drive that often requires a Transimpedance Amplifier (TIA) interface [33, 45].

In this work, the implementation of a Low-IF receiver is considered, alleviating the concern about the flicker noise near DC spectrum. Figure 9 shows the single-balanced passive mixer topology, along with the noise sources related to  $R_{ON}$  resistance.

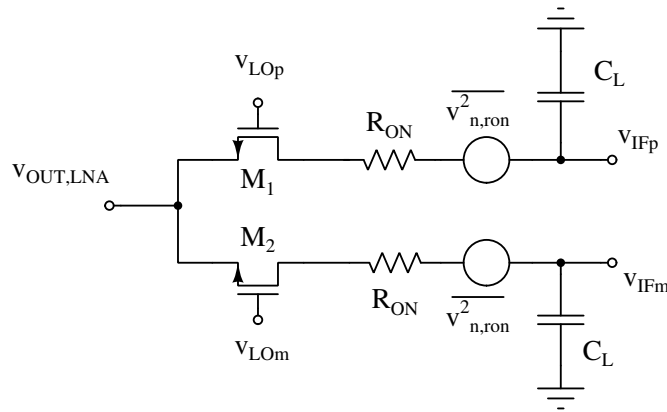


Figure 9: Passive mixer showing  $R_{ON}$  resistances and their related noise voltage sources  $\overline{v_{n,ron}^2}$ .

Source: Author

A complete analysis of the thermal noise behavior in the  $R_{ON}$  resistance is presented by [47], where the noise behavior is presented for the periods when the switch is on or off. Simplifying the expression shown in [47], it is possible to see that in any case the thermal noise spectral density is proportional to  $\frac{kT}{C}$ , where  $k$  is the Boltzmann constant,  $T$  the absolute temperature in Kelvin, and  $C$  the capacitance connected to the switch, in the case of Figure 9 being represented by  $C_L$ , the input capacitance of the next stage.

This noise behavior is expected in the analysis of sample-and-hold circuits with a similar arrangement of MOS switch and capacitor [48]. Therefore, this result suggests that a possible design procedure to adjust noise contribution from the mixer is to control the capacitance seen in its output, although this approach may be difficult due that it is not always possible to control the sizing of the next stage.

### 2.2.3 Gain

In [26], an extensive analysis on the gain of the sampling mixer is presented, based on the study of the discrete-time system response for when the switch is on, and the mixer is sampling the input signal, and for when the switch is off, in which the load capacitor holds the previously sampled signal.

Equation 2.27 shows the gain relation for the mixer, where  $Y_1(f)$  and  $Y_2(f)$  represent the response of the MOS switch and capacitor pair in the sampling and hold periods, respectively [26]. It is possible to see the frequency translation on the input  $X(f)$  to



$X(f \pm f_{LO})$  at the mixer output, where a high frequency and low frequency components are generated.

$$|Y_1(f) + Y_2(f)| = \sqrt{\frac{1}{\pi^2} + \frac{1}{4}} |X(f \pm f_{LO})| = 0.593 |X(f \pm f_{LO})| \quad (2.27)$$

where  $Y_1(f)$  and  $Y_2(f)$  represent the response of the MOS switch and capacitor pair in the sampling and hold periods, respectively;  $X(f \pm f_{LO})$  is the input signal after frequency translation, generating a high and a low frequency components.

For the case of the single-balanced circuit in Figure 8, where two MOS switch and capacitor pairs are implemented with complementary LO signal, the gain result is doubled, as shown in Equation 2.28.

Equation 2.28 shows the case of single-balanced topology gain.

$$|Y_1(f) + Y_2(f)| = 2 \times 0.593 |X(f \pm f_{LO})| = 1.186 |X(f \pm f_{LO})| \approx 1.48dB \quad (2.28)$$

This result shows a gain above 0 dB for the mixer, a satisfactory result for a passive circuit. The presence of a gain instead of an attenuation in this passive circuit is due to the sample-and-hold effect at the capacitors [26].

## 2.2.4 Linearity

The On-Resistance of MOS switches in a sampling circuit varies with the input and output levels [44], therefore affecting the signal linearity. For an input signal  $v_{IN}(t) = V_0 \cos(\omega_0 t) + V_M$ , where  $V_M$  represents the mean value, and  $V_0 = V_{DD}/2$ , the output voltage held at the capacitor is represented by Equation 2.29.

$$V_{out}(t) = \frac{V_0}{\sqrt{R_{on}^2 C_L^2 \omega_0^2 + 1}} \cos[\omega_0 t - \tan^{-1}(R_{on} C_L \omega_0)] + V_M \quad (2.29)$$

where  $V_{out}(t)$  is the output voltage held by the load capacitor  $C_L$ ;  $V_0$  is the mean voltage level of the input signal;  $R_{on}$  is the on-resistance of the MOS switch;  $C_L$  is the load capacitor at the output of the mixer;  $\omega_0$  is the angular frequency of the input signal in rad/s.

The bandwidth must be large to negligibly attenuate the signal, thus  $R_{on} C_L \omega_0 \ll 1$ .

With periodic input,  $R_{on}$  varies periodically, therefore can be approximated by a fourier series, as seen in Equation 2.30.

$$R_{on}(t) = R_0 + R_1 \cos(\omega_0 t) + R_2 \cos(2\omega_0 t) + \dots \quad (2.30)$$

where  $R_{on}(t)$  is the time-varying on-resistance of the MOS switch;  $R_n$  the coefficients for each harmonic  $n$ ;  $\omega_0$  is the angular frequency of the input signal in rad/s.

Based on the Equation 2.30, the total harmonic distortion (THD) in the mixer can be calculated, as seen in Equation 2.31. The THD thus serves as a metric for the mixer nonlinearity.

$$THD = \frac{R_1^2 + R_2^2}{4} C_L^2 \omega_0^2 \quad (2.31)$$

where THD is the total harmonic distortion measurement for the MOS switch and capacitor mixer;  $R_1$  and  $R_2$  are the coefficients for the first and second harmonics, respectively;  $C_L$  is the load capacitance at the output of the mixer;  $\omega_0$  is the angular frequency of the input signal in rad/s.

The expression in 2.31 suggests that the distortion may be alleviated by minimizing the capacitance  $C_L$ . Also, the hamonics' coefficients  $R_1$  and  $R_2$  can be obtained by derivating the resistance function in the time-domain, shown in Equation 2.32.

$$R_{ON}(t) = \frac{1}{k'_n \frac{W}{L} (V_{DD} - v_{IN}(t) - V_{TH})} \quad (2.32)$$

As shown in [44], the resistance of the switch rapidly grows as  $V_{DD} - v_{IN}$  approaches  $V_{TH}$ , stating that the switch is approaching the off-state. Therefore, an operation condition where the signal  $v_{IN}(t)$  spans a peak-to-peak value of  $V_{DD} - V_{TH}$  is the worst case for distortion, as the steeper  $R_{ON}(t)$  response in time would result in great values for the harmonic coefficients  $R_1$  and  $R_2$ , related to the time-domain derivative of  $R_{ON}(t)$ .

Therefore, a proper design strategy to minimize distortion is to minimize  $C_L$ , and work with peak-to-peak  $v_{IN}$  span much less than  $V_{DD} - V_{TH}$ , or  $v_{IN}(t)_{max} \ll V_{DD} - V_{TH}$ .

## 2.2.5 Input Impedance

The input impedance analysis for the sampling mixer is based on its discrete-time behavior, where the input impedance  $Z_{in, sb}$  of the single-balanced passive mixer is derived from the expression of its frequency-domain current response,  $I_{in}(f)$ , and the input signal in frequency domain,  $X(f)$ , as reported in [26]. Result in the final expression is shown in Equation 2.33.

$$Z_{in, sb}(\omega) = \frac{1}{2} \left[ R_{ON} + \frac{1}{j\omega C_L} \right] \quad (2.33)$$

The result for the input impedance  $Z_{in, sb}$  will be applied in the RF Front-End design, where it will represent the load impedance seen in the output of the LNA.

## 2.2.6 Design Procedure

The following design steps are suggested in this work for the Mixer design, where its bandwidth, linearity and DC biasing is concerned.

The Mixer bandwidth, gave by the relation of its time-constant  $R_{ON}C_L$ , suggests that as  $C_L$  is often given by the input capacitance of the subsequent stage, the value of  $R_{ON}$  may be calculated, so that  $\frac{1}{R_{ON}C_L} \gg \omega_c$ , where  $\omega_c$  stands for the maximum frequency of the input signal.

For linearity improvement, the relation obtained in the previous Linearity section must be satisfied, thus  $v_{IN_{max}} < V_{DD} - V_{TH}$ .

Figure 10 shows the DC bias placement for the mixer. Ideally, a common-mode value of  $v_{IN_{max}}/2$  may be defined for the mixer DC biasing voltage  $V_b$ , thus assuring the required operation or a peak-to-peak  $v_{IN}$  of  $v_{IN_{max}}$ .

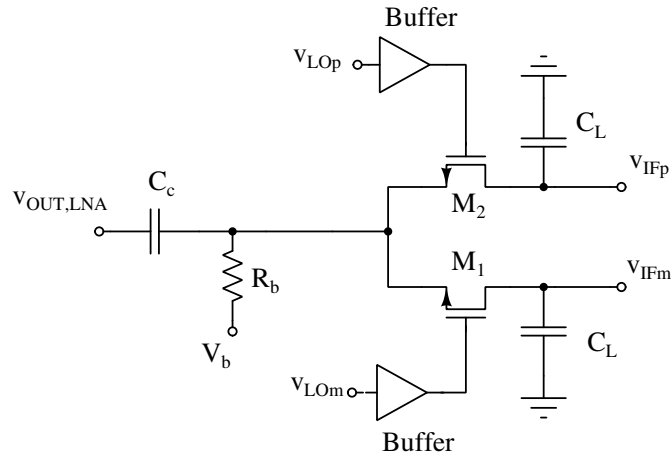


Figure 10: Single-balanced passive mixer circuit showing biasing and LO buffers.

Source: Author

## 2.3 RF Front-End with LNA and Passive Sampling Mixer

Figure 11 presents the connection of the LNA and mixer, forming the RF front-end circuit. Since the design of the Mixer changes the input impedance seen by the LNA, and other parameters of the LNA depend on the mixer performance, such as LNA gain related to mixer noise, it is expected that design iterations have to be made to assure the maintenance of the desired performance for the two blocks.

Therefore, the design procedure for the RF Front-End may start with the LNA design, using a expected theoretical load impedance value, based on the previously presented input impedance expression for the Mixer. After, the design of the mixer, using the data from the impedance of the subsequent block, and performance specifications of the input signal, linearity and noise is done. Finally, the inspection of the two blocks connected, forming the RF Front-End, and adjustment of the performance parameters are executed.

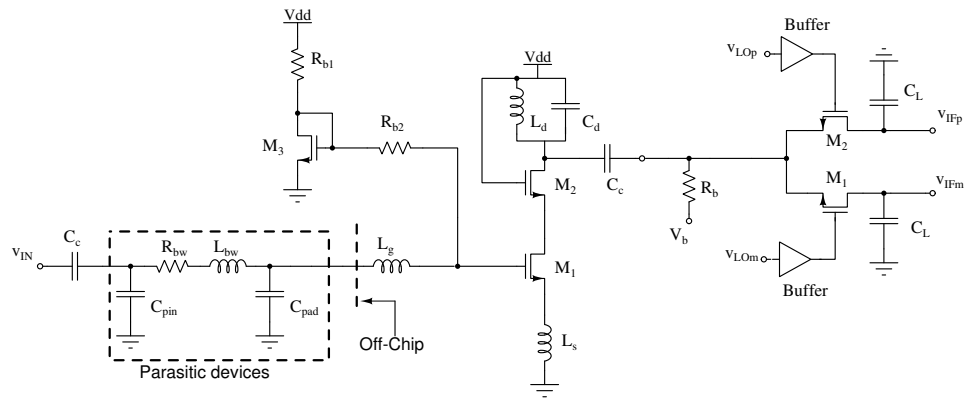


Figure 11: RF Front-End circuit showing LNA and Mixer circuits with the chosen topologies.

Source: Author

### 3 IMPLEMENTATION AND EXPERIMENTAL RESULTS

This chapter includes the implementation of the circuits proposed for the solution of the stated problem. Three design implementations are presented, using 180nm CMOS technology and 130nm CMOS technology.

The first design corresponds to the first approach to design a LNA with a reduced voltage supply of 0.5 V, minimizing its power consumption. Using the theoretical formulations from the methodology chapter, the boundaries of the solution are analyzed. Thus, resulting in a good start point for performing the simulations. The initial assumptions are used to perform the design using a 180nm CMOS technology from TSMC. The problem of having a  $V_{TH}$  near to the supply voltage is studied, applying the forward bulk biasing technique when necessary [12, 49, 50].

The second design uses the same 180nm CMOS technology, making an effort to enhance the performance seen on the first design, changing parameters related to gain, linearity, matching and power consumption.

The third design uses a 130nm CMOS technology from GlobalFoundries, and applies the knowledge obtained from the LNA designs, extending it to implement a sampling mixer and an IF amplifier.

All the designs include further study on post-fabrication tests. The design of test boards and strategies for testing the integrated circuits performance are included. Moreover, the designs of the integrated circuits include adjustable biasing structures and Buffer circuits to support the test procedures.

The designs include a Buffer circuit, intended to match the output of the circuit in the last stage with the  $50 \Omega$  input impedance of the measurement equipment. This approach guarantees that the circuit's gain is not affected. In each design case, the Buffer topology choice is detailed showing the benefits of each choice.

During the design, the performance of the circuits is evaluated using schematic and

post-layout simulations. The design and simulations were realized using software tools by Cadence Design Systems. The schematic capture and layout used is the Virtuoso, the simulations were configured using the Analog Design Environment (ADE) and performed using the Spectre simulator. Assura was used for the layout verification, including design rule check (DRC) and layout versus schematic (LVS) simulations. Quantus QRC was used for the parasitic extraction after the layout verification. The post-layout simulations were performed with ADE and Spectre using the extracted models from Quantus QRC. Moreover, Mentor Calibre software was also used for design rule check (DRC) simulation after the circuits layout.

After the design of the integrated circuits, the design of the test structures have been performed. The Autodesk EAGLE software was used for the design of printed circuit boards (PCB) to perform the interface between the fabricated integrated circuits and the test equipment [51]. In the PCBs are included interface circuits for the RF inputs and outputs, such as passive matching networks and SubMiniature version A (SMA) coaxial connectors. Moreover, structures for DC biasing setting are also included. The PCB design mostly used surface-mounted devices (SMD) to reduce the board area, as well as to reduce path lengths and component parasitics, thus reducing the performance degeneration in RF circuits.

The Keysight ADS software was used to aid in the sizing of the PCB tracks in the RF signal paths. Those tracks were considered transmission lines, observing the reflection and phase displacement through the track. The LineCalc tool in ADS was used, based on the FR-4, material of the PCB substrate, its permittivity, the substrate thickness and track length. The track width was designed for a characteristic impedance of  $50 \Omega$ , making an optimal matching with the test equipment and the integrated circuits.

In the first design, including integrated LNA and Buffer circuits fabricated using 180nm CMOS technology, the chip-on-board method [52] was used to connect the fabricated die to the PCB. Wire bonding was used to connect the pads of the fabricated die to the PCB pads. The other two designs used standard SMD packages instead.

Tables 4, 5 and 6 present the design specifications for the RF Front-End, the LNA and the Mixer blocks, respectively. The specifications are to be followed as the design objective for the blocks in this chapter.

Table 4: Design specifications for the RF Front-End design following BLE specification.

Parameter	Value
Supply Voltage	0.5 V
Power Consumption	< 1 mW
Noise Figure, SSB	< 20 dB
Input Power	$\leq$ -20 dBm
1 dB Compression Point	> -35 dBm
$IIP_3$	> -25 dBm
Conversion Gain	> 10 dB
Input Reflection Ratio ( $S_{11}$ )	< -10 dB
Input Impedance	50 $\Omega$
Input frequency band	2.4 GHz - 2.4835 GHz
Input center frequency	2.44 GHz
Output Intermediate Frequency	2 MHz

Table 5: Design specifications for the LNA design following BLE specification.

Parameter	Value
Supply Voltage	0.5 V
Power Consumption	< 1 mW
Noise Figure	< 10 dB
Input Power	$\leq$ -20 dBm
1 dB Compression Point	> -35 dBm
$IIP_3$	> -25 dBm
Power Gain ( $S_{21}$ )	$\geq$ 10 dB
Input Reflection Ratio ( $S_{11}$ )	< -10 dB
Input Impedance	50 $\Omega$
Input frequency band	2.4 GHz - 2.4835 GHz
Input center frequency	2.44 GHz



Table 6: Design specifications for the Mixer design following BLE specification.

Parameter	Value
Noise Figure, SSB	< 20 dB
1 dB Compression Point	> -35 dBm
$IIP_3$	> -25 dBm
Conversion Gain	$\approx$ 0 dB
Input frequency band	2.4 GHz - 2.4835 GHz
Input center frequency	2.44 GHz
Output Intermediate Frequency	2 MHz

### 3.1 First LNA design in 180nm CMOS technology

The first design implementation included in this work is a cascode common-source LNA with inductive source degeneration in 180nm CMOS technology. The device parameters are based on a process design kit (PDK) from the TSCM foundry. The PDK also includes simulation models using BSIM3 standard and design rules files for layout verification.

The design follows the chosen specifications, which include supply voltage ( $V_{DD}$ ) at 0.5 V. The main design objective is to minimize power consumption, keeping a gain value higher than 10 dB and noise figure below the calculated maximum. Thus, the transistors' operation must be driven towards weak inversion, which brings difficulties to RF design, since the maximum operational frequency is reduced on this inversion mode. Therefore, the devices are required to achieve a transconductance level that results in a good gain and noise figure performance.

Due to reverse short-channel effect, The threshold voltage ( $V_{TH}$ ) behavior in the 180nm CMOS technology used in this work increases as the channel length approaches the technology minimum [53]. Consequently, the design for operation at higher frequencies, despite benefiting from channel length reduction, has an added complexity for low supply voltage due to the  $V_{TH}$  behavior.

The first design also includes a Buffer in a common source configuration with current-source load topology. The Buffer is designed to have a gain near to 0 dB. Thus, it has low impact on the measured gain, which approximates the LNA gain. However, compared to the other buffer designs in this work, shows a larger area, power consumption, and an added complexity to define the output common-mode voltage [44].

Figure 12 shows the full design of the LNA and Buffer, showing integrated and discrete parts, as well as the board and chip parasitic devices.

The considered parasitic passive devices come from the bondwire, internal pad and PCB or package pins.  $R_{bw}$  and  $L_{bw}$  stand for the bondwire resistance and inductance, respectively [54].  $C_{pin}$  and  $C_{pad}$  represent the capacitance from off-chip connection and integrated pad, respectively.  $C_{pin}$  may receive capacitive contributions from package pins, when the die has a package, or solely PCB connection when chip-on-board connection is used. The parasitic devices from bondwires, pads and pins are present in connections between the integrated circuits and off-chip components. Those parasitic components are represented in the circuit by the impedance values  $Z_{par\_in}$  and  $Z_{par\_out}$ . The resistors  $R_{bias}$  adjust the reference current  $I_{bias}$  biasing the LNA and Buffer circuits.  $C_c$  and  $C_{c\_int}$  capacitors perform the ac coupling between input source and LNA input pin, and between LNA output and Buffer input, respectively. The input matching network, responsible for controlling the LNA input impedance  $Z_{in}$  is realized using inductor  $L_{match}$  and capacitor  $C_{match}$ .

Apart from the devices represented inside the rectangle with label "Integrated" and  $C_{pad}$ , all elements in the figure represent off-chip devices or parasitic entities.

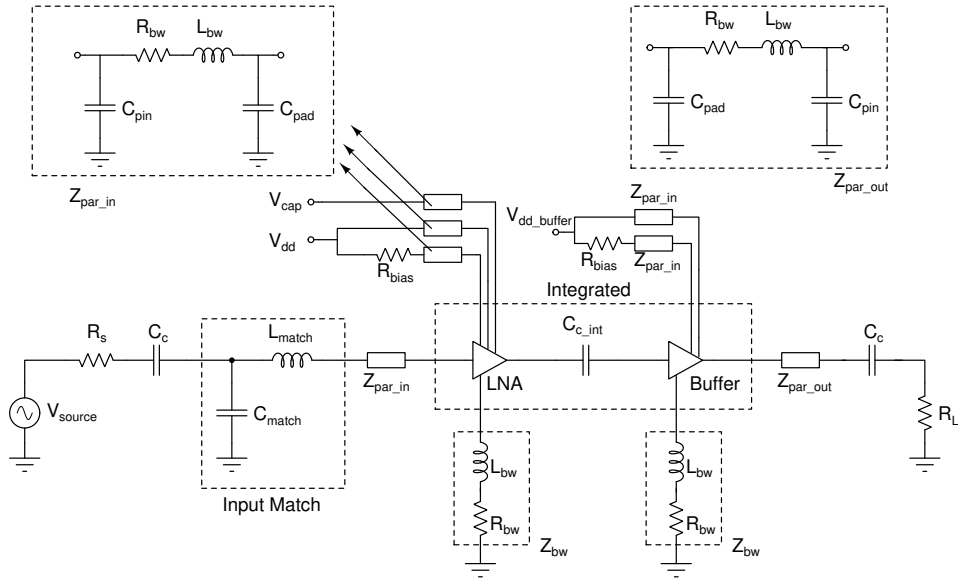


Figure 12: The implemented cascode common-source LNA with inductive source degeneration and common-source Buffer circuit in 180nm CMOS technology.

Source: Author

$C_{pin}$  and  $C_{pad}$  are estimated values based on connection dimensions.  $C_c$  is chosen to be a value to give a sufficient low frequency high-pass cutoff, performing the required signal coupling. Load resistance  $R_L$  value is based on the standard load resistance of the measurement equipment.

The resulting dimensions for the LNA and Buffer circuit are shown in Table 7.

Table 7: Device dimensions for the LNA and buffer circuit.

Parameter	Value
$R_s$	50 $\Omega$
$R_{bias}$	3 k $\Omega$
$R_{bias,buffer}$	5 k $\Omega$
$L_{match}$	9.88 nH
$C_{match}$	1.85 pF
$R_{bw}$	1 $\Omega$
$L_{bw}$	1 nH
$C_{pin}$	100 fF
$C_{pad}$	100 fF
$C_c$	100 nF
$R_L$	50 $\Omega$
$V_{DD}$	0.5 V
$V_{DD,buffer}$	1.8 V

Figure 13 shows the LNA circuit, implementing the cascode common-source with inductive degeneration topology, along with parasitic and external components. The topology was adapted from the one shown in the methodology chapter of this work. The LC tank capacitor was replaced for a variable capacitor to allow adjustments on the resonating frequency of the LC tank after fabrication. The gate inductor was removed from the integrated circuit and is implemented as off-chip by the matching network inductor  $L_{match}$ . The source inductor was also removed, being replaced by the bondwire inductance on the source terminal,  $L_{bw}$ . The removal of the gate and source inductors resulted in a substantial reduction on the circuit area after the layout phase. Moreover, the implementation added terminals for bulk biasing of the MOSFETs.

The elements in the input match circuit, and parasitic devices in  $Z_{par.in}$  are the same as described for the LNA and Buffer circuit.

Transistor  $M_3$  drain voltage is defined by the sizing of  $M_3$  and the incoming  $I_{bias}$ , and

set the input common-mode voltage of  $M_1$ . The resistor  $R_{bias}$  combined with  $M_3$  gate capacitance perform a low-pass filtering, avoiding signal leakage from the input node.

$C_c$  and  $C_{c\_int}$  capacitors perform the ac coupling between input source and LNA input pin, and between LNA output and Buffer input, respectively. The input matching network, responsible for controlling the LNA input impedance  $Z_{in}$  is realized using inductor  $L_{match}$  and capacitor  $C_{match}$ .

As with the LNA and Buffer circuit, input match,  $Z_{par\_in}$  and  $Z_{bw}$  represent off-chip devices or parasitic entities.

$C_L$  represents the load capacitance, in this case coming from the input of the Buffer stage.

$L_D$  act as a tuned load for the amplifier, and is designed to give the required gain, based on its embedded parallel resistance.

$C_D$  is a variable capacitor that permits adjusting the output matching of the circuit with  $L_D$  and  $C_L$ .

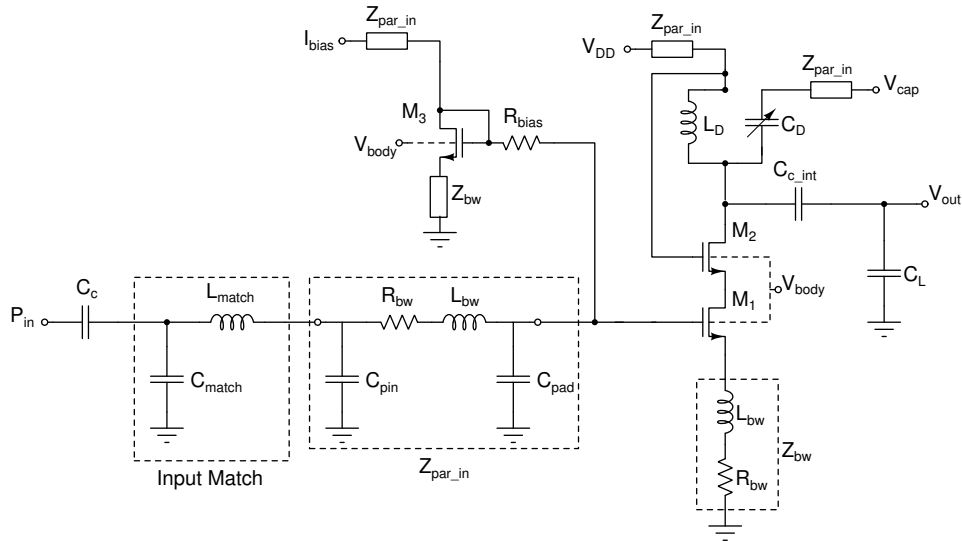


Figure 13: The cascode common-source LNA with inductive source degeneration circuit in 180nm technology, along with parasitic and other external devices.

Source: Author

The LNA circuit design followed the steps of the design strategy proposed in the methodology chapter of this work. The PDK parameters were observed through simulations with the available NMOS and PMOS transistors. As suggested in the proposed

strategy, the first approach is to verify if the transfer frequency ( $f_T$ ) for the MOSFETs biased with 0.5 V supply is sufficient to allow the operation in the desired frequency range, between 2.4 GHz and 2.4835 GHz.

This design comprises  $V_{TH}$  reduction using the forward bulk biasing (FBB) approach [12, 49, 50]. This technique uses a positive bulk to source voltage  $V_{BS}$ , as a way to lower the threshold due to depletion region length reduction on the MOSFET substrate.

Equation 3.1 [44] shows the relation between  $V_{TH}$  and the bulk to source voltage  $V_{BS}$ . For  $\phi_F$  representing the fermi potential, with voltage level between 0.3 V and 0.4 V.

$$V_{TH} = V_{TH0} + \gamma \left( \sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F} \right) \quad (3.1)$$

where  $V_{TH}$  is the MOSFET threshold voltage;  $V_{TH0}$  is the MOSFET threshold voltage component without body effect;  $\gamma$  is the body effect coefficient;  $\phi_F$  is the fermi potential for the bulk semiconductor;  $V_{bs}$  is the voltage potential between the MOSFET bulk and source terminals.

Table 8 shows the  $f_T$  response as a function of the applied  $V_{BS}$  voltage, simulated using the technology device models for a nMOS transistor, the same used for the input stage of the amplifiers in this design. The nMOS device used a minimum channel length of 180nm. It shows that for a biasing without applied FBB the  $f_T$  would not be sufficient for the desired operational frequency range.

Table 9 shows the simulated threshold voltage response as a function of the applied  $V_{BS}$  voltage for a nMOS transistor using a minimum channel length of 180nm. Again, the results show  $V_{TH}$  values matching the design needs for higher  $V_{BS}$  values.

Table 8: Transfer frequency response as a function of the applied bulk to source voltage.

$V_{BS}(V)$	0	0.1	0.2	0.3	0.4	0.5
$f_T(GHz)$	0.95	1.7	2.9	4.8	7.5	11

Table 9: Threshold voltage response as a function of the applied bulk to source voltage.

$V_{BS}(V)$	0	0.1	0.2	0.3	0.4	0.5
$V_{TH}(V)$	0.55	0.52	0.49	0.46	0.425	0.39

While resulting in satisfactory reduction of the  $V_{TH}$ , applying FBB exponentially increases the current leakage through the forward biased junction between bulk and source

terminals, and therefore, leading to additional power consumption and possible latch-up failure. To account for those drawbacks, the  $V_{BS}$  voltage used in the FBB has to be constrained to a maximum harmless value. The maximum voltage of 0.5 V considered for this design assures that the critical current conduction levels in the forward biased junction are not achieved.

Moreover, the increased bulk potential also results in a reduction of the depletion region length in the MOSFET substrate. This effect leads to higher device capacitances.

The choice of the input common-mode gate voltage,  $V_{CM}$ , was based on the results showed in the  $f_T$  simulations as a function of  $V_{GS}$  and the channel length. A  $V_{CM}$  of 400 mV is proposed, giving a room for maximum 200 mVpp input, or -10 dBm. A safety margin is added, considering maximum -20 dBm input, with maximum 100 mVpp input signal.

Following, the input matching is performed, by analyzing the impedance of the LNA input, and applying L-type network match procedure to achieve a input impedance of 50  $\Omega$  [26]. The L-type network was implemented by the  $L_{match}$  and  $C_{match}$  components.

The width of  $M_1$  was adjusted to set the minimum noise figure response at the center of the required input signal frequency range [27, 55].

After the input matching, the value of the inductor  $L_D$  was adjusted to achieve the required gain. Moreover, the center of the capacitance range given by  $C_D$  is set to match the LC tank with the capacitance from the subsequent stage's input and the capacitances attached to the drain of  $M_2$ .

The resulting dimensions for the LNA circuit are shown in Table 10.

The value of the parasitic devices and coupling capacitor  $C_c$  are the same for the LNA and buffer circuit. The value of  $L_{match}$  and  $C_{match}$  from the input matching circuit are also the same as given in table 7.

Transistors  $M_1$  and  $M_2$  dimensions are given by the ratio of their channel width and length.

Table 10: Device dimensions for the LNA circuit.

Parameter	Value
$M_1, M_2$	128 $\mu m$ / 0.18 $\mu m$
$L_D$	1.16 nH
$C_D$	0.3 - 1 pF
$R_{bias}$	16 k $\Omega$
$C_{c_{int}}$	7 pF
$V_{body}$	0.5 V

Figure 14 shows only the Buffer circuit, implementing the cascode common-source topology, along with parasitic and external components.

For this circuit and the following implementations shown in this work, unless otherwise represented or stated, the bulk terminals of NMOS and PMOS transistors are connected to ground and  $V_{DD}$  pins, respectively.

The elements in the input match circuit, and parasitic devices in  $Z_{par.in}$  are the same described for the LNA and Buffer circuit.

The  $M_5$  drain voltage acts as common-mode reference to transistor  $M_1$ . Its drain voltage is defined by the relation of its aspect ratio,  $\frac{W}{L}$ ,  $R_1$  and  $I_{bias}$ . Moreover, it is a current reference for  $M_3$  and  $M_4$ .  $M_3$  and  $M_2$  set the DC bias current for the output in the drain of  $M_1$ . The resistor  $R_{bias}$  combined with  $M_5$  gate capacitance perform a low-pass filtering, avoiding signal leakage from the input node.

$C_c$  and  $C_{c_{int}}$  capacitors perform the ac coupling between Buffer output and output pin, and between LNA output and Buffer input, respectively.

As with the LNA and Buffer circuit, input match,  $Z_{par.in}$  and  $Z_{bw}$  represent off-chip devices or parasitic entities.

Transistor  $M_1$  and  $M_2$  are designed to have gain near 0 dB with a 50  $\Omega$  load within the BLE frequency band.

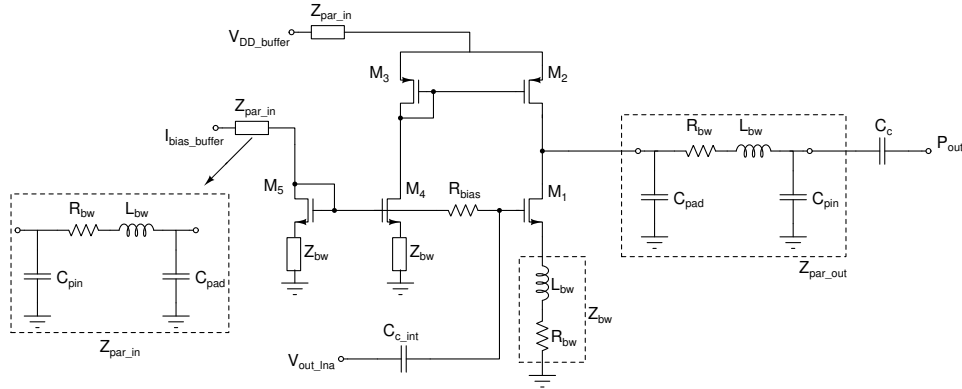


Figure 14: The common-source Buffer with current-source load circuit in 180nm CMOS technology.

Source: Author

The resulting dimensions for the Buffer circuit are shown in Table 11.

The value of the coupling capacitor between LNA and buffer,  $C_{c,int}$ , is the same as in table 10. The value of the coupling capacitor,  $C_c$ , between Buffer and output pin,  $P_{out}$ , is the same as in Table 7.

The supply voltage for the buffer,  $V_{DD,buffer}$  is the same as described in Table 7.

Table 11: Device dimensions for the Buffer circuit.

Parameter	Value
$M_1$	$120 \mu m / 0.4 \mu m$
$M_2$	$136 \mu m / 0.4 \mu m$
$M_3$	$2 \mu m / 0.4 \mu m$
$M_4, M_5$	$1.9 \mu m / 0.4 \mu m$
$R_{bias}$	$16 \text{ k}\Omega$

### 3.1.1 Schematic simulations

After circuit sizing, following the described design procedures, the schematic simulations were used to adjust the results. Figure 15 shows the results for scattering parameters (S-Parameters) simulation of the LNA.

The S21 parameter represents the power gain of the circuit, and shows that it meets the specifications for gain magnitude and frequency tuning. S11 parameter shows the



input insertion loss, and shows a value below -15 dB for the frequencies of interest. The S22 and S12 parameters measure the output reflection and reverse gain, respectively, and show a satisfactory behavior.

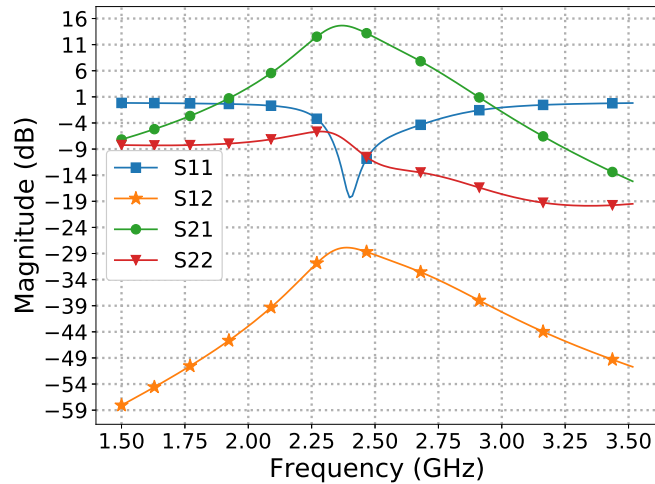


Figure 15: S-Parameter results for the schematic simulations of LNA.

Source: Author

Following the simulations, Figure 16 shows the results for the noise figure simulation of the LNA. The result shows a satisfactory noise figure result, below 4 dB for the frequency range of interest.

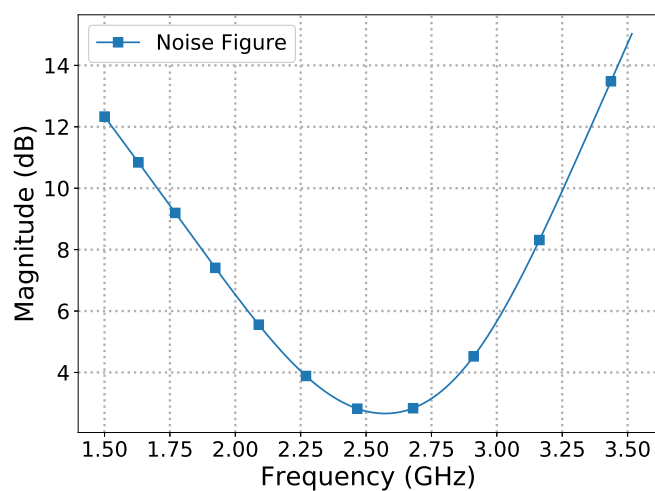


Figure 16: Noise Figure results for the schematic simulation of the LNA.

Source: Author

The linearity measures are performed using a two-tone test simulation [26]. Figure 17 shows the results for the 1-dB compression point simulation of the LNA. The 1-dB compression point result is satisfactory comparing to the expected results.

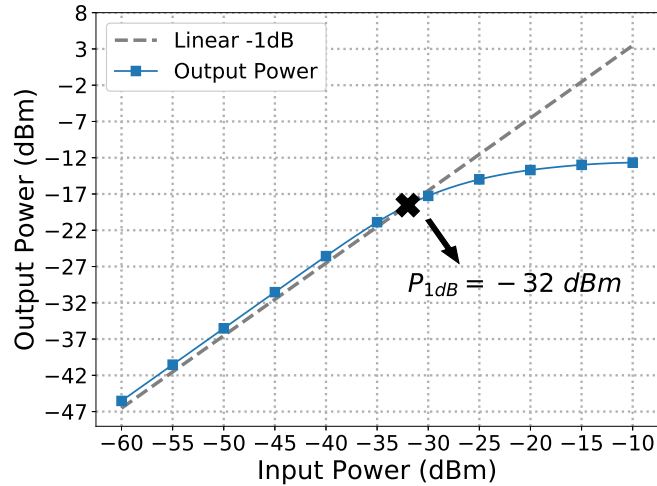


Figure 17: 1-dB compression point result for the schematic simulation of the LNA.

Source: Author

Figure 18 shows the results for two-tone test simulation of the LNA showing third-order intercept point ( $IIP_3$ ) results. The  $IIP_3$  result is satisfactory comparing to the expected results.

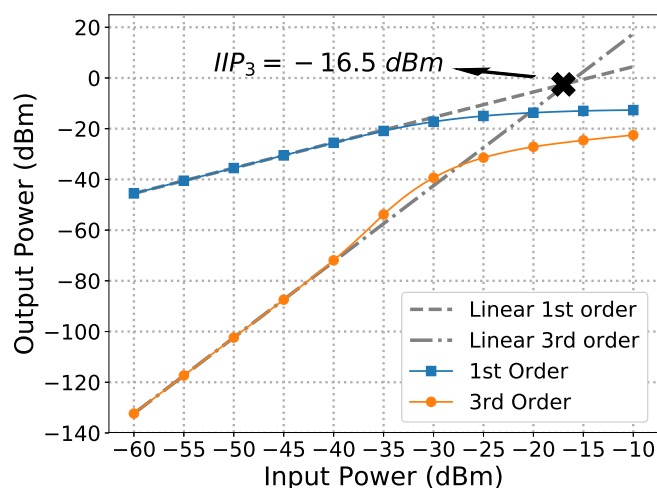


Figure 18:  $IIP_3$  result for the schematic simulation of LNA.

Source: Author

Table 12 shows the performance specifications achieved after schematic simulations.  $I_{DC}$  stands for the DC current from  $V_{DD}$  terminal to ground, and  $P_{DC}$  the power achieved multiplying it by the supply  $V_{DD}$ .

$Re\{Z_{in}\}$  and  $Im\{Z_{in}\}$  represent the real and imaginary components of the input impedance  $Z_{in}$ , respectively.

Table 12: Performance obtained after schematic simulations.

Parameter	Value
Power Gain (S21) (dB)	15.8
Input Return Loss (S11) (dB)	-18
Noise Figure (dB)	3
1-dB Compression Point (dBm)	-32
$IIP_3$ (dBm)	-32
$I_{DC}$ (mA)	0.44
$P_{DC}$ (mW)	0.22
$Re\{Z_{in}\}$ ( $\Omega$ )	58.4
$Im\{Z_{in}\}$ ( $\Omega$ )	-6.11

After assuring that the results obtained satisfy the required specifications, the layout of the circuits is performed.

### 3.1.2 Layout

Figure 19 shows the layout for the LNA and Buffer circuit, describing the specific blocks and the total size.

The layout comprises the integrated components shown during the design steps, where only one integrated inductor is used. The resulting layout shows a dominance of the inductor in the area occupation. The choice of using external matching for the gate inductor, which is usually larger than the others, copes with saving area.

A pitch of 200  $\mu m$  was added at the input and output pads, where each of them presents two ground pins by their sides, in order to reduce noise when interfacing with RF Ground-Signal-Ground (GSG) microprobes.

To save area, no ESD protections are included, demanding careful handling during experimental tests.

Guardring protections are added in the RF transistors to reduce noise. Also, plenty of substrate connections are used, with the same objective.

Metal crossing is avoided to reduce cross coupling noise among metal levels. Each metal level is used either for vertical or horizontal connections, helping to reduce crossing area.

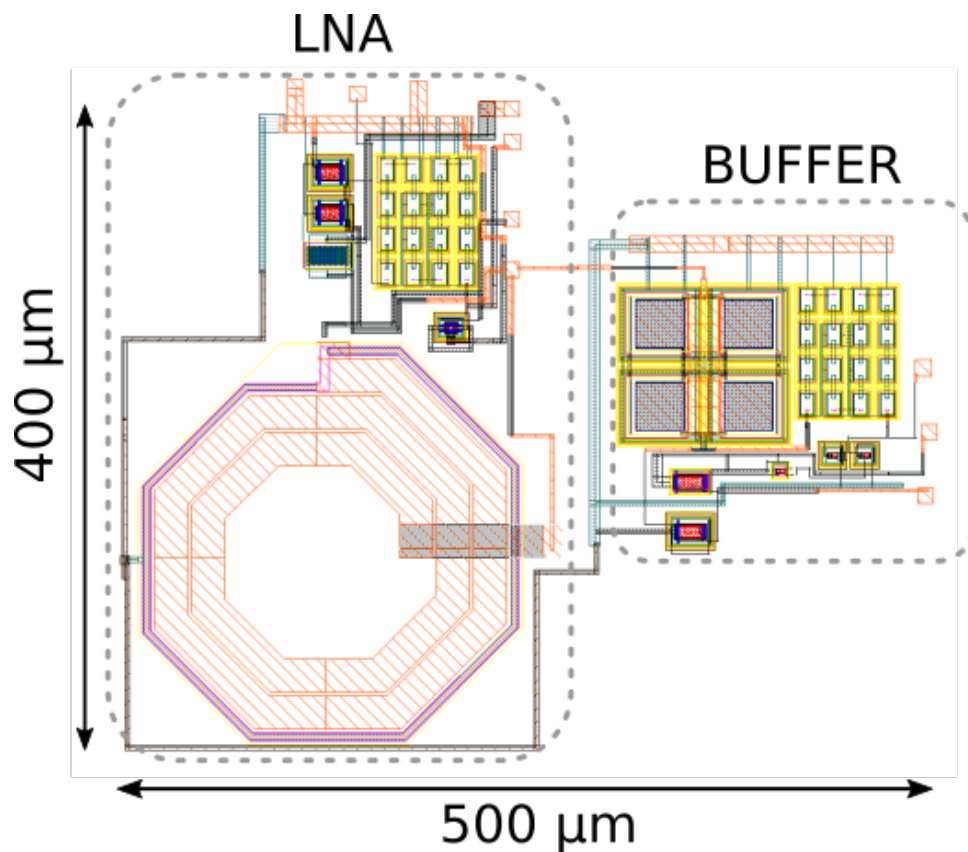


Figure 19: Layout of the LNA and buffer circuits in 180nm CMOS technology.

Source: Author

After iterations between schematic and post-layout simulations, some component values were adjusted accounting for the parasitic variations after the layout.

Table 13 shows the final values for the LNA and buffer circuit, after the necessary adjustments from the initial values on table 7.

Table 13: Final sizing values for LNA and buffer circuit after adjustments.

Parameter	Value
$L_{match}$	8.6 nH
$C_{match}$	1.55 pF
$R_{bias}$	1 k $\Omega$
$R_{bias,buffer}$	5 k $\Omega$

### 3.1.3 Post layout simulations

After layout and parasitic extraction, the same tests were applied and the results adjusted and compared.

Figure 20 shows the results for scattering parameters (S-Parameters) simulation of the LNA and Buffer circuits.

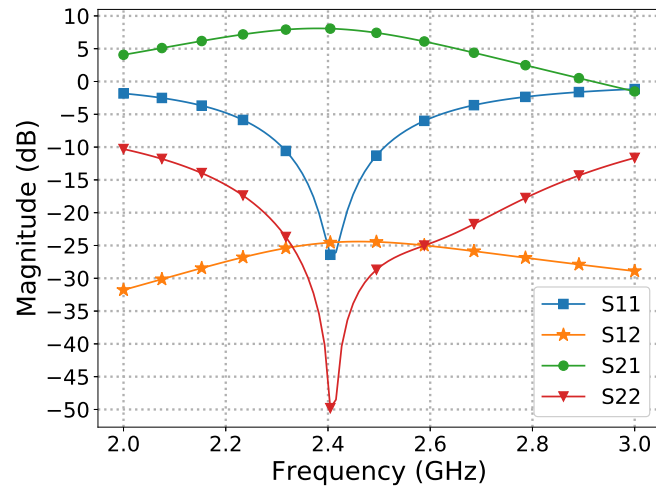


Figure 20: S-Parameter results for the post-layout simulation of the LNA and Buffer circuit in 180nm CMOS technology.

Source: Author

Figure 21 shows the results for noise figure simulation of the LNA and Buffer circuit.

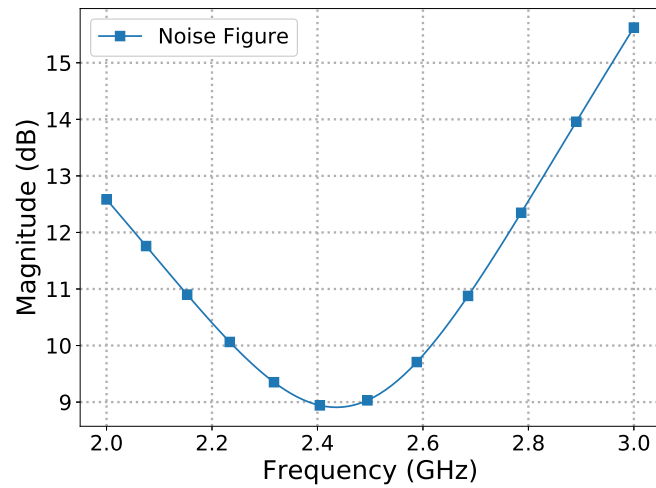


Figure 21: Noise Figure results for the post-layout simulation of the LNA and Buffer circuit in 180nm CMOS technology.

Source: Author

Figure 22 shows the results for 1-dB compression point simulations of the LNA and Buffer circuit.

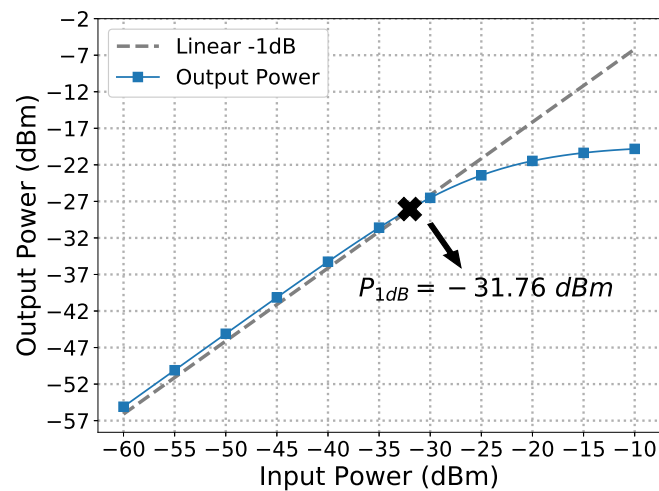


Figure 22: 1-dB compression point simulation for the post-layout of LNA and Buffer.

Source: Author

Figure 23 shows the results for two-tone simulations of the LNA and Buffer circuit showing third-order intercept point (IP3) results.

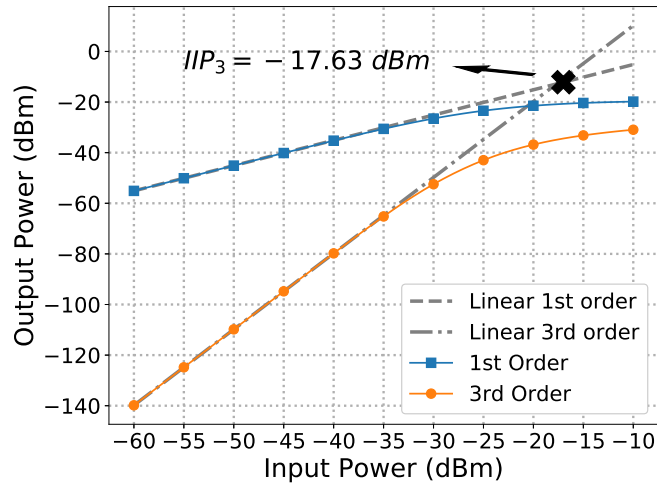


Figure 23:  $IIP_3$  results for the post-layout simulation of the LNA and Buffer circuit in 180nm CMOS technology.

Source: Author

Table 14 shows the performance specifications achieved after post-layout simulations.  $I_{DC}$  stands for the DC current from  $V_{DD}$  terminal to ground, and  $P_{DC}$  the power consumption achieved multiplying it by the supply  $V_{DD}$ .

$Re\{Z_{in}\}$  and  $Im\{Z_{in}\}$  represent the real and imaginary components of the input impedance  $Z_{in}$ , respectively.

Table 14: Performance obtained after post-layout simulations of the LNA and Buffer circuit.

Parameter	Value
Power Gain (S21) (dB)	8.5
Input Return Loss (S11) (dB)	-25
Noise Figure (dB)	8.8
1-dB Compression Point (dBm)	-31.76
$IIP_3$ (dBm)	-17.63
$I_{DC}$ (mA)	0.77
$P_{DC}$ (mW)	0.38
$Re\{Z_{in}\}$ ( $\Omega$ )	51.5
$Im\{Z_{in}\}$ ( $\Omega$ )	-0.58

After comparing the obtained results with the required specifications, the LNA and

Buffer circuit was fabricated using a 180nm CMOS technology.

### 3.1.4 Experimental results

Figure 24 shows the die micrograph after fabrication of the LNA and Buffer circuits in TSMC 180nm CMOS technology.

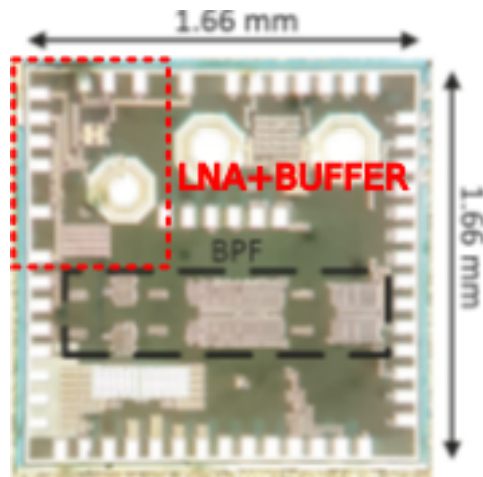


Figure 24: Die micrograph for the LNA and Buffer circuit.

Source: Author

The design of the PCB for testing the fabricated circuit followed the strategy describes at the beginning of this chapter. Figure 25 shows the schematic capture of the PCB design realized using Autodesk EAGLE software.

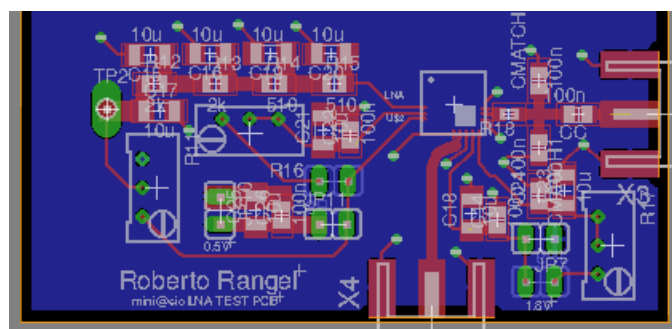


Figure 25: Schematic capture of the designed test PCB for the LNA and Buffer circuit on Autodesk EAGLE software.

Source: Author



Figure 26 shows the test PCB after fabrication. It is possible to observe the placement of the die, using chip-on-board technology. It is also shown the location of the passive network to perform the input matching.



Figure 26: Fabricated test PCB for the LNA and Buffer circuit.

Source: Author

The data was obtained using the Vector Network Analyzer (VNA) model HP8510B [21], which was calibrated for the ISM band, from 1.5 GHz to 3.5 GHz.

Figure 27 shows the Smith Chart plot for the input reflection ratio ( $S_{11}$ ) obtained with the data extracted from the measurement with the VNA. It shows that before applying the matching circuit, the impedance was distant of the desired 50 ohm for 2.4 GHz.

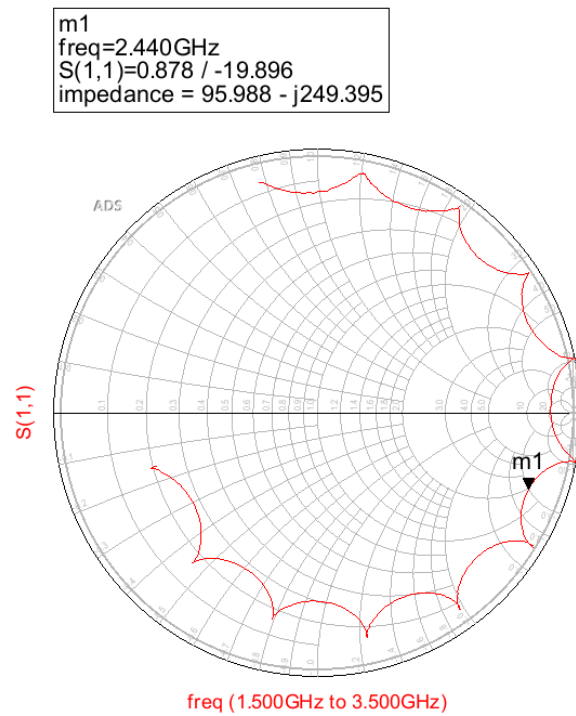


Figure 27: Smith Chart plot for S11 of experimental LNA and Buffer circuit.

Source: Author

Figure 28 shows the S-Parameters measurement results with data extracted from the measurements in the VNA. It is possible to see that the input reflection (S11) is fairly high for all the band, showing no match, therefore no selectivity. Also, the power gain (S21) shows no tuning in the output, probably due to lack of input matching.

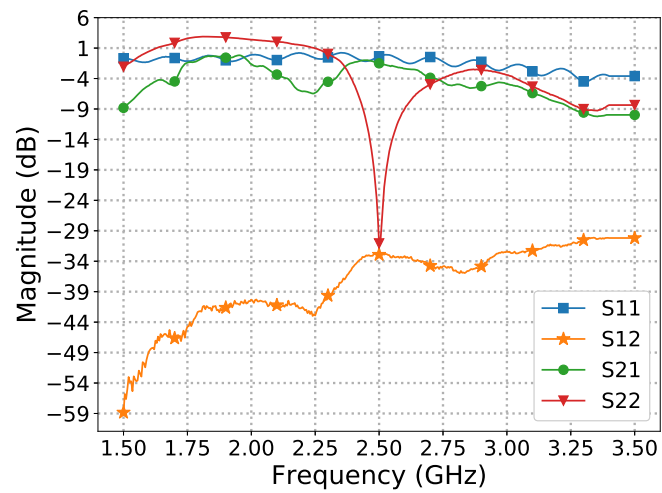


Figure 28: S-Parameter analysis of experimental LNA and Buffer circuit.

Source: Author

The extracted data was imported in the Keysight ADS software, as a way to design a proper input matching circuit. Figure 29 describe the matching procedure using LC elements. The procedure was performed using the Smith Chart Tool of Keysight ADS software. Starting from the impedance seen on the previous figure for the measured unmatched S11, the components were sized such that the final network could drive the input impedance seen at its input to  $50 \Omega$ .

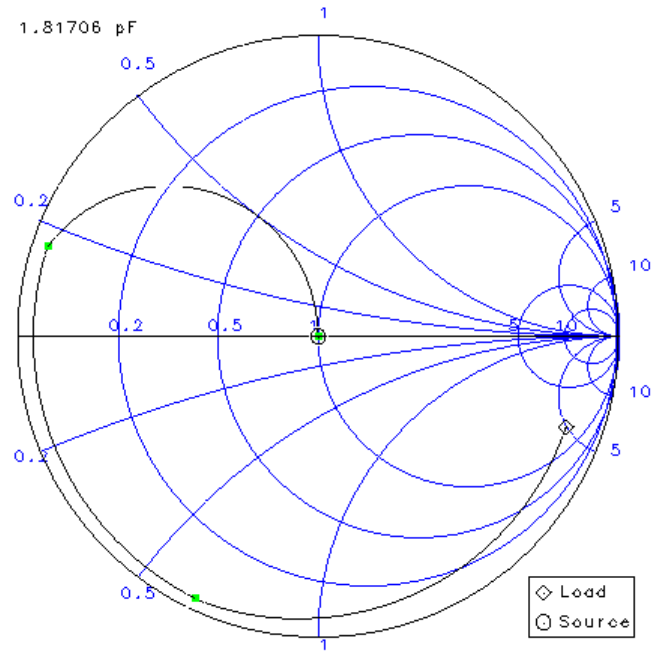


Figure 29: Impedance transformation performed after applying the designed matching circuit in simulation performed by the Smith Chart Tool in the Keysight ADS software using the data extracted from the measurements of the unmatched LNA and Buffer circuit.

Source: Author

Figure 30 describes the obtained LC network, in which the component values are described in the Table 15.

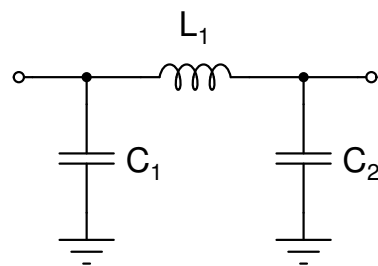


Figure 30: Designed ideal input matching circuit for the LNA and Buffer circuit.

Source: Author

Table 15: Sizing values for ideal input matching circuit for the measured LNA and Buffer circuit.

Parameter	Value
$L_1$	2.59 nH
$C_1$	7.79 pF
$C_2$	1.82 pF

Figure 31 shows the Smith Chart simulation for the input reflection ratio,  $S_{11}$ , using the designed ideal matching network and the experimental data extracted from the unmatched LNA and Buffer circuit.

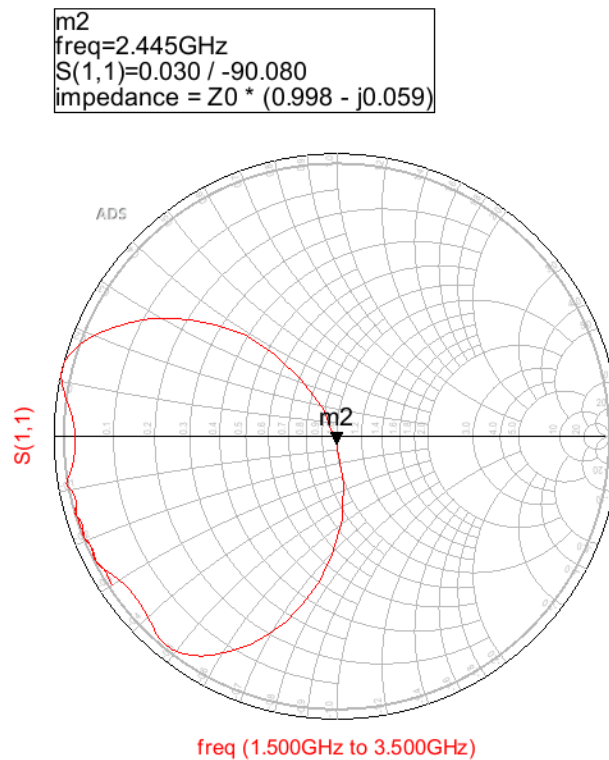


Figure 31: Smith chart plot for the simulation of experimental circuit data with designed input matching.

Source: Author

Figure 32 shows the S-Parameters results using the same configuration of ideal input matching and unmatched data from measurements of the LNA and Buffer.

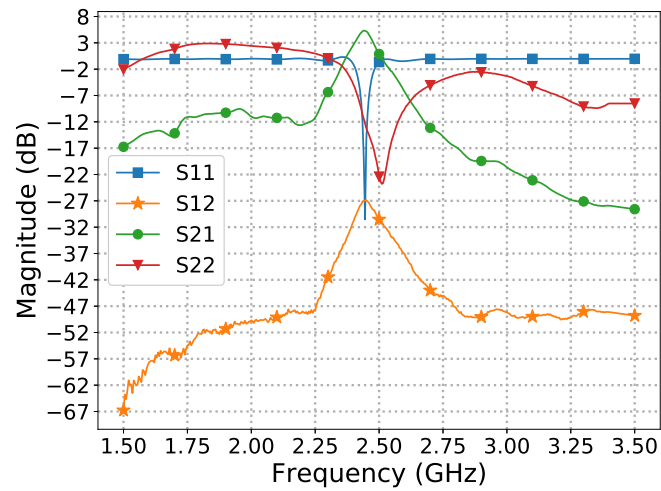


Figure 32: S-parameter simulation of experimental circuit data with designed input matching.

Source: Author

After the simulations using Keysight ADS, the values were rounded to a near commercial component value. With the adjusted component value, the input matching network was realized in the PCB. After adjustments in the PCB, the matching network elements were resized to better approximate the  $50 \Omega$  input impedance. The VNA was used to verify the input impedance. The final result of the measured LNA and Buffer circuit using the real input matching is shown in figure 33.

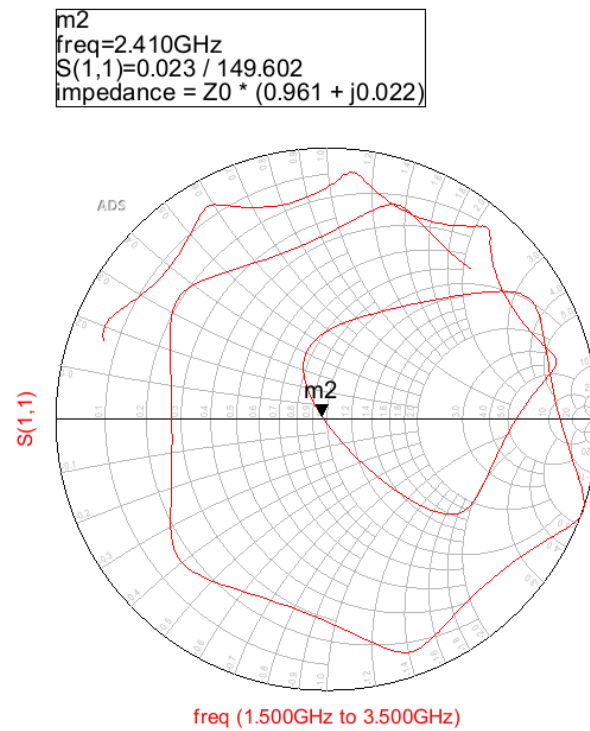


Figure 33: Smith Chart plot showing the measured S11 of the LNA and Buffer circuit with the real input matching circuit realized in the PCB.

Source: Author

Figure 34 shows the real input matching circuit, as realized in the PCB, after adjustments on the initial ideal network designed in the Keysight ADS.

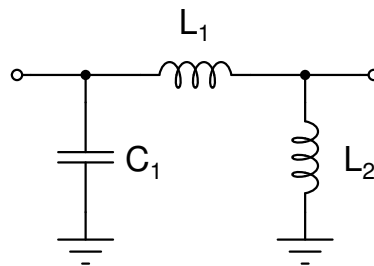


Figure 34: Input matching circuit after adjustments on PCB.

Source: Author

Table 16 shows the values of the commercial components used to implement the real input matching network in the PCB.

Table 16: Sizing values for implemented input matching circuit of 180nm LNA.

Parameter	Value
$L_1$	3.3 nH
$L_2$	1.8 nH
$C_1$	1 pF

Figure 35 shows the result for the S-Parameter measurement performed by the VNA in the LNA and Buffer circuit using the realized input matching circuit.

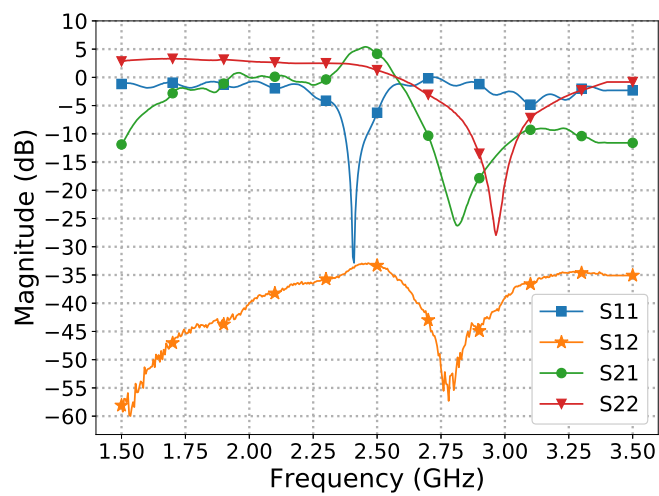


Figure 35: S-parameter simulation for the measured circuit with measured input matching.

Source: Author

Table 17 shows the performance specifications achieved in experimental circuit.

$Re\{Z_{in}\}$  and  $Im\{Z_{in}\}$  represent the real and imaginary components of the input impedance  $Z_{in}$ , respectively.



Table 17: Performance obtained in experimental circuit.

Parameter	Value
Power Gain (S21) (dB)	5.5
Input Return Loss (S11) (dB)	-33
$I_{DC}$ (mA)	0.45
$P_{DC}$ (mW)	0.23
$Re\{Z_{in}\}$	48.05
$Im\{Z_{in}\}$	1.1

## 3.2 Second Cascode common-source LNA in 180nm technology

After the first design and fabrication, the design was restarted as a way to review the previous circuit. This time the circuit gain was improved seeking to overcome the flaws on the previously measured circuit.

In the second design of LNA in 180nm design, a source-follower buffer was used for matching with  $50\Omega$  load. Although the gain will not be 0dB, a more stable biasing and output common-mode voltage are defined.

The gate inductor  $L_G$  is now integrated. It permits evaluating the variation from design to experimental results, and evaluate if it is worth to have it integrated instead of an off chip matching circuit.

This design also follow the specifications set on the start of the chapter, trying to improve the performance compared to the first design.

Figure 36 show the LNA and Buffer circuit in this second implementation.

The parasitic passive devices considered come from the bondwire, internal pad and PCB or package pins.  $R_{bw}$  and  $L_{bw}$  stand for the bondwire resistance and inductance, respectively.  $C_{pin}$  and  $C_{pad}$  represent the capacitance from off-chip connection and integrated pad, respectively.  $C_{pin}$  may receive capacitive contributions from package pins, when the die has a package, or solely PCB connection when chip-on-board connection is used. The parasitic devices from bondwires, pads and pins are present in connections between the integrated circuits and off-chip components. Those parasitic components are represented in the circuit by the impedance values  $Z_{par.in}$  and  $Z_{par.out}$ .

The resistors  $R_{bias}$  is placed to isolate the terminal  $V_{bias}$  of the RF signal. The terminal  $V_{bias}$  is responsible for setting the common-mode voltage at the gate of the input transistor  $M_1$  of the LNA.

$C_c$  and  $C_{c,int}$  capacitors perform the ac coupling between input source and LNA input pin, and between LNA output and Buffer input, respectively. The input matching network, responsible for controlling the LNA input impedance  $Z_{in}$ , is realized using inductor  $L_{match}$  and capacitor  $C_{match}$ .

Apart from the devices represented inside the rectangle with label "Integrated" and  $C_{pad}$ , all elements in the figure represent off-chip devices or parasitic entities.

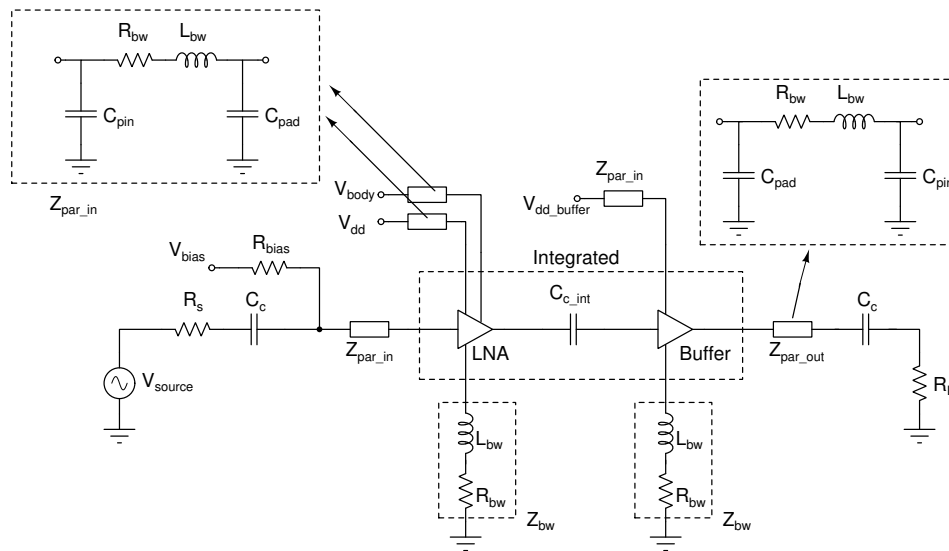


Figure 36: Circuit showing the implementation of the LNA and the Buffer circuit in 180nm technology.

Source: Author

Table 18: Device dimensions for the second LNA and Buffer design.

Parameter	Value
$R_s$	50 $\Omega$
$R_{bias}$	10 k $\Omega$
$R_{bw}$	1 $\Omega$
$L_{bw}$	1 nH
$C_{pin}$	100 fF
$C_{pad}$	100 fF
$C_c$	100 nF
$R_L$	50 $\Omega$
$V_{DD}$	0.5 V
$V_{DD.buffer}$	1.8 V

Figure 37 shows the LNA circuit, implementing the cascode common-source with inductive source degeneration topology, along with parasitic and external components.

$C_c$  and  $C_{c,int}$  capacitors perform the ac coupling between input source and LNA input pin, and between LNA output and Buffer input, respectively. The input matching network, responsible for controlling the LNA input impedance  $Z_{in}$  is realized using inductor  $L_{match}$  and capacitor  $C_{match}$ .

As with the LNA and the Buffer circuit, input match,  $Z_{par.in}$  and  $Z_{bw}$  represent off-chip devices or parasitic entities.

$C_L$  represents the load capacitance, in this case coming from the input of the Buffer stage.

$L_D$  act as a tuned load for the amplifier, and is designed to give the required gain, based on its embedded parallel resistance.

$C_D$  capacitor is part the output impedance of the circuit with  $L_D$  and  $C_L$ . It adjusts the value to give resonance in the center frequency of the band of interest.

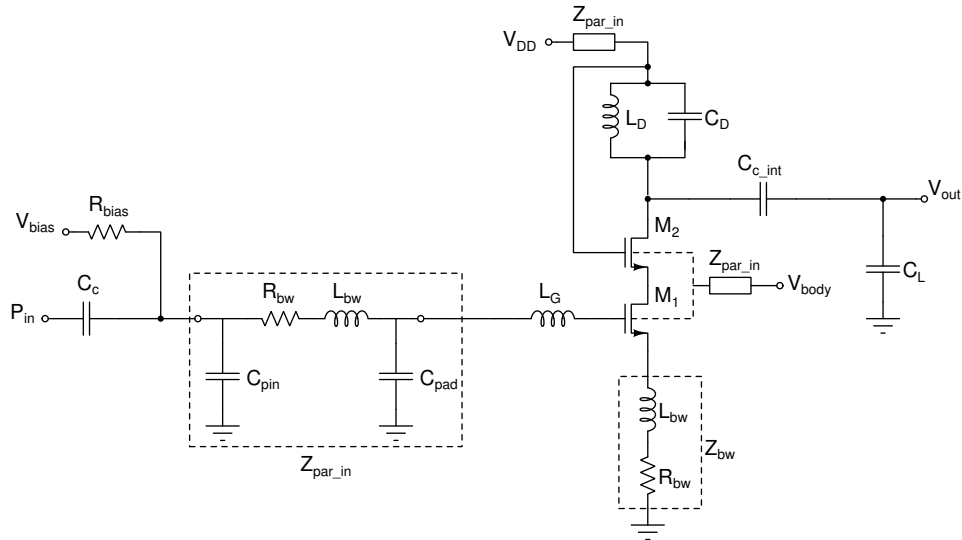


Figure 37: The second implementation of the cascode common-source LNA with inductive source degeneration circuit in 180nm CMOS technology, along with parasitic and other external devices.

Source: Author

Different from the first design, now for saving pins on the chip, the capacitor on the drain is chosen to be fixed. Otherwise, a pin is added to change the value of  $V_{body}$  biasing on transistor bulk terminal. Because of the suspicion that the voltage at the bulk caused undesired effects on the first design, it is added the possibility of changing it and observe the consequences.

The value of coupling capacitor between LNA and buffer,  $C_{c,int}$ , also changed as it was observed in the simulations that a smaller capacitor could be used without altering the coupling effects on the frequency band of interest.

The transistors are made bigger to increase gm and thus reduce noise and increase the gain. Also the load inductor  $L_D$  is made larger to help increasing the gain.

Table 19: Sizing values for second LNA 180nm.

Parameter	Value
$M_1, M_2$	144 $\mu m$ / 0.18 $\mu m$
$L_D$	3.9 nH
$C_D$	0.8 pF
$R_{bias}$	10 k $\Omega$
$C_{c.int}$	1.77 pF
$V_{body}$	0.5 V

Figure 38 shows the Buffer circuit, implementing the NMOS source follower topology, along with parasitic and external components. This topology is one of the most simple buffer implementations, giving predictable DC values and attenuation around 3 dB [44].

The parasitic devices in  $Z_{par.in}$  are the same described for the LNA and Buffer circuit.

The  $M_3$  drain voltage acts as common-mode reference to transistor  $M_1$ . Its drain voltage is defined by the relation of its aspect ratio,  $\frac{W}{L}$ ,  $R_1$  and  $V_{DD.buffer}$  at the desired DC current. And the current at  $M_3$  drain serve as reference for the output current biasing of the buffer, passing by  $M_1$  and  $M_2$  drain.

$C_c$  and  $C_{c.int}$  capacitors perform the ac coupling between Buffer output and output pin, and between LNA output and Buffer input, respectively.

As with the LNA and Buffer circuit, input match,  $Z_{par.in}$  and  $Z_{bw}$  represent off-chip devices or parasitic entities.

Transistor  $M_1$  and  $M_2$  are designed to give a gain near 0 dB with a 50  $\Omega$  load within the BLE frequency band.

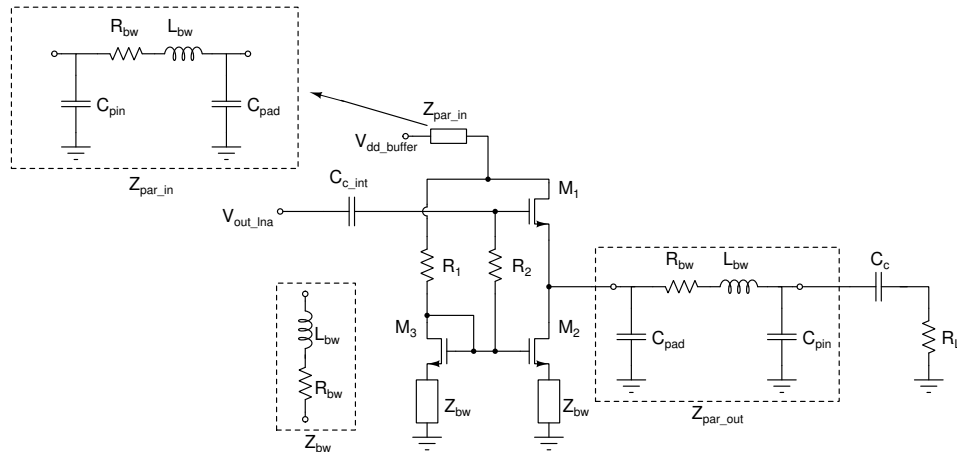


Figure 38: Circuit showing the Buffer circuit in 180nm technology, along with parasitic and other external devices.

Source: Author

The buffer topology was changed to a source follower to avoid problems with output common-mode voltage setting, reduce area and power consumed by the buffer. On the other hand, it is expected that the gain be reduced by 3 dB [44].

Table 20: Sizing values for second buffer 180nm.

Parameter	Value
$M_1$	$64 \mu m / 0.18 \mu m$
$M_2$	$6 \mu m / 0.18 \mu m$
$M_3$	$1.5 \mu m / 0.5 \mu m$
$R_1$	1 k $\Omega$
$R_2$	10.8 k $\Omega$

### 3.2.1 Schematic simulations

After circuit sizing, following the described design procedures, the schematic simulations were used to adjust the results. Figure 39 shows the results for scattering parameters (S-Parameters) simulation of the LNA.

The S21 parameter shows that the gain values are higher than the achieved in the first design. S11 parameter continues to show values below -15 dB for the frequencies of interest, as in the first design. The S22 and S12 parameters show a satisfactory behavior.

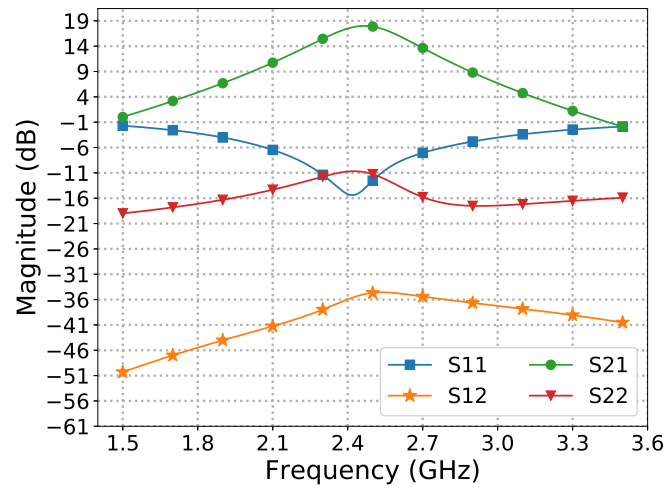


Figure 39: S-Parameter result for the schematic simulation of the second LNA circuit.

Source: Author

Following the simulations, Figure 40 shows the results for the noise figure simulation of the LNA. The result shows a satisfactory noise figure result, below 4 dB for the frequency range of interest.

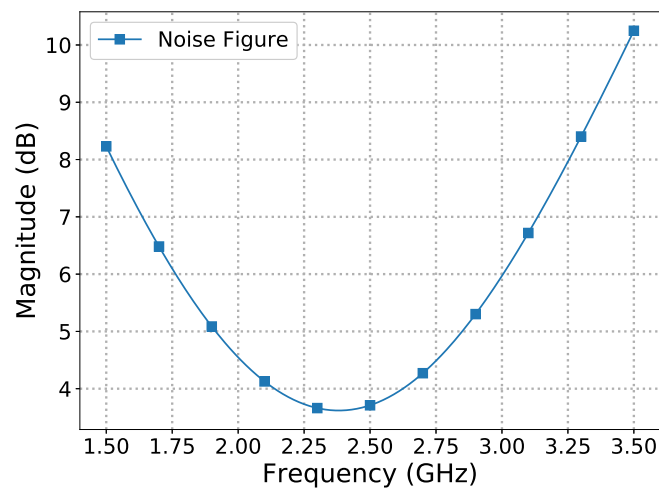


Figure 40: Noise Figure result for the schematic simulation of the second LNA circuit.

Source: Author

The linearity measures are performed using a two-tone test simulation [26]. The simulation results in the 1-dB Compression Point and  $IP_3$  curves. Figure 41 shows the results for the 1-dB compression point simulation of the LNA circuit. The 1-dB compression

point result is satisfactory comparing to the expected results.

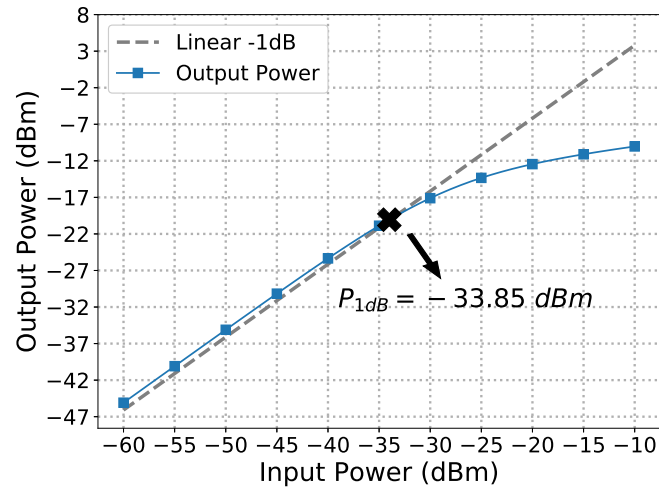


Figure 41: 1-dB compression point result for the schematic of LNA circuit.

Source: Author

Figure 18 shows the results for two-tone test simulation of the LNA showing third-order intercept point ( $IP_3$ ) results. The  $IIP_3$  result is satisfactory comparing to the expected results.

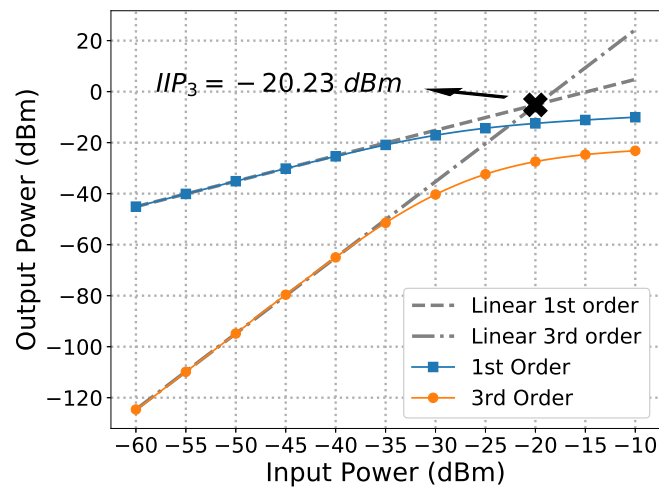


Figure 42:  $IIP_3$  result for the schematic simulation of the LNA circuit.

Source: Author

Table 21 shows the performance specifications achieved after schematic simulations.



Table 21: Performance obtained after schematic simulations.

Parameter	Value
Power Gain (S21) (dB)	18.6
Input Return Loss (S11) (dB)	-16
Noise Figure (dB)	3.2
1-dB Compression Point (dBm)	-33.85
$IIP_3$ (dBm)	-20.23
$I_{DC}$ (mA)	0.73
$P_{DC}$ (mW)	0.37
$Re\{Z_{in}\}$ ( $\Omega$ )	47.6
$Im\{Z_{in}\}$ ( $\Omega$ )	-21

After assuring that the results obtained match with the required specifications, the layout of the circuits is performed.

### 3.2.2 Layout

Figure 43 shows the layout for the LNA and the Buffer circuit, describing the specific blocks and the total size.

The layout comprises the integrated components shown during the design steps, where the drain ( $L_D$ ) and gate ( $L_G$ ) inductors are integrated. The resulting layout shows a dominance of the inductors in the area occupation.

To save area, no ESD protections are included, demanding careful handling during experimental tests.

Guardring protections are added in the RF transistors to reduce noise. Also, plenty of substrate connections are used, with the same objective.

Metal crossing is avoided to reduce cross coupling noise among metal levels. Each metal level is used either for vertical or horizontal connections, helping to reduce crossing area.

The layout was improved in this second implementation to increase the width of the ground and supply routing metal, reducing the parasitic resistance in the interconnections.

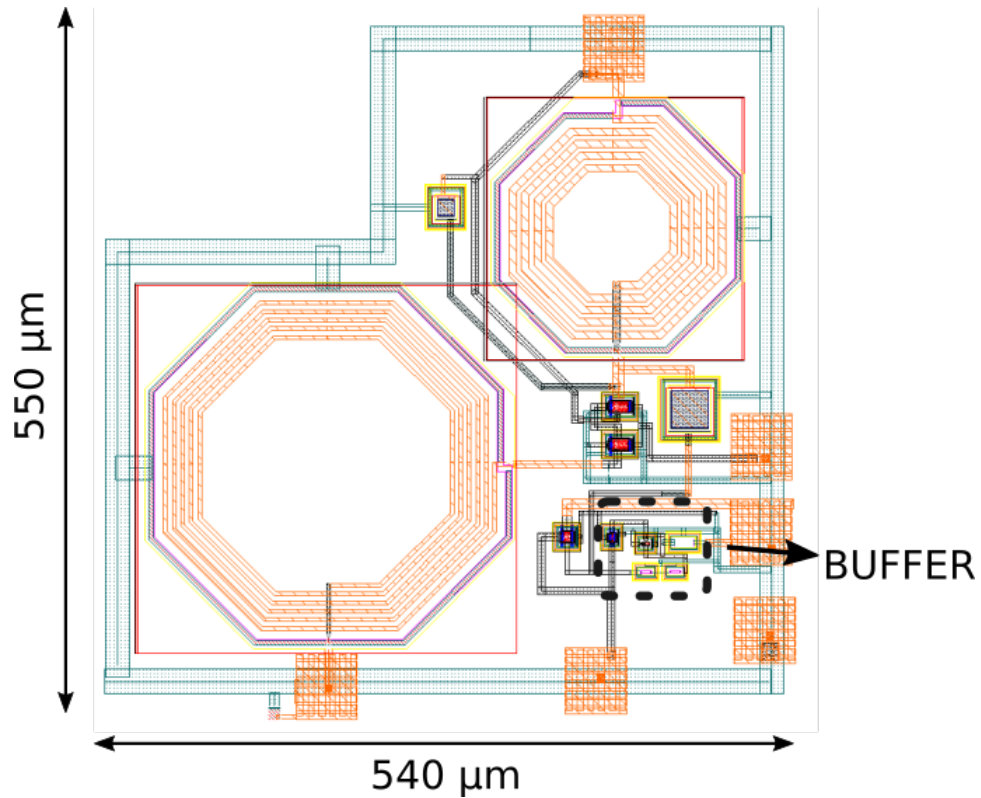


Figure 43: Layout for the second LNA and the Buffer circuit in 180nm CMOS technology.

Source: Author

### 3.2.3 Post layout simulations

After layout and parasitic extraction, the same tests were applied and the results adjusted and compared.

Figure 44 shows the results for scattering parameters (S-Parameters) simulation of the second LNA and Buffer circuit.

It is possible to observe that the post-layout of the second implementation is better comparing to the first one, and has a better proximity to the schematic simulations.

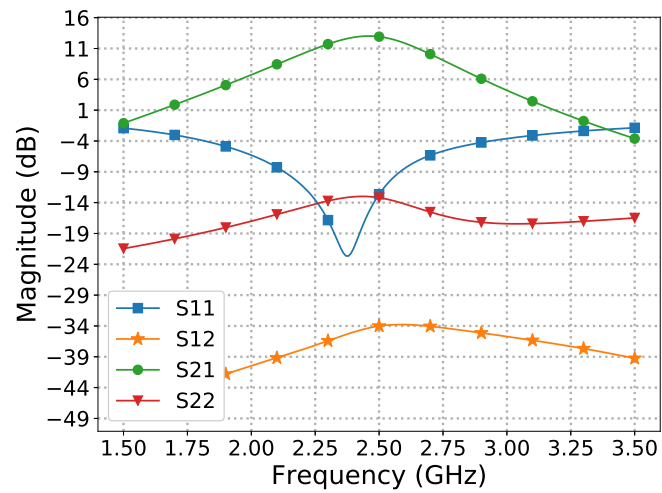


Figure 44: S-Parameter results for post-layout simulation of the second LNA and buffer circuit.

Source: Author

Figure 45 shows the results for noise figure simulation of the LNA and Buffer circuit. The degradation comparing to the schematic simulation was reduced, comparing to the first design.

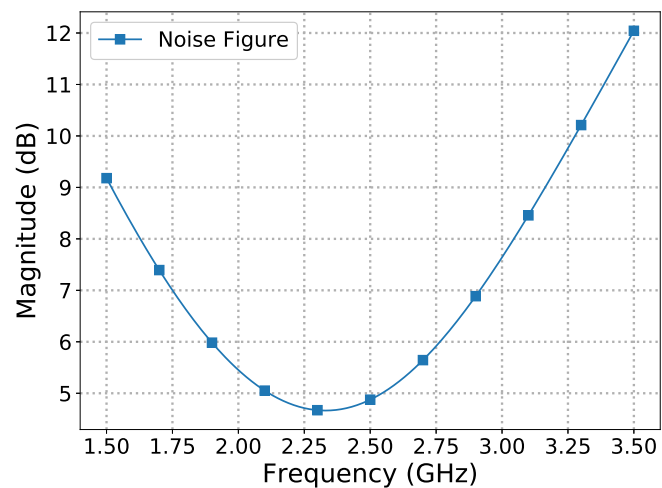


Figure 45: Noise Figure results for post-layout simulation of the second LNA and Buffer circuit.

Source: Author

Figure 46 shows the results for 1-dB compression point simulations of the LNA and

Buffer circuit.

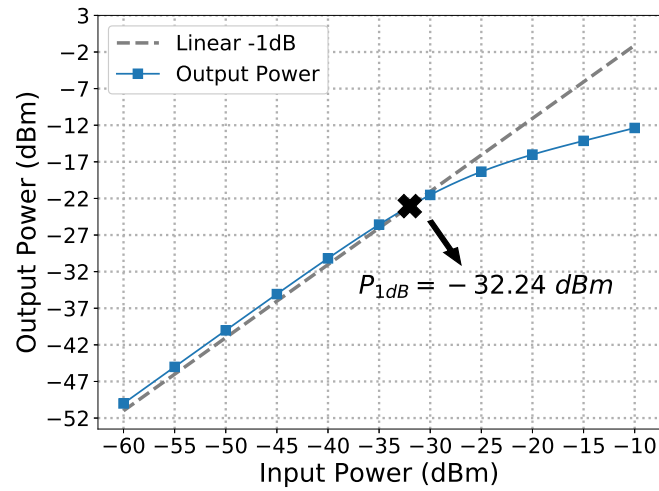


Figure 46: 1-dB compression point result for post-layout simulation of the second LNA and Buffer circuit.

Source: Author

Figure 47 shows the results for two-tone simulations of the LNA and Buffer circuit showing third-order intercept point (IP3) results.

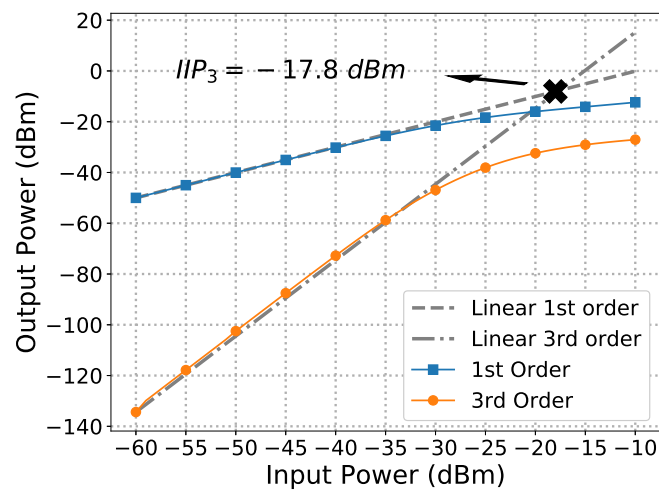


Figure 47: IIP3 result for post-layout simulation of the second LNA and buffer circuit.

Source: Author

Table 22 shows the performance specifications achieved after post-layout simulations.

Table 22: Summary of results obtained in post-layout simulations.

Parameter	Value
Power Gain (S21) (dB)	14
Input Return Loss (S11) (dB)	-23
Noise Figure (dB)	4
1-dB Compression Point (dBm)	-32.24
$IIP_3$ (dBm)	-17.8
$I_{DC}$ (mA)	0.69
$P_{DC}$ (mW)	0.34
$Re\{Z_{in}\}$ ( $\Omega$ )	40.3
$Im\{Z_{in}\}$ ( $\Omega$ )	2.27

After comparing the obtained results with the required specifications, the LNA and the Buffer circuit was fabricated using a 180nm CMOS technology.

### 3.2.4 Experimental results

Figure 48 shows the die micrograph after fabrication of the LNA and the Buffer circuit in TSMC 180nm technology.

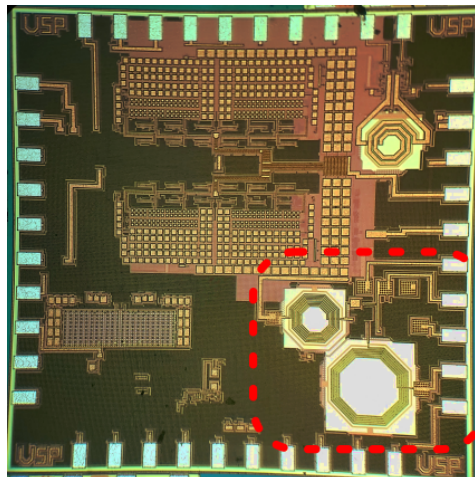


Figure 48: Die micrograph for the second LNA and Buffer circuit.

Source: Author

Figure 49 shows the resulting PCB for the tests with this second design. This time, the die is placed in a standard QFP44 package.

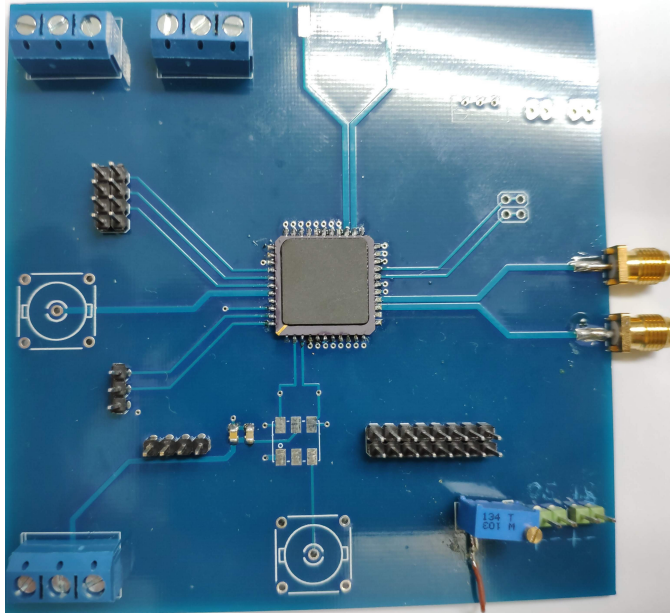


Figure 49: Fabricated test PCB for the second LNA and Buffer circuit.

Source: Author

The experimental data was obtained using the Vector Network Analyzer (VNA) model HP8510B [21], which was calibrated for the ISM band, from 1.5 GHz to 3.5 GHz. S-parameter data were obtained using VNA equipment and passed to Keysight ADS through S2P file for analysis and visualization.

Figure 50 shows the Smith Chart plot for the input reflection ratio ( $S_{11}$ ) obtained with the data extracted from the measurement with the VNA. It shows that the matching results are better than in the first design, due to the integrated  $L_G$  used in this second design. However, the input impedance is still distant from the optimal  $50 \Omega$  value.

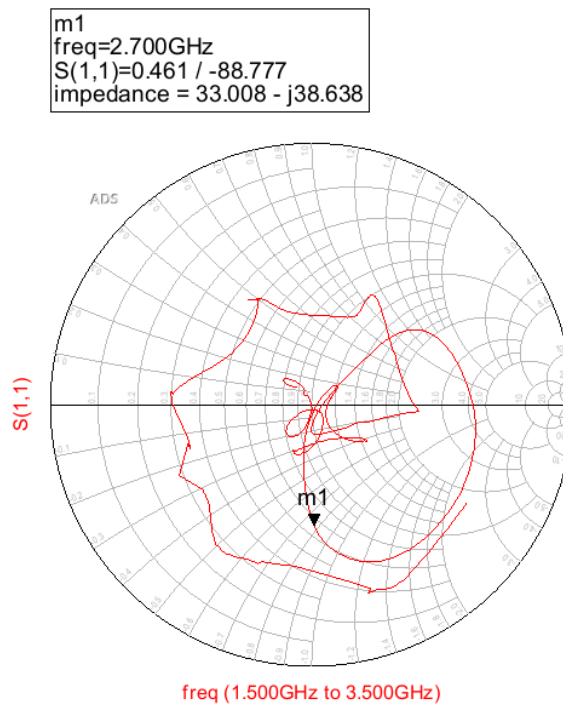


Figure 50: Smith Chart plot for S11 of experimental measurement of the second LNA and Buffer circuit.

Source: Author

Figure 51 shows the S-Parameter results with data extracted from the measurements in the VNA. The input reflection results shows a matching at the frequency of interest. However, it is not very selective, which may be due to imperfections on the transmission line calculations performed during the PCB design.

The power gain (S21) shows a tuning behavior and a higher gain than the experimental data for the first design. However, the tuning is displaced from the frequency of interest. Unfortunately, in this design the LC tank capacitor  $C_D$  is not variable, not allowing the adjustment of the resonating frequency of the S21.

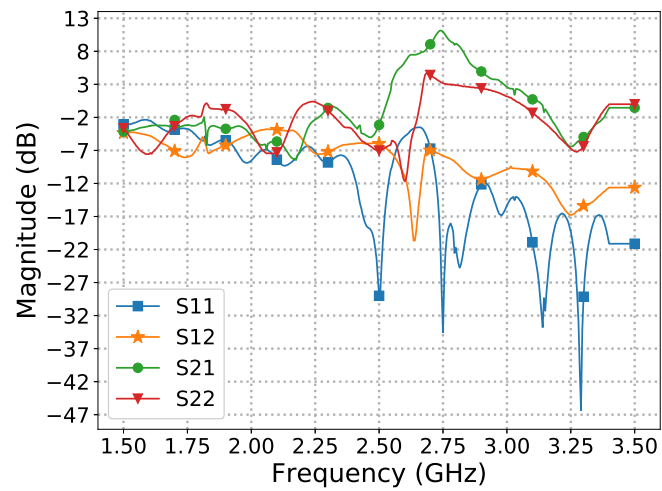


Figure 51: S-parameter results for experimental measurement of the second LNA and Buffer circuit.

Source: Author

The VNA data was imported in the Keysight ADS software to analyze how the response would get enhanced applying an input matching circuit. A procedure similar to the performed with the first design was realized. Figure 52 shows the procedure of using a LC network to drive the input impedance towards the optimal  $50 \Omega$  value.



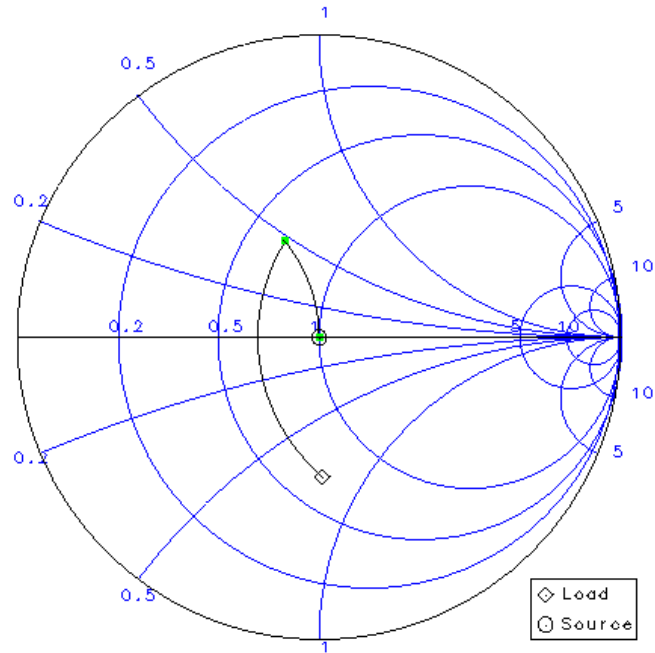


Figure 52: Impedance transformation performed by the Smith Chart Tool in the Keysight ADS software using the data extracted from the measurements of the second LNA and Buffer circuit.

Source: Author

Figure 53 shows the resulting ideal input matching circuit, and Table 23 the device values.

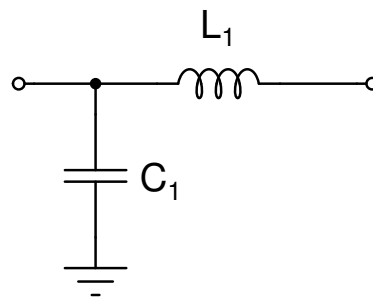


Figure 53: Designed ideal input matching circuit for the second LNA and Buffer circuit.

Source: Author

Table 23: Sizing values for ideal input matching circuit for the measured second LNA and Buffer circuit.

Parameter	Value
$L_1$	3.67 nH
$C_1$	0.85 pF

Figure 54 shows the Smith Chart simulation for the input reflection ratio,  $S_{11}$ , using the designed ideal matching network and the experimental data extracted from the second LNA and Buffer circuit.

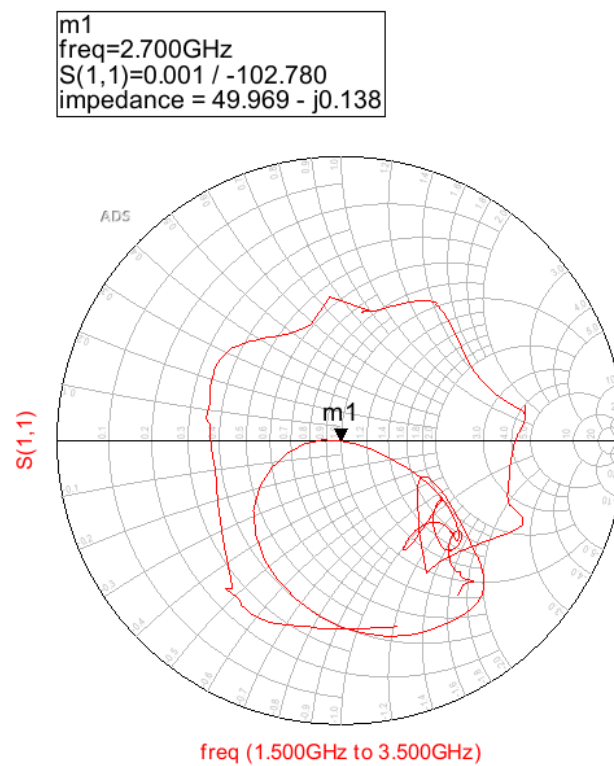


Figure 54: Smith chart plot for the simulation of experimental circuit data with designed input matching.

Source: Author

Figure 55 shows the S-Parameters results using the same configuration of ideal input matching and data from measurements of the second LNA and Buffer.

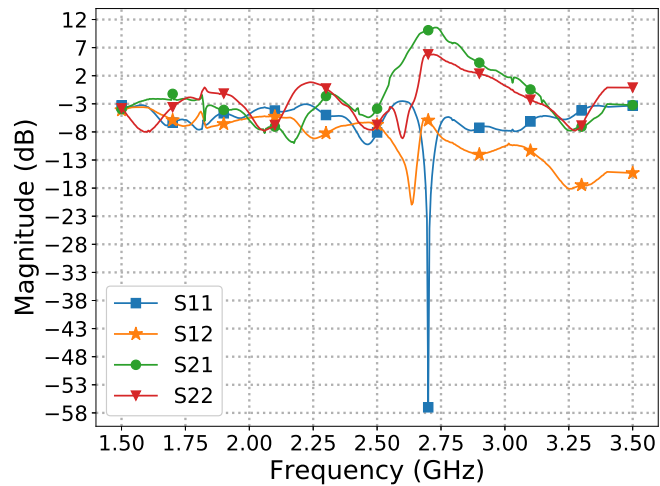


Figure 55: S-parameter simulation of experimental circuit data with designed input matching.

Source: Author

The results show that the input matching circuit would help to adjust the input matching response, reducing the effect of the PCB imperfections. Unfortunately, the PCB for the second design does not include the pad connections for the implementation of the input matching circuit, making it difficult to implement the real matching circuit.

Table 24 shows the performance specifications achieved in experimental circuit.

Despite the higher power consumption, it has a better band tuning and higher gain than the first tapeout. As the capacitor at the drain terminal could not be controlled, the resonating frequency could not be adjusted and showed a center frequency higher than the desired of 2.44 GHz.

Table 24: Summary of results obtained in experimental circuit.

Parameter	Value
Power Gain (S21) (dB)	11
Input Return Loss (S11) (dB)	-58
$I_{DC}$ (mA)	0.7
$P_{DC}$ (mW)	0.35

### 3.3 RF Front-end design in 130nm BiCMOS technology

The third implementation extends the previous fabricated designs by including the complete RF Front-End structure. This design uses a 130nm BiCMOS technology from GlobalFoundries. The first two LNA designs contributed with information regarding the LNA behavior at Low Voltage operation, and also showed the possible parameter variations in the experimental results.

helped to learn the behavior of the LNA, and the divergence of the experimental results compared to the simulations.

This design includes the cascode common-source LNA with inductive degeneration, a single-balanced passive sampling mixer, a simple common-source IF amplifier with resistive load, and a common-source buffer with resistive load.

The common-source buffer has been chosen to try to avoid the attenuation experienced when using a source follower. Different from the first one used, now a resistor load is used to help defining the output common-mode voltage.

In this technology, the lower  $V_{TH}$  values allowed the implementation without the need of  $V_{TH}$  reducing techniques like the FBB implemented in the previous designs.

Table 25 shows the simulated  $f_T$  response as a function of the channel length for a nMOS transistor, the same used for the input stage of the amplifiers in this design. The results show that the  $f_T$  holds satisfactory values in the presented channel length range, therefore making unnecessary the use of FBB.

Table 26 shows the simulated threshold voltage response as a function of the channel length for a nMOS transistor. Again, the results show  $V_{TH}$  values matching the design needs.

Table 25: Transfer frequency response as a function of the nMOS transistor channel length.

$L(nm)$	120	150	200	250	300	400
$f_T(GHz)$	125	90	50	30	20	11

Table 26: Threshold voltage response as a function of the nMOS transistor channel length.

$L(nm)$	120	150	200	250	300	400
$V_{TH}(V)$	0.4	0.37	0.33	0.31	0.3	0.29

Figure 56 shows the RF Front-End circuit along with the IF amplifier and Buffer.

The parasitic passive devices considered come from the bondwire, internal pad and PCB or package pins.  $R_{bw}$  and  $L_{bw}$  stand for the bondwire resistance and inductance, respectively.  $C_{pin}$  and  $C_{pad}$  represent the capacitance from off-chip connection and integrated pad, respectively.  $C_{pin}$  may receive capacitive contributions from package pins, when the die has a package, or solely PCB connection when chip-on-board connection is used. The parasitic devices from bondwires, pads and pins are present in connections between the integrated circuits and off-chip components. Those parasitic components are represented in the circuit by the impedance values  $Z_{par\_in}$  and  $Z_{par\_out}$ . The resistors  $R_{bias}$  adjust the reference current  $I_{bias}$  biasing the LNA and Buffer circuits.  $C_c$  and  $C_{c\_int}$  capacitors perform the ac coupling between input source and LNA input pin, and between LNA output and Buffer input, respectively. The input matching network, responsible for controlling the LNA input impedance  $Z_{in}$  is realized using inductor  $L_{match}$  and capacitor  $C_{match}$ .

Apart from the devices represented inside the rectangle with label "Integrated" and  $C_{pad}$ , all elements in the figure represent off-chip devices or parasitic entities.

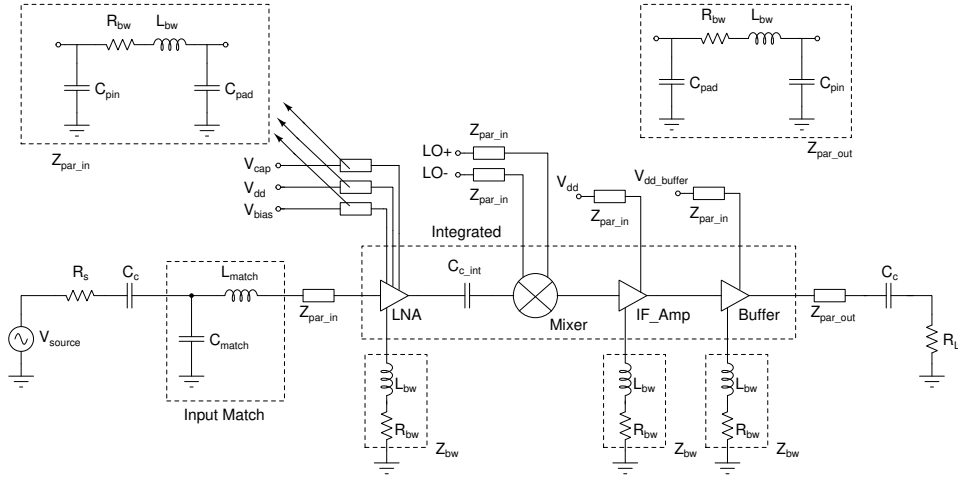


Figure 56: The implemented RF Front-End, common-source IF amplifier with resistive load and common-source Buffer with resistive load circuits in 130nm BiCMOS technology.

Source: Author

Table 27 describe the values of the devices included in this design.

Table 27: Device dimensions for the Front-End, IF Amplifier and Buffer circuit in 130nm CMOS technology.

Parameter	Value
$R_s$	50 $\Omega$
$L_{match}$	6.55 nH
$C_{match}$	2.5 pF
$R_{bw}$	1 $\Omega$
$L_{bw}$	1 nH
$C_{pin}$	100 fF
$C_{pad}$	100 fF
$C_c$	100 nF
$C_{c.int}$	10 pF
$R_L$	50 $\Omega$
$V_{DD}$	0.5 V
$V_{DD.buffer}$	1.2 V

Figure 57 shows the LNA circuit, implementing the cascode common-source with inductive source degeneration topology, along with parasitic and external components.

As with the first design in the 180nm CMOS technology, this implementation includes a variable capacitor device for the capacitor  $C_D$  in the LC tank, making possible to adjust its resonating frequency. The source inductor is not included in the integrated design, instead being represented by the bondwire inductance in the source,  $L_{bw}$ . The gate inductor have also been removed from the integrated circuit and is rather implemented off-chip by the matching network inductor  $L_{match}$ .

The elements in the input match circuit and the parasitic devices in  $Z_{par.in}$  are the same described for the RF Front-End, IF Amplifier and Buffer circuit.

Transistor  $M_3$  drain voltage is defined by the sizing of  $M_3$  and the incoming  $I_{bias}$ , and set the input common-mode voltage of  $M_1$ . The resistor  $R_{bias}$  combined with  $M_3$  gate capacitance perform a low-pass filtering, avoiding signal leakage from the input node.

$C_c$  and  $C_{c.int}$  capacitors perform the ac coupling between input source and LNA input pin, and between LNA output and Buffer input, respectively. The input matching network, responsible for controlling the LNA input impedance  $Z_{in}$  is realized using inductor  $L_{match}$  and capacitor  $C_{match}$ .

As with the RF Front-End, IF Amplifier and Buffer circuit, the input match,  $Z_{par\_in}$  and  $Z_{bw}$  represent off-chip devices or parasitic entities.

$C_L$  represents the load capacitance, in this case coming from the input of the Buffer stage.

$L_D$  act as a tuned load for the amplifier, and is designed to give the required gain, based on its embedded parallel resistance.

$C_D$  capacitor is part the output matching of the circuit with  $L_D$  and  $C_L$ . It adjusts the value to give resonance in the center frequency of the band of interest.

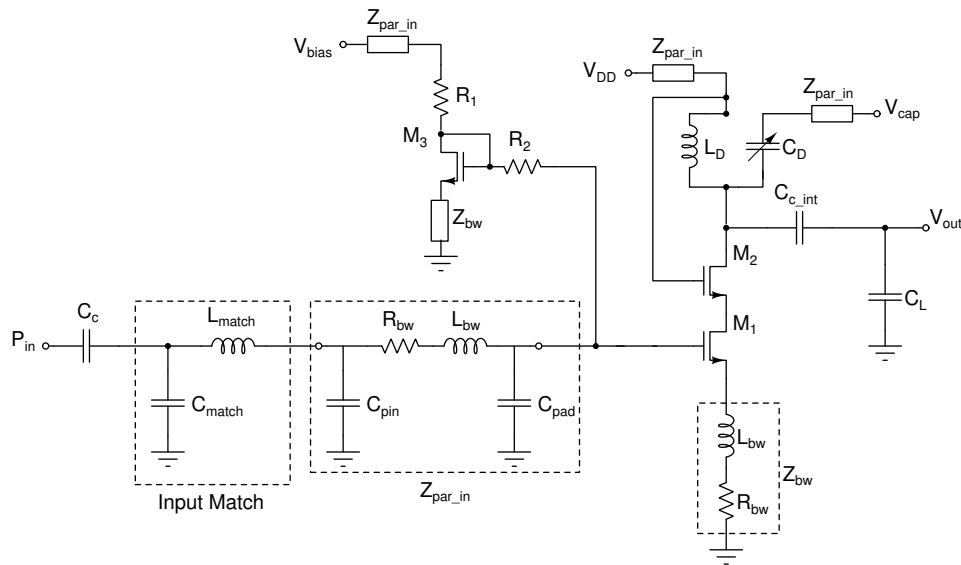


Figure 57: The implemented circuit of the cascode common-source LNA with inductive source degeneration block in 130nm BiCMOS technology.

Source: Author

Table 28 describe the values of the devices included in this design.

Table 28: Device dimensions for the cascode common-source LNA with inductive source degeneration in 130nm BiCMOS technology.

Parameter	Value
$M_1, M_2$	100 $\mu m$ / 0.32 $\mu m$
$L_D$	2 nH
$C_D$	0.14 - 0.69 pF
$R_1$	10 k $\Omega$
$R_2$	10 k $\Omega$
$C_{c.int}$	10 pF

Figure 58 shows only the single-balanced passive sampling Mixer circuit along with parasitic and external components.

The parasitic devices in  $Z_{par.in}$  are the same described for the Front-End, IF Amplifier and Buffer circuit.

The  $M_3$  drain voltage acts as the input common-mode voltage  $V_{CM}$  of the Mixer. Its drain voltage is defined by the relation of its aspect ratio,  $\frac{W}{L}$ ,  $R_1$  and  $V_{DD\_buffer}$  at the desired DC current. The voltage  $V_{CM}$  will also represent the input common-mode voltage of the IF Amplifier stage, at the  $V_{out+}$  and  $V_{out-}$  pins seen in the Figure 58

The design procedure for the Mixer, accounting for the  $V_{CM}$  definition, bandwidth and noise considerations, follows the strategy proposed in the methodology chapter of this work.

$C_c$  and  $C_{c.int}$  capacitors perform the AC coupling between Buffer output and output pin, and between LNA output and the Buffer input, respectively.

As with the Front-End, IF Amplifier and Buffer circuit, the input match,  $Z_{par.in}$  and  $Z_{bw}$  represent off-chip devices or parasitic entities.

Transistor  $M_1$  and  $M_2$  are designed to give a gain near to 0 dB with a 50  $\Omega$  load within the BLE frequency band.



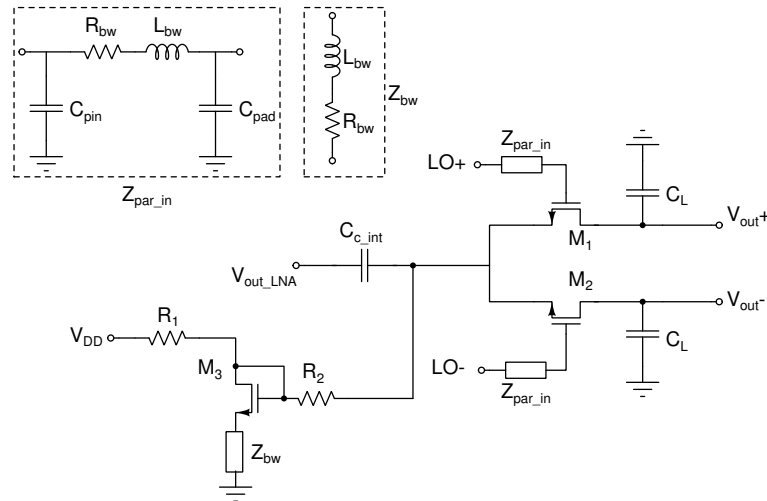


Figure 58: The implemented single-balanced passive sampling Mixer circuit in 130nm BiCMOS technology.

Source: Author

The values for the device dimensions implemented in the Mixer design are shown in Table 29.

Table 29: Device dimensions the single-balanced passive sampling Mixer in 130nm BiCMOS technology.

Parameter	Value
$M_1, M_2$	$192 \mu m / 0.32 \mu m$
$R_1$	11 k $\Omega$
$R_2$	11 k $\Omega$
$C_L$	300 fF

Figure 59 shows the common-source IF Amplifier with resistive load circuit. This simple amplifier topology is included to help increasing the circuit conversion gain, serving as an IF baseband amplifier. It uses resistive load to ease the design, relaxing the procedure for definition of the output common-mode voltage.

The parasitic devices in  $Z_{par\_in}$  are the same described for the RF Front-End, IF Amplifier and Buffer circuit.

The  $R_D$  resistors represent the load of the common-source IF Amplifier.

$C_c$  and  $C_{c\_int}$  capacitors perform the ac coupling between Buffer output and output



As with the LNA and Buffer circuit, input match,  $Z_{par\_in}$  and  $Z_{bw}$  represent off-chip devices or parasitic entities.

Transistor  $M_1$  and  $M_2$  are designed to have gain near 0 dB with a  $50 \Omega$  load within the BLE frequency band. Resistors  $R_D$  are designed to show an optimal matching with external  $50 \Omega$  resistance, representing the input impedance of the test equipment.

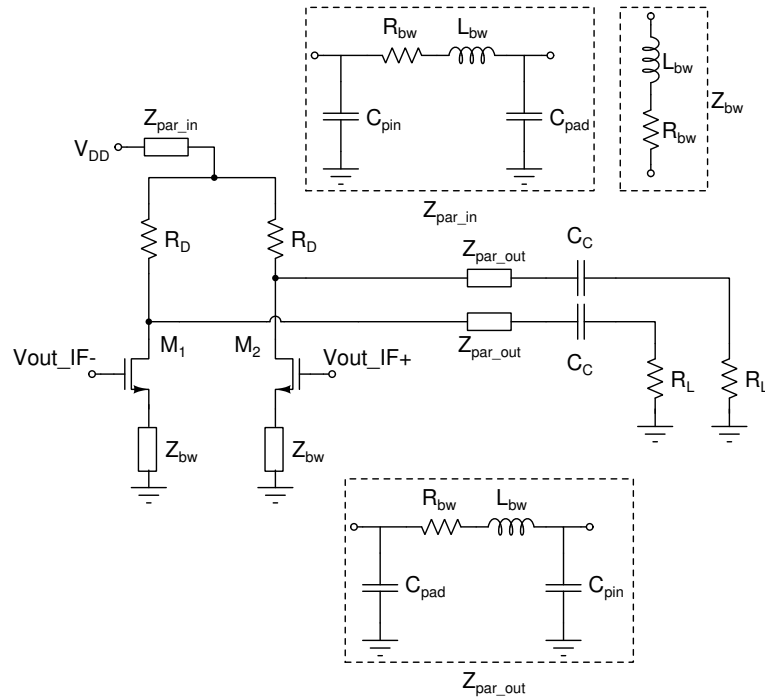


Figure 60: The implemented common-source Buffer with resistive load circuit in 130nm BiCMOS technology.

Source: Author

The resulting dimensions for the common-source Buffer with resistive load circuit are shown in Table 31.

Table 31: Device dimensions for the common-source Buffer with resistive load in 130nm BiCMOS technology.

Parameter	Value
$M_1, M_2$	$960 \mu m / 1 \mu m$
$R_D$	$50 \Omega$

### 3.3.1 Schematic simulations

After circuit sizing, following the described design procedures, the schematic simulations were used to adjust the results. Figure 61 shows the results for scattering parameters (S-Parameters) simulation of the common-source LNA with inductive source degeneration.

The S21 parameter represents the power gain of the circuit, and shows that it meets the specifications for gain magnitude and frequency tuning. S11 parameter shows the input insertion loss, and shows a value below -15 dB for the frequencies of interest.

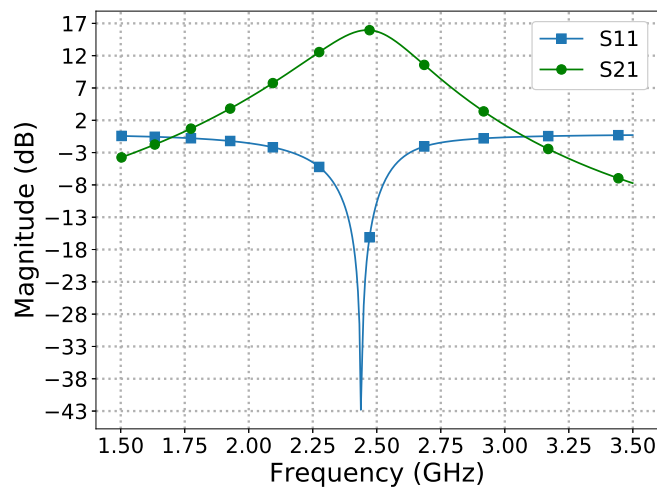


Figure 61: S-Parameter results for the schematic simulation of the common-source LNA with inductive source degeneration in 130nm BiCMOS technology.

Source: Author

Following the simulations, Figure 62 shows the results for the Noise Figure simulation of the common-source LNA with inductive source degeneration. The result shows a satisfactory noise figure result, below 4 dB for the frequency range of interest.

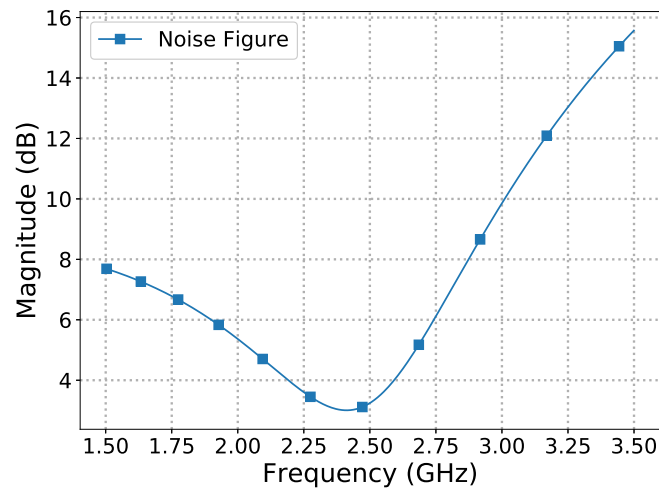


Figure 62: Noise Figure result for the schematic simulation of the common-source LNA with inductive source degeneration in 130nm BiCMOS technology.

Source: Author

Table 32 shows the performance specifications achieved after schematic simulations.  $I_{DC}$  stands for the DC current from  $V_{DD}$  terminal to ground, and  $P_{DC}$  the power achieved multiplying it by the supply  $V_{DD}$ .

Table 32: Summary of performance obtained in the LNA after schematic simulations.

Parameter	Value
Power Gain (S21) (dB)	17
Input Return Loss (S11) (dB)	-43
Noise Figure (dB)	3
$I_{DC}$ (mA)	0.38
$P_{DC}$ (mW)	0.19

### 3.3.2 Post-Layout simulations of the LNA circuit

After assuring that the results obtained match with the required specifications, the layout of the LNA circuit was performed, intending to realize the parasitic extractions,

After layout and parasitic extraction, the same tests were applied and the results adjusted and compared.

Figure 63 shows the results for scattering parameters (S-Parameters) simulation of

the LNA circuit.

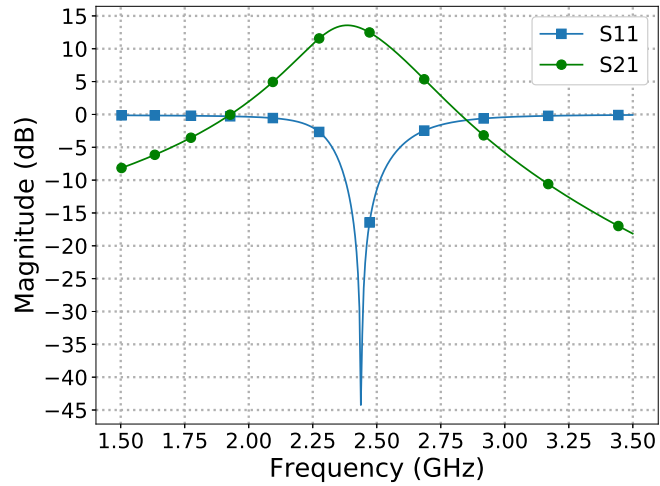


Figure 63: S-Parameter result for the post-layout simulation of the common-source LNA with inductive source degeneration in 130nm BiCMOS technology.

Source: Author

Figure 64 shows the results for noise figure simulation of the LNA and Buffer circuit.

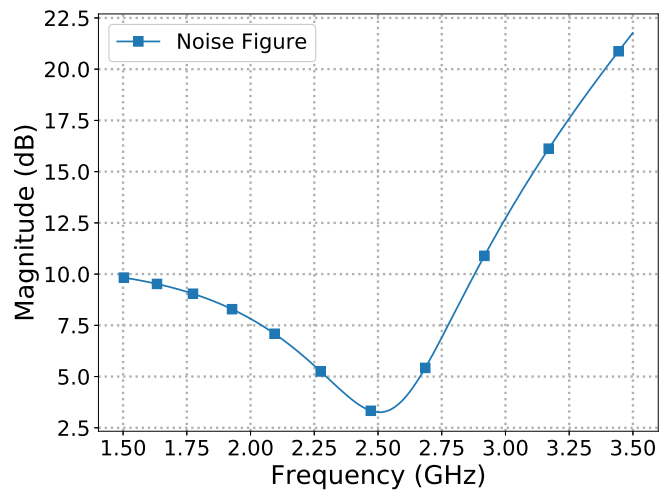


Figure 64: Noise Figure result for the post-layout simulation of common-source LNA with inductive source degeneration in 130nm BiCMOS technology.

Source: Author

Figure 65 shows the results for 1-dB compression point simulations of the LNA circuit.

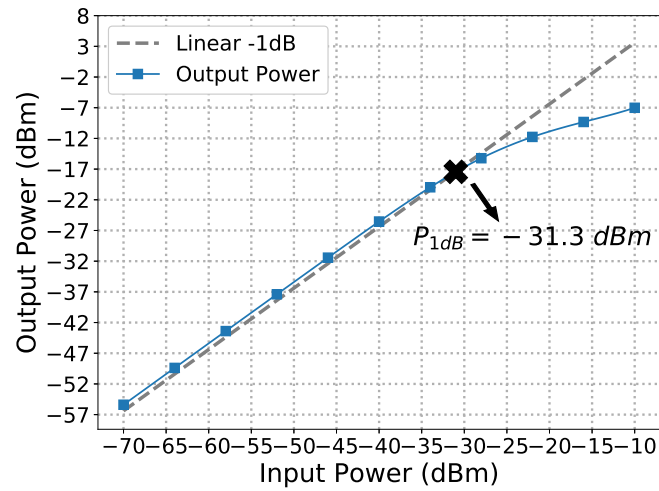


Figure 65: 1-dB compression point result for the post-layout simulation of the common-source LNA with inductive source degeneration in 130nm BiCMOS technology.

Source: Author

Figure 66 shows the results for two-tone simulations of the LNA circuit showing third-order intercept point (IP3) results.

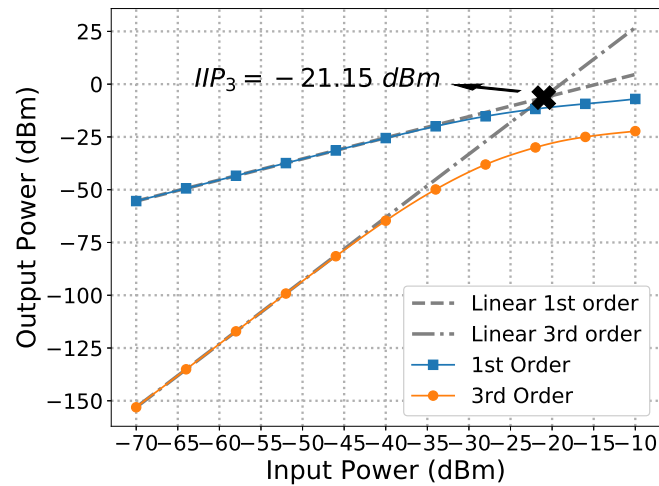


Figure 66: IIP3 result for the post-layout simulation of the common-source LNA with inductive degeneration in 130nm BiCMOS technology.

Source: Author

## 3.4 Front-end

Because of the impact of the interface impedance, rather than performing the Mixer design alone, after the LNA design, the complete RF Front-End design was performed.

### 3.4.1 Layout

The fact of being a BiCMOS technology instead of a conventional CMOS make the MOSFETs more susceptible to latch-up errors. Therefore, the layout implementation is hardened with more carefully designed substrate connections, also including reverse biased diodes to avoid latch-up.

Figure 67 shows the layout for the RF Front-End, IF Amplifier and Buffer circuit, describing the specific blocks and the total size. Despite of having more implemented blocks, the fact of using a technology with shorter minimum channel length resulted in a layout with less area.



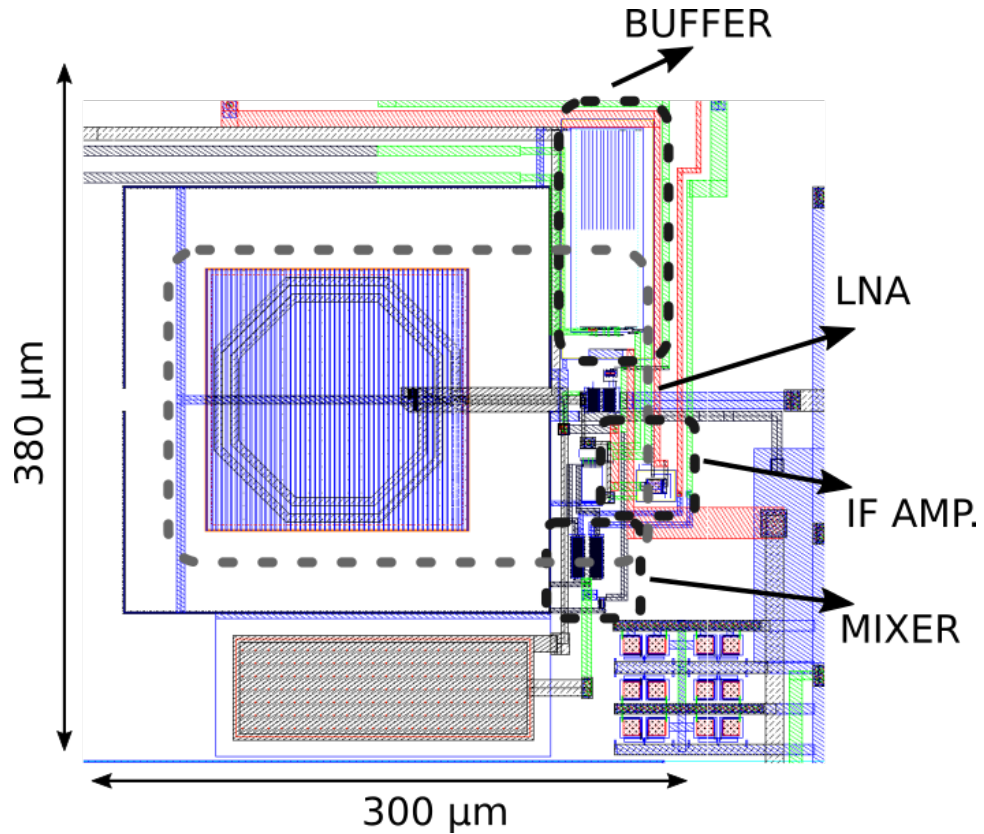


Figure 67: Layout for the RF Front-End, IF Amplifier and Buffer circuit in 130nm BiCMOS technology.

Source: Author

### 3.4.2 Post layout simulations

The following results present the post-layout simulation performance of the RF Front-End, IF Amplifier and Buffer circuit.

Figure 68 shows the conversion gain result for a RF signal with 2.44 GHz at the input, and IF in the range of zero to 5 MHz at the output of the Buffer.

The result shows that the circuit presents a satisfactory conversion gain for the required IF of 2 MHz, even if it is in the presence of attenuation from the Buffer circuit.

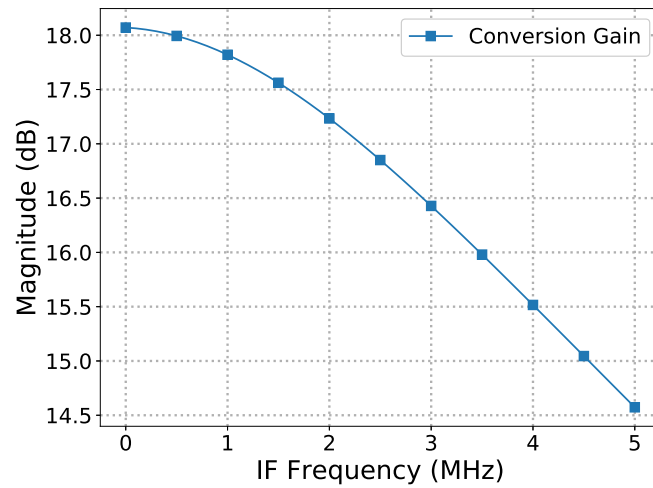


Figure 68: Conversion gain result for the post-layout simulation of the RF Front-End, IF Amplifier and Buffer circuit for a 2.44 GHz input in 130nm BiCMOS technology.

Source: Author

Figure 69 shows the results for noise figure simulation of the RF Front-End, IF Amplifier and Buffer circuit. The result show a high noise value, near the maximum 20 dB value considered. Thus, implying that the noise figure should be reduced in the blocks after the LNA. Moreover, the LNA gain can be increased as an approach to reduce the overall noise figure.

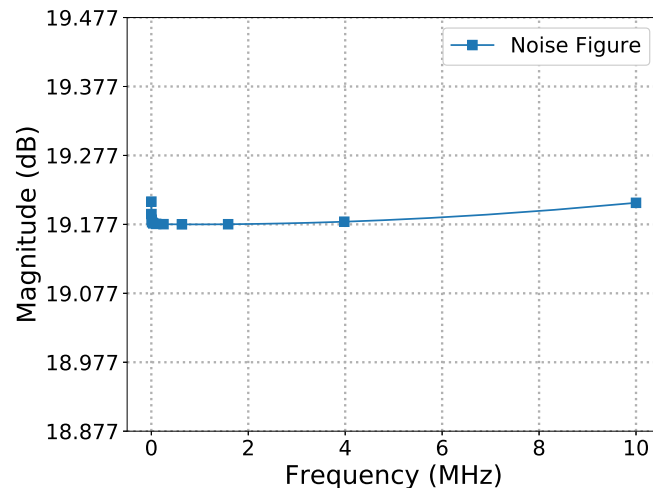


Figure 69: Noise Figure post-layout simulation of LNA and Mixer for a 2.44 GHz input in 130nm technology.

Source: Author

Figure 70 shows the results for 1-dB compression point simulations of the RF Front-End, IF Amplifier and Buffer circuit. The result matches with the required linearity response for the implemented circuit.

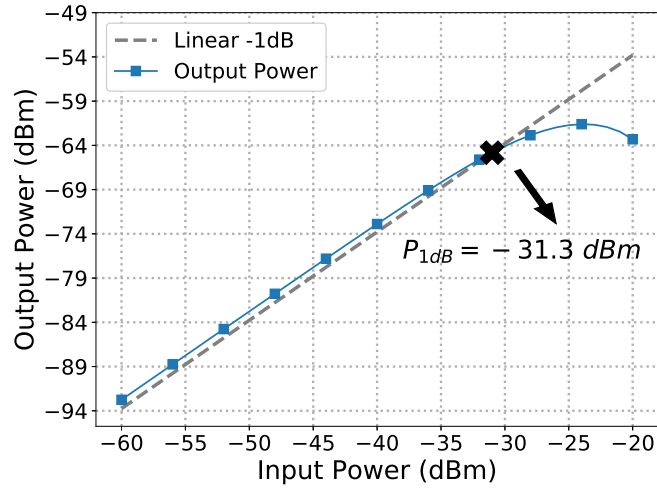


Figure 70: 1-dB compression point result for the post-layout simulation of the RF Front-End, IF Amplifier and Buffer in 130nm BiCMOS technology.

Source: Author

Figures 71, 72 and 73 show the results for the signal feedthrough analysis, standing for the RF to IF port leakage, LO to IF port leakage, and LO to RF port leakage, respectively. The results indicate a low leakage level among the ports.

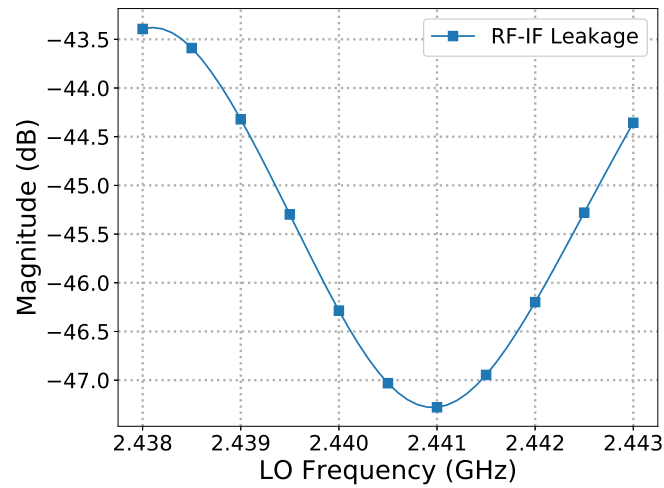


Figure 71: Leakage signal result from RF to IF port for the post-layout simulation of RF Front-End, IF Amplifier and Buffer circuit in 130nm BiCMOS technology.

Source: Author

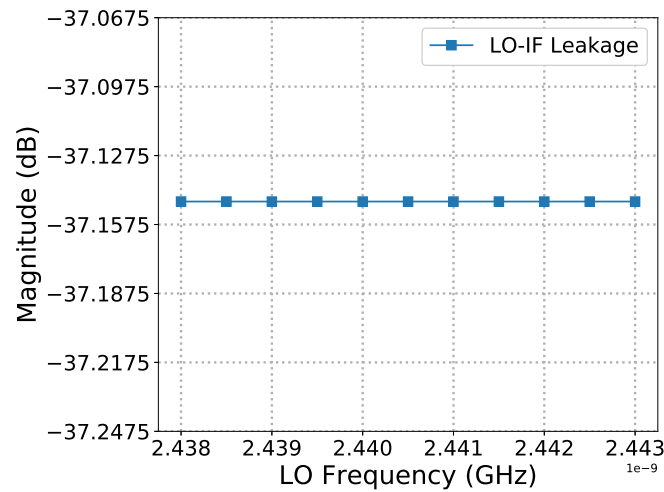


Figure 72: Leakage signal result from LO to IF port for the post-layout simulation of RF Front-End, IF Amplifier and Buffer circuit in 130nm BiCMOS technology.

Source: Author

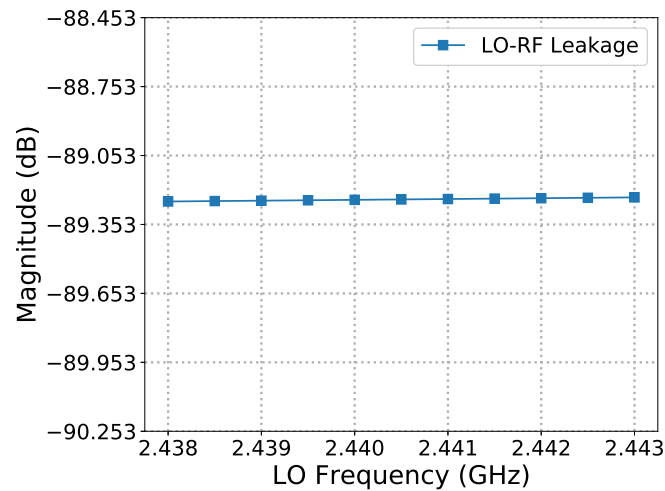


Figure 73: Leakage signal result from LO to RF port for the post-layout simulation of RF Front-End, IF Amplifier and Buffer circuit in 130nm BiCMOS technology.

Source: Author

Table 33 shows the performance specifications achieved after the post-layout simulations of the RF Front-End, IF Amplifier and Buffer circuit in 130nm BiCMOS technology.

Table 33: Summary of results obtained in post-layout simulations.

Parameter	Value
Power Gain (S21) (dB)	14
Input Return Loss (S11) (dB)	-23
Noise Figure (dB)	4
1-dB Compression Point (dBm)	-32.24
$IIP_3$ (dBm)	-17.8
$I_{DC}$ (mA)	0.69
$P_{DC}$ (mW)	0.34
$Re\{Z_{in}\}$ ( $\Omega$ )	40.3
$Im\{Z_{in}\}$ ( $\Omega$ )	2.27

### 3.4.3 Experimental results

Figure 74 shows the die micrograph after fabrication of the RF Front-End, IF Amplifier and Buffer circuit in GlobalFoundries 130nm BiCMOS technology.

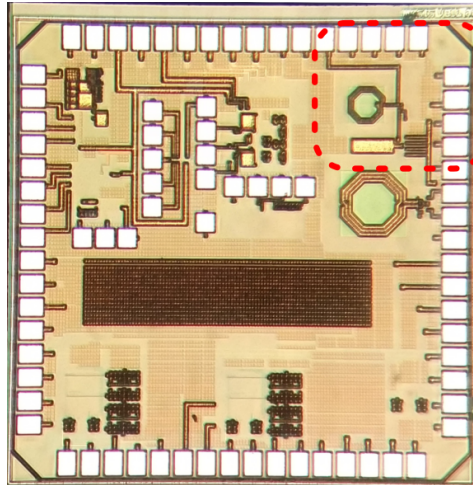


Figure 74: Die micrograph for the RF Front-End, IF Amplifier and Buffer circuit, fabricated in GlobalFoundries 130nm BiCMOS technology.

Source: Author

The design of the PCB for testing the fabricated circuit followed the strategy describes at the beginning of this chapter. Figure 75 shows the schematic capture of the PCB design realized using Autodesk EAGLE software.

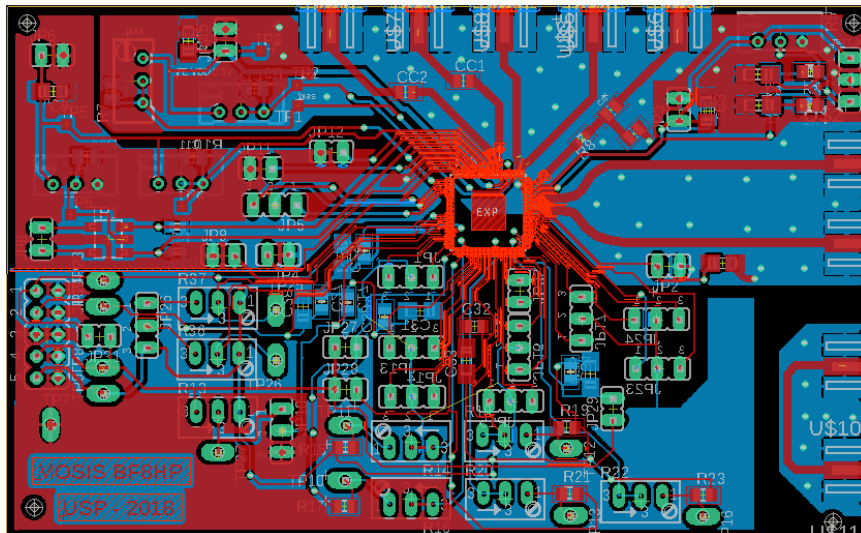


Figure 75: Schematic capture of the designed test PCB for the RF Front-End, IF Amplifier and Buffer circuit in Autodesk EAGLE software.

Source: Author

Figure 76 shows the fabricated test PCB. The placement of the die used a conventional

QFP packaging technology.

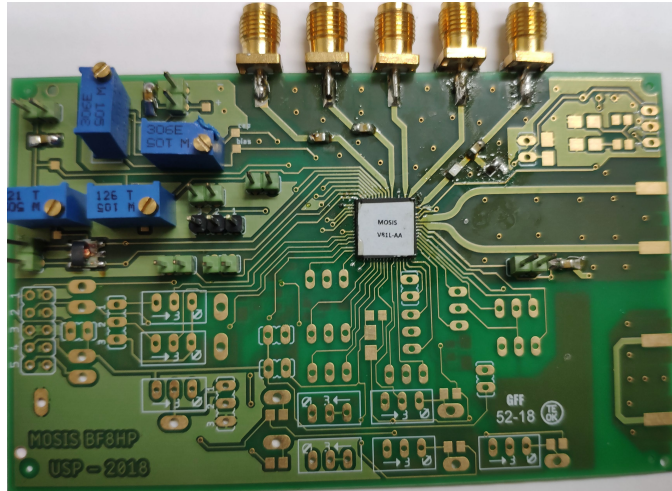


Figure 76: Fabricated test PCB for the RF Front-End, IF Amplifier and Buffer circuit.

Source: Author

After the test PCB fabrication, the experimental measurement of the fabricated circuits were performed. First, the S-Parameter measure with the Vector Network Analyzer (VNA) was performed, analyzing the unmatched circuit input to support the design of the passive input matching network design. After the input matching network realization in the PCB, the tests using Spectrum Analyzer and Oscilloscope were performed to observe the output characteristics of the downconverted signal, and the resulting conversion gain.

The S-Parameter data was obtained using the Vector Network Analyzer (VNA) model HP8510B [21], which was calibrated for the ISM band, from 1.5 GHz to 3.5 GHz.

Figure 77 shows the Smith Chart plot for the input reflection ratio ( $S_{11}$ ) obtained with the data extracted from the measurement with the VNA. It shows that before applying the matching circuit, the impedance was distant of the desired 50 ohm for 2.44 GHz.

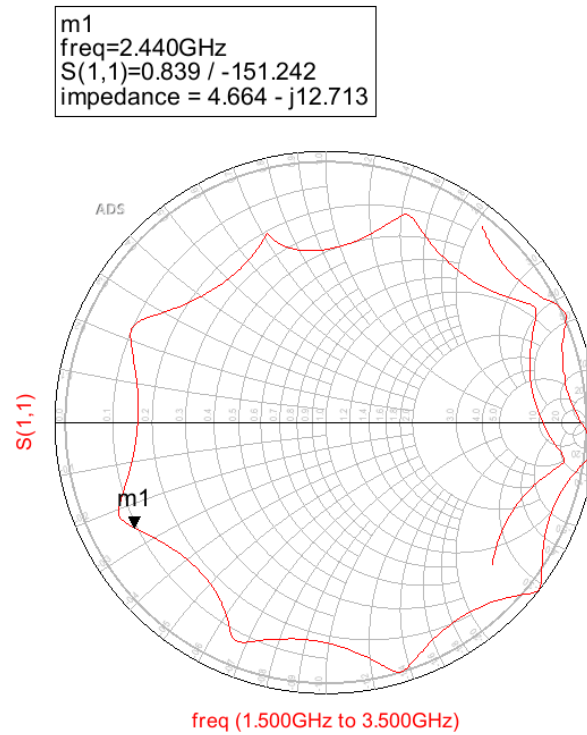


Figure 77: Smith Chart plot for S11 of experimental RF Front-End, IF Amplifier and Buffer circuit.

Source: Author

Figure 78 shows the S-Parameters measurement results with data extracted from the measurements in the VNA. It is possible to see that the input reflection (S11) is fairly high for all the band, showing no match, therefore no input selectivity.



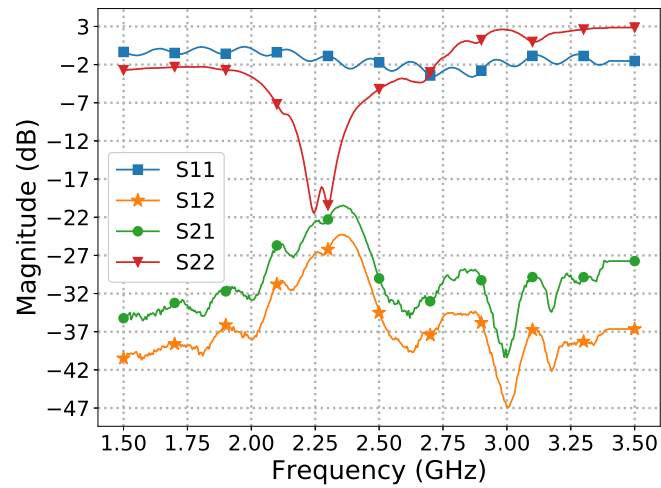


Figure 78: S-Parameter analysis of the experimental RF Front-End, IF Amplifier and Buffer circuit.

Source: Author

The extracted data was imported in the Keysight ADS software, as a way to design a proper input matching circuit. Figure 79 describe the matching procedure using LC elements. The procedure was performed using the Smith Chart Tool of Keysight ADS software. Starting from the impedance seen on the previous figure for the measured unmatched S11, the components were sized such that the final network could drive the input impedance seen at its input to  $50 \Omega$ .

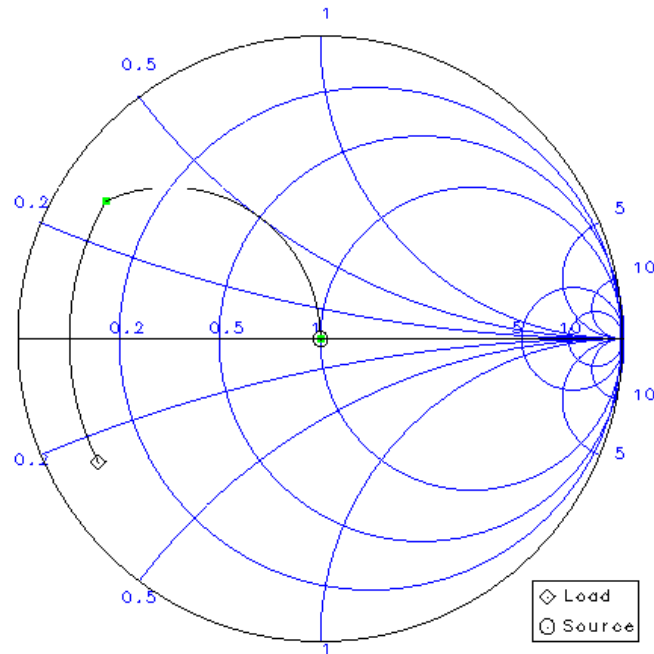


Figure 79: Impedance transformation performed by the Smith Chart Tool in the Keysight ADS software using the data extracted from the measurements of the unmatched RF Front-End, IF Amplifier and Buffer circuit.

Source: Author

Figure 80 describes the obtained LC network, in which the component values are described in the Table 34.

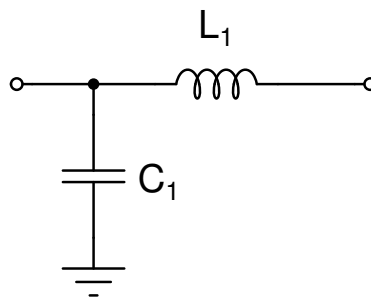


Figure 80: Designed ideal input matching circuit for the RF Front-End, IF Amplifier and Buffer circuit.

Source: Author

Table 34: Device dimensions for LC network input matching for the RF Front-End, IF Amplifier and Buffer circuit in 130nm BiCMOS technology.

Parameter	Ideal
$L_1$	1.8 nH
$C_1$	4.14 pF

Figure 81 shows the Smith Chart simulation for the input reflection ratio, S11, using the designed ideal matching network and the experimental data extracted from the unmatched RF Front-End, IF Amplifier and Buffer circuit.

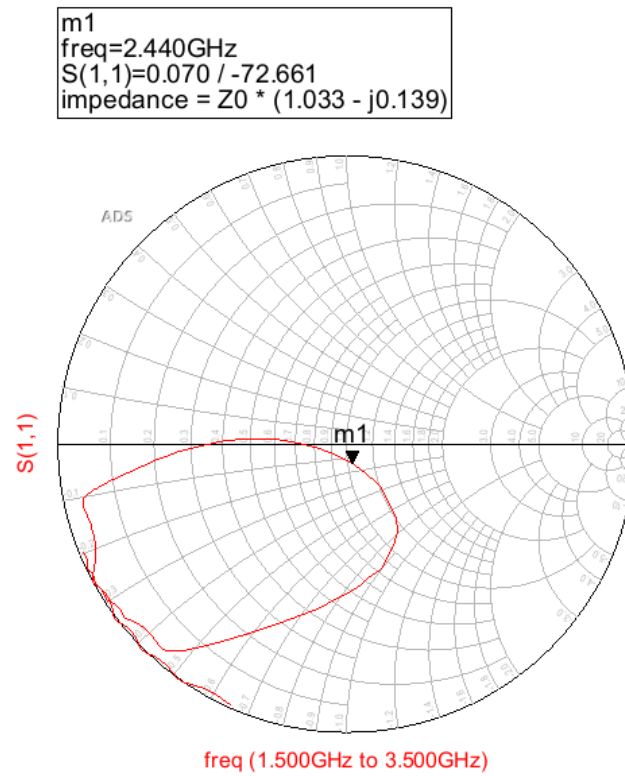


Figure 81: Smith Chart plot simulation for S11 of experimental RF Front-End circuit with designed LC matching.

Source: Author

Figure 82 shows the S-Parameters results using the ideal input matching and unmatched data from measurements of the RF Front-End, IF Amplifier and Buffer circuit.

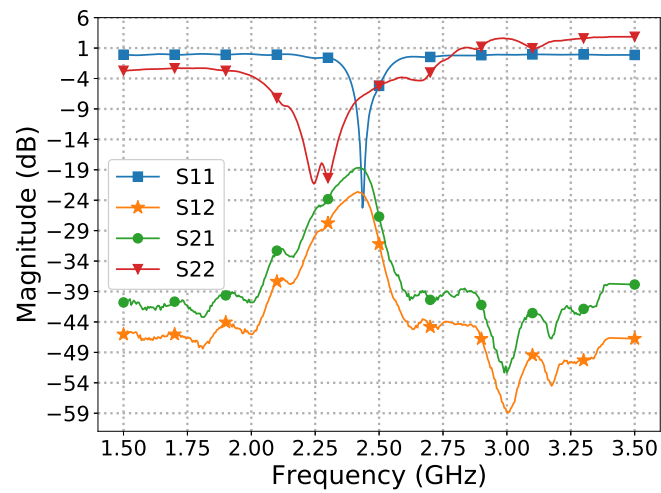


Figure 82: S-parameter simulation of experimental RF Front-End circuit with designed LC matching.

Source: Author

After the simulations using Keysight ADS, the values were rounded to a near commercial component value. With the adjusted component value, the input matching network was realized in the PCB. After adjustments in the PCB, the matching network elements were resized to better approximate the  $50 \Omega$  input impedance. The VNA was used to verify the input impedance. The final result of the measured RF Front-End, IF Amplifier and Buffer circuit using the real input matching is shown in figure 83.

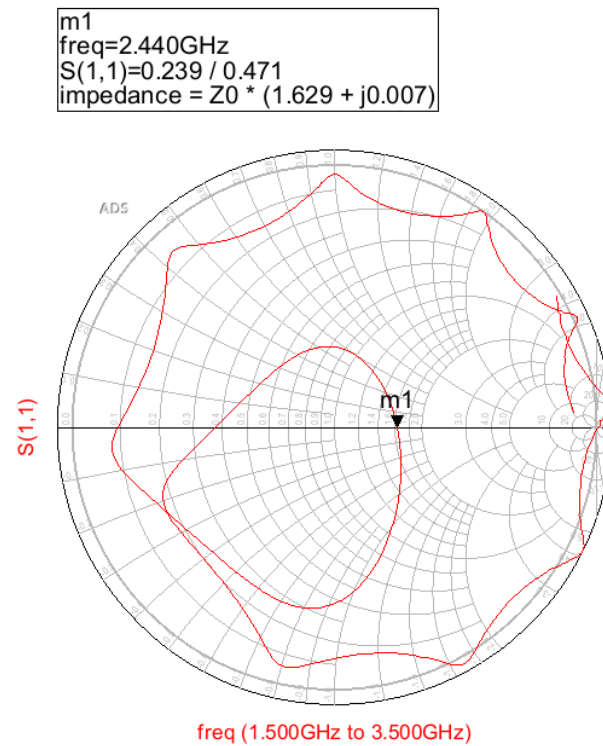


Figure 83: Smith Chart plot showing the measured S11 of the RF Front-End, IF Amplifier and Buffer circuit with the real input matching circuit realized in the PCB.

Source: Author

Figure 84 shows the result for the S-Parameter measurement performed by the VNA in the RF Front-End, IF Amplifier and Buffer circuit using the realized input matching circuit.

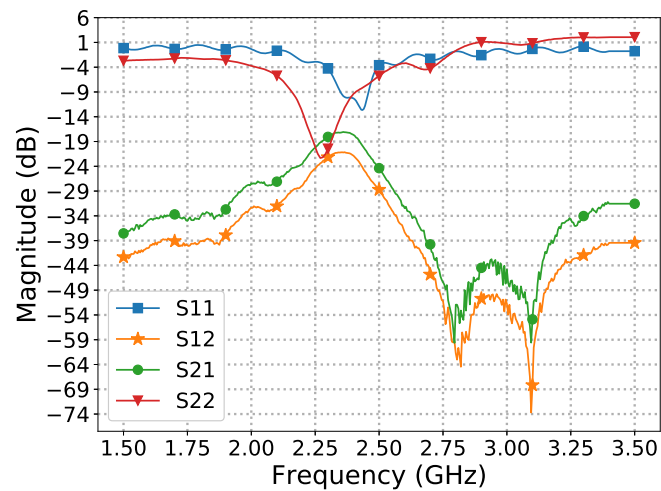


Figure 84: S-parameter measurement of experimental RF Front-End circuit with implemented LC matching.

Source: Author

Table 35 shows the values of the commercial components used to implement the real input matching network in the PCB.

Table 35: Device dimensions for the experimental LC network input matching for the RF Front-End, IF Amplifier and Buffer circuit in 130nm BiCMOS technology.

Parameter	Implemented
$L_1$	1.8 nH
$C_1$	1.1 pF

After the input matching measurements using the VNA, the Keysight Infiniivision DSOX6004A oscilloscope at 6 GSPS, was used to analyze the transient response of the circuits. The results include a low-pass filtering with 20 MHz passband, to allow the evaluation of the downconverted IF signal at 2 MHz. Figure 85 shows the resulting IF signal for a 2.44 GHz input. The figure includes the voltages at each output node, and the resulting differential output voltage.

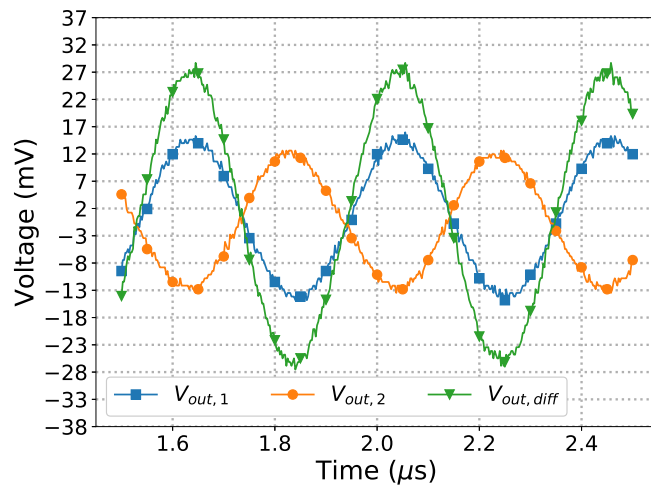


Figure 85: Differential and single-ended output signals for 0.5V supply.

Source: Author

Figure 86 shows the resulting IF signal for a 2.44 GHz input, at different supply voltage values.

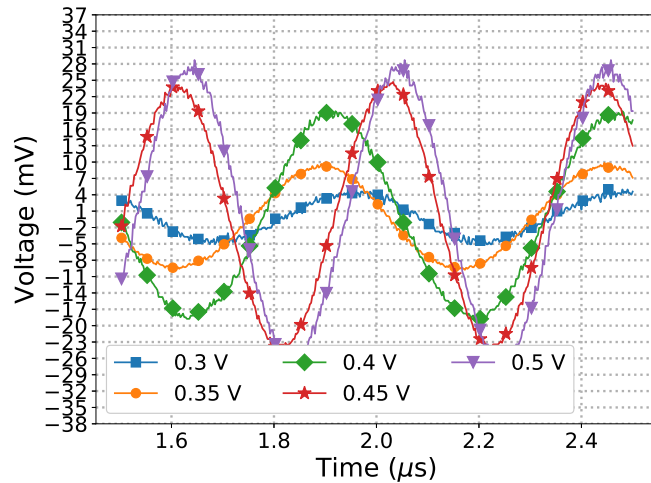


Figure 86: Transient output IF signal for different supply voltages.

Source: Author

Figure 87 shows a comparison between the output rms voltage  $V_{out}$  as a function of the supply voltage, and the input rms voltage  $V_{in}$ .

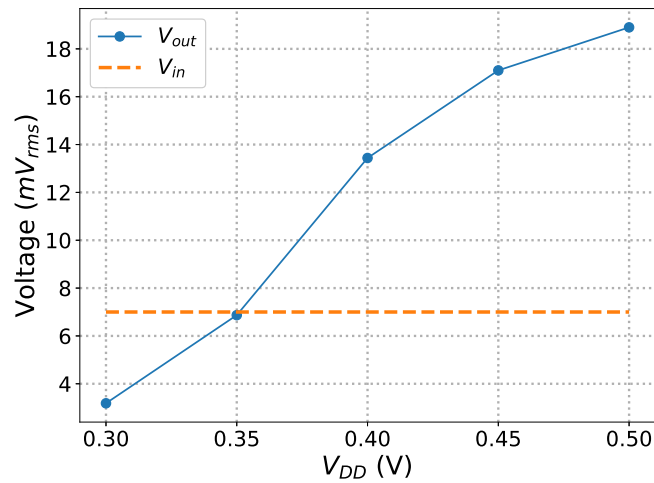


Figure 87: Input and output rms signals as a function of  $V_{DD}$ .

Source: Author

Table 36 shows the performance specifications achieved in experimental circuit.

Considering that power gain has suffered decrements from the buffer and from board unmatched transmission line parts.

Despite the higher power, it has a better band tuning and higher gain than the first fabricated circuit.

Table 36: Summary of results obtained in experimental circuit.

Parameter	Value
Power Gain (S21) (dB)	11
Input Return Loss (S11) (dB)	-58
$I_{DC}$ (mA)	0.7
$P_{DC}$ (mW)	0.35



## 4 CONCLUSION

In this chapter the main obtained results will be discussed, and also compared with the expected theoretical values.

### 4.1 Results Discussion

During the implementation phase of this work, three designs were performed. All the circuits are focused on low voltage and low power operation. First a LNA circuit was implemented in 180nm CMOS technology. Then, the LNA received improvements and was fabricated in the same technology node. Finally, the third design implemented a Front-End and IF amplifier system in a 130nm BiCMOS technology.

The circuits passed through post-layout simulations and experimental measurements to verify their proximity to the expected performance. In the case of 180nm technology, the area obtained was bigger, for the same performance specifications. Moreover, due to the use of low voltage, forward body biasing techniques were necessary to obtain a sufficient  $V_{th}$  reduction for proper device biasing, without it, the devices would operate in weak inversion region, thus needing prohibitively large area to achieve the required speed and transconductance, and in some cases even not having the required maximum transfer frequency for proper operation.

The noise analysis of the post-layout simulations showed good results, within the expected values, and since the BLE standard does not require very low values, the achieved performance was sufficient.

The linearity of the circuits proven to be very tied to the requirements in the post-layout simulations. The reduction on the supply voltage value imposed severe reduction on the maximum input voltage allowed. If the theoretical commonly used value of 0 dBm [26,27] was considered in the input, the gain compression and third intercept point at the input would be insufficient.

## 4.2 Future Works

For future works it would be of good contribution also include the design of the full Front-End system in a technology that impose the same  $V_{th}$  critical values as the 180nm technology used for the first two designs in this work. The study of the forward body biasing could be extend to the other blocks and evaluated from their point of view.

Linearity improvement techniques could be analyzed and applied to overcome the restrictions seen on the results of this work. In [56] linearization techniques using parallel PMOS devices would be applied to help. Also, differential implementations would be studied, however with added power and area.

A better analysis on the test boards could be applied to identify and solve transmission line problems that brought degradations to the matching on the experimental settings of this work. A design with help of a software capable of performing electromagnetic (EM) simulations would help to evaluate the influence of parasitic devices and transmission line nonlinearities.

It was observed that the sampling mixer impose a serious restriction due to necessity of using an input common mode voltage. With low supply voltage, this common mode voltage critically approaches the  $V_{DD} - V_{th}$  which limits the input voltage of the MOS switches and add nonlinearity behavior.

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